# NLAS4783

# Triple SPDT 1.0 Ω $R_{ON}$ Switch

The NLAS4783 is a triple independent ultra−low $R_{ON}$ SPDT analog switch with ENABLE. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS4783 can handle a balanced microphone/speaker/ring−tone generator in a monophone mode. The device contains a break−before−make feature.

### Features

- Single Supply Operation
  1.65 to 3.6 V $V_{CC}$
- Tiny 3 x 3 mm 16−Pin QFN Package
  Meets JEDEC MO−220 Specifications
- Low Static Power
- OVT on Logic Address and Enable Inputs
- This is a Pb−Free Device*

### Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone−Chip/Amplifier Switching
- Three Unbalanced (Single−Ended) Switches
- Stereo Balanced (Push−Pull) Switching

### Important Information

- ESD Protection:
  Human Body Model (HBM) > 8000 V
  Machine Model (MM) > 400 V
- Ringtone−Chip/Amplifier Switching
- Continuous Current Rating Through each Switch ±300 mA
- Conforms to: JEDEC MO−220, Issue H, Variation VEED−6
- Pin−for−Pin Compatible with MAX4783

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

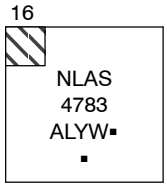
**ON Semiconductor®**

**http://onsemi.com**

**MARKING DIAGRAM**

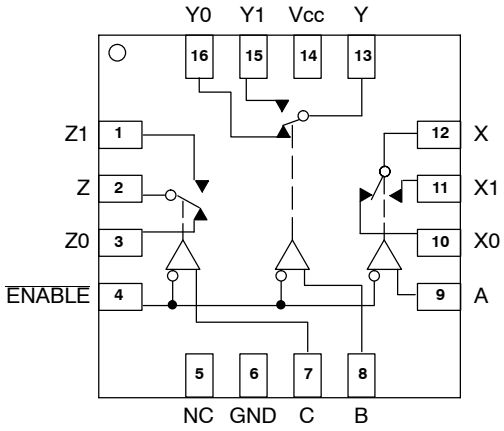



**QFN−16**
**CASE 485AE**




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**PIN CONNECTIONS**




**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

© Semiconductor Components Industries, LLC, 2008

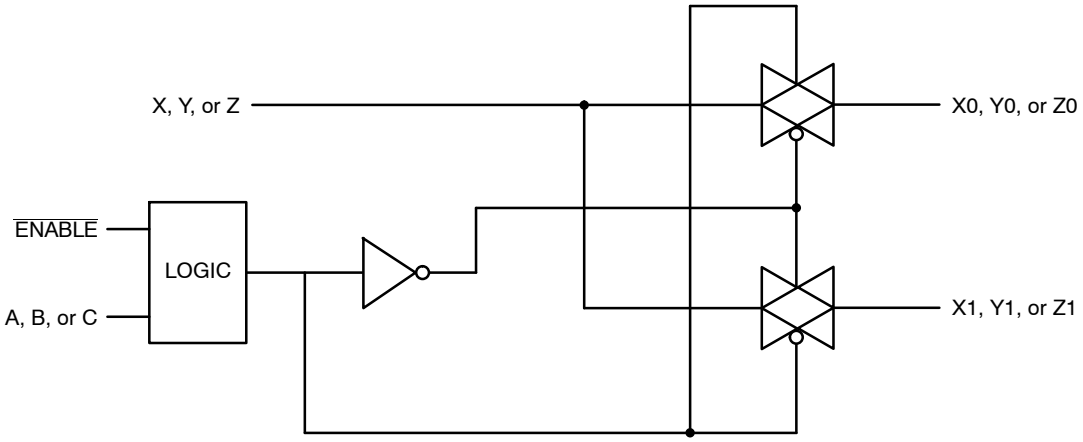



**Figure 1. Input Equivalent Circuit**

**PIN FUNCTION DESCRIPTION**

| QFN PIN # | Symbol | Description |
|---|---|---|
| 15 | Y1 | Analog Switch Y Normally Open Input |
| 16 | Y0 | Analog Switch Y Normally Closed Input |
| 1 | Z1 | Analog Switch Z Normally Open Input |
| 2 | Z | Analog Switch Z Output |
| 3 | Z0 | Analog Switch Z Normally Closed Input |
| 4 | $\overline{\text{ENABLE}}$ | Digital Enable Input. Normally connect to GND. Drive to logic high to set all switches off. |
| 5 | NC | No Connection. Not internally connected. |
| 6 | GND | Ground |
| 7 | C | Digital Address C Input |
| 8 | B | Digital Address B Input |
| 9 | A | Digital Address A Input |
| 10 | X0 | Analog Switch X Normally Closed Input |
| 11 | X1 | Analog Switch X Normally Open Input |
| 12 | X | Analog Switch X Output |
| 13 | Y | Analog Switch Y Output |
| 14 | $V_{CC}$ | Positive Analog and Digital Supply Voltage Input |

**TRUTH TABLE/SWITCH PROGRAMMING**

| Enable Input | Select Input | | | All Switches Open |
|---|---|---|---|---|
| | C | B | A | |
| H | X | X | X | |
| L | L | L | L | X–X0<br>Y–Y0<br>Z–Z0 |
| L | L | L | H | X–X1<br>Y–Y0<br>Z–Z0 |
| L | L | H | L | X–X0<br>Y–Y1<br>Z–Z0 |
| L | L | H | H | X–X1<br>Y–Y1<br>Z–Z0 |
| L | H | L | L | X–X0<br>Y–Y0<br>Z–Z1 |
| L | H | L | H | X–X1<br>Y–Y0<br>Z–Z1 |
| L | H | H | L | X–X0<br>Y–Y1<br>Z–Z1 |
| L | H | H | H | X–X1<br>Y–Y1<br>Z–Z1 |

1. Input and output pins are identical and interchangeable. Both pins can be considered input or output. Bidirectional signal pass.

**MAXIMUM RATINGS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | −0.5 to +4.6 | V |
| $V_{IS}$ | Analog Input Voltage ($V_{NO}$, $V_{NC}$, or $V_{COM}$) | −0.5 to $V_{CC}$ | V |
| $V_{IN}$ | Digital Select Input Voltage | −0.5 to +4.6 | V |
| $I_{anl1}$ | Continuous DC Current from COM to NC/NO | ±300 | mA |
| $I_{anl-pk\ 1}$ | Peak Current from COM to NC/NO, 10 Duty Cycles (Note 2) | ±500 | mA |
| $I_{clmp}$ | Continuous DC Current into COM/NC/NO with Respect to $V_{CC}$ or GND | ±100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Defined as 10% ON, 90% off duty cycle.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | 1.65 | 3.6 | V |
| $V_{IS}$ | Analog Input Voltage ($V_{NO}$, $V_{NC}$, or $V_{COM}$) | | – | $V_{CC}$ | V |
| $V_{IN}$ | Digital Select Input Voltage | | – | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −40 | 85 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Time, SELECT | $V_{CC}$ = 1.6–2.7 V<br>$V_{CC}$ = 3.0–3.6 V | –<br>– | 20<br>10 | ns/V |

**DC CHARACTERISTICS – Digital Section** (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ | Guaranteed Limit | | Unit |
|---|---|---|---|---|---|---|
| | | | | −40°C to 25°C | <85°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage, Select Inputs | | 1.65<br>2.7<br>3.6 | 1.0<br>1.4<br>1.8 | 1.0<br>1.4<br>1.8 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage, Select Inputs | | 1.65<br>2.7<br>3.6 | 0.4<br>0.5<br>0.6 | 0.4<br>0.5<br>0.6 | V |
| $I_{IN}$ | Maximum Input Leakage Current, Select Inputs | $V_{IN}$ = 3.6 V or GND | 3.6 | ± 0.1 | ± 1.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{IN}$ = 3.6 V or GND | 0 | ±0.5 | ±2.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (Note 3) | Select and $V_{IS}$ = $V_{CC}$ or GND | 1.65 to 3.6 | ± 1.0 | ± 2.0 | μA |

**DC ELECTRICAL CHARACTERISTICS – Analog Section**

| Symbol | Parameter | Condition | $V_{CC}$ | Guaranteed Maximum Limit | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | −40°C to 25°C | | <85°C | | |
| | | | | Min | Max | Min | Max | |
| $R_{ON}$ | NC/NO On−Resistance (Note 3) | $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$<br>$V_{IS}$ = GND to $V_{CC}$<br>$I_{IN}I \leq$ 100 mA | 2.7 – 3.6 | | 1.0 | | 1.2 | Ω |
| $R_{FLAT}$ | NC/NO On−Resistance Flatness (Notes 3, 5) | $I_{COM}$ = 100 mA<br>$V_{IS}$ = 0 to $V_{CC}$ | 2.7 – 3.6 | | 0.2 | | 0.2 | Ω |
| $\Delta R_{ON}$ | On−Resistance Match Between Channels (Notes 3 and 4) | $V_{IS}$ = 1.3 V;<br>$I_{COM}$ = 100 mA | 2.7 – 3.6 | | 0.4 | | 0.6 | Ω |
| $I_{NC(OFF)}$<br>$I_{NO(OFF)}$ | NC or NO Off Leakage Current (Note 3) | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$V_{NO}$ or $V_{NC}$ = 0.3 V<br>$V_{COM}$ = 3.3 V | 3.6 | −5.0 | 5.0 | −10 | 10 | nA |
| $I_{COM(ON)}$ | COM ON Leakage Current (Note 3) | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$V_{NO}$ 0.3 V or 3.3 V with $V_{NC}$ floating or<br>$V_{NC}$ 0.3 V or 3.3 V with $V_{NO}$ floating<br>$V_{COM}$ = 0.3 V or 3.3 V | 3.6 | −10 | 10 | −100 | 100 | nA |

3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
4. $\Delta R_{ON}$ = $R_{ON(MAX)}$ − $R_{ON(MIN)}$ between NC1 and NC2 or between NO1 and NO2.
5. Flatness is defined as the difference between the maximum and minimum value of on−resistance as measured over the specified analog signal ranges.

**AC ELECTRICAL CHARACTERISTICS** (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $V_{IS}$ (V) | Guaranteed Maximum Limit | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | −40°C to 25°C | | | <85°C | | |
| | | | | | Min | Typ* | Max | Min | Max | |
| $t_{ON}$ | Turn−On Time | $R_L$ = 50 Ω, $C_L$ = 35 pF (Figures 3 and 4) | 2.3 – 3.6 | 1.5 | | | 25 | | 27 | ns |
| $t_{OFF}$ | Turn−Off Time | $R_L$ = 50 Ω, $C_L$ = 35 pF (Figures 3 and 4) | 2.3 – 3.6 | 1.5 | | | 15 | | 20 | ns |
| $t_{BBM}$ | Minimum Break−Before−Make Time | $V_{IS}$ = 3.0 $R_L$ = 300 Ω, $C_L$ = 35 pF (Figure 2) | 3.0 | 1.5 | 2.0 | 8.0 | | | | ns |

| | | Typical @ 25, $V_{CC}$ = 3.6 V | |
|---|---|---|---|
| $C_{IN}$ | Control Pin Input Capacitance | 2.5 | pF |
| $C_{SN}$ | SN Port Capacitance | 75 | pF |
| $C_D$ | D Port Capacitance When Switch is Enabled | 240 | pF |

*Typical Characteristics are at 25°C.

**ADDITIONAL APPLICATION CHARACTERISTICS** (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Condition | $V_{CC}$ (V) | 25°C | Unit |
|---|---|---|---|---|---|
| | | | | Typical | |
| BW | Maximum On−Channel −3dB Bandwidth or Minimum Frequency Response | $V_{IN}$ centered between $V_{CC}$ and GND (Figure 5) | 1.65 – 3.6 | 17 | MHz |
| $V_{ONL}$ | Maximum Feed−through On Loss | $V_{IN}$ = 0 dBm @ 100 kHz to 50 MHz $V_{IN}$ centered between $V_{CC}$ and GND (Figure 5) | 1.65 – 3.6 | −0.10 | dB |
| $V_{ISO}$ | Off−Channel Isolation | f = 100 kHz; $V_{IS}$ = 1 V RMS; $C_L$ = 5 nF $V_{IN}$ centered between $V_{CC}$ and GND(Figure 5) (Note 6) | 1.65 – 3.6 | −62 | dB |
| Q | Charge Injection Select Input to Common I/O | $V_{IN}$ = $V_{CC\ to}$ GND, $R_{IS}$ = 0 Ω, $C_L$ = 1 nF Q = $C_L$ x $\Delta V_{OUT}$ (Figure 6) | 1.65 – 3.6 | 50 | pC |
| THD | Total Harmonic Distortion THD + Noise | $F_{IS}$ = 20 Hz to 20 kHz, $R_L$ = $R_{gen}$ = 600 Ω, $C_L$ = 50 pF $V_{IS}$ = 2 V RMS | 3.0 | 0.015 | % |
| VCT | Channel−to−Channel Crosstalk | f = 100 kHz; $V_{IS}$ = 1 V RMS, $C_L$ = 5 pF, $R_L$ = 50 Ω $V_{IN}$ centered between $V_{CC}$ and GND (Figure 5) | 1.65 – 3.6 | −62 | dB |

6. Off−Channel Isolation = 20log10 (Vcom/Vno), Vcom = output, Vno = input to off switch.

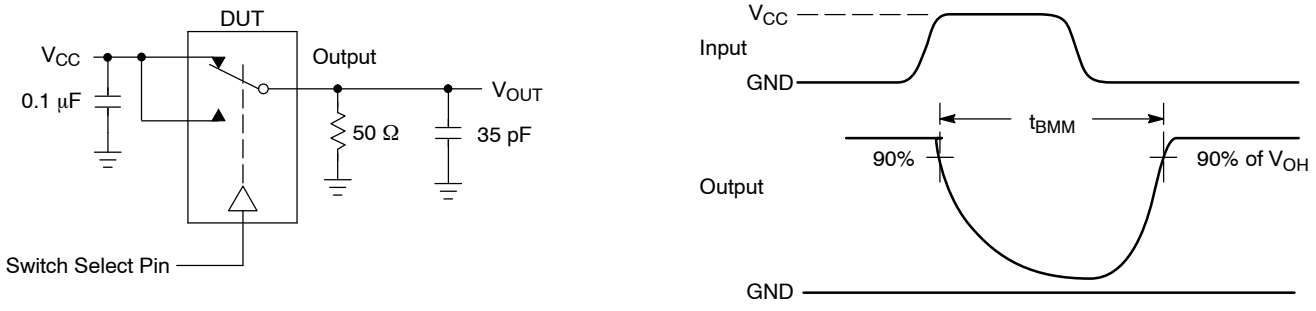



**Figure 2. $t_{BBM}$ (Time Break−Before−Make)**

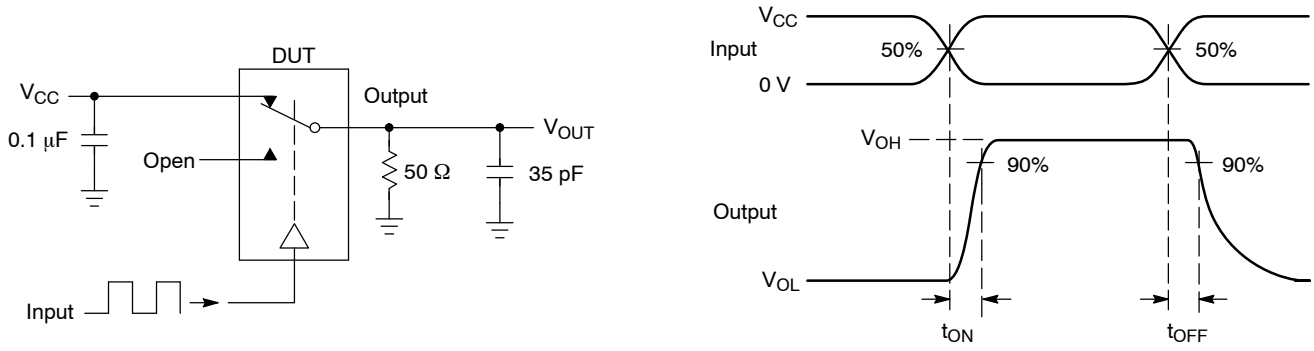



**Figure 3. $t_{ON}/t_{OFF}$**

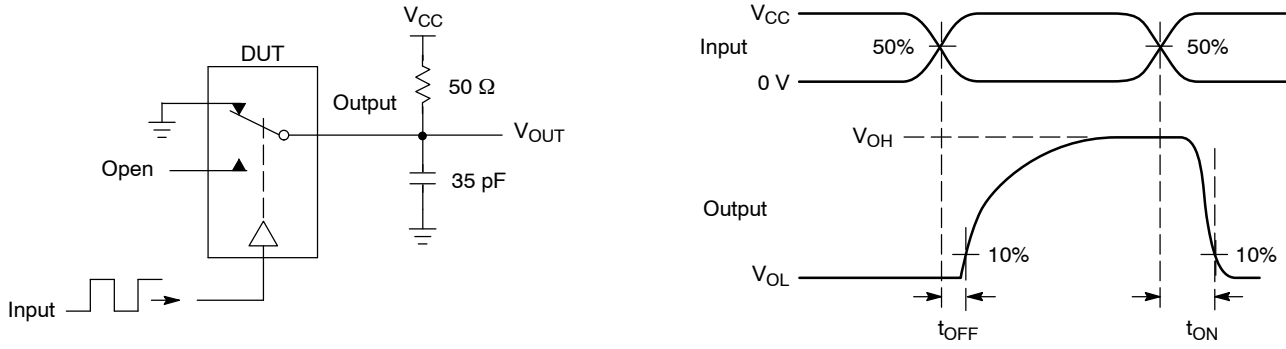
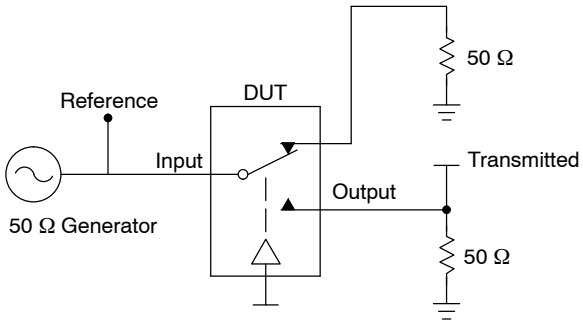



**Figure 4. $t_{ON}/t_{OFF}$**




Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. $V_{ISO}$, Bandwidth and $V_{ONL}$ are independent of the input signal direction.

$V_{ISO}$ = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for $V_{IN}$ at 100 kHz

$V_{ONL}$ = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for $V_{IN}$ at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below $V_{ONL}$
$V_{CT}$ = Use $V_{ISO}$ setup and test to all other switch analog input/outputs terminated with 50 Ω

**Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/$V_{ONL}$**

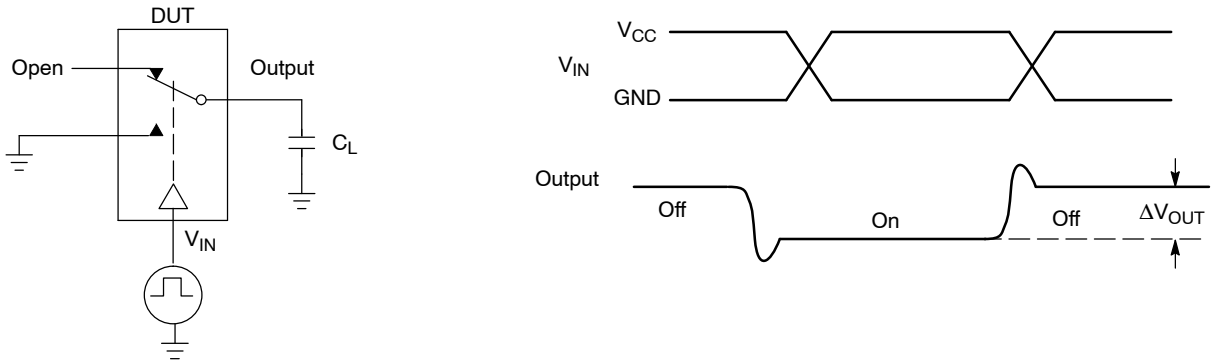



**Figure 6. Charge Injection: (Q)**

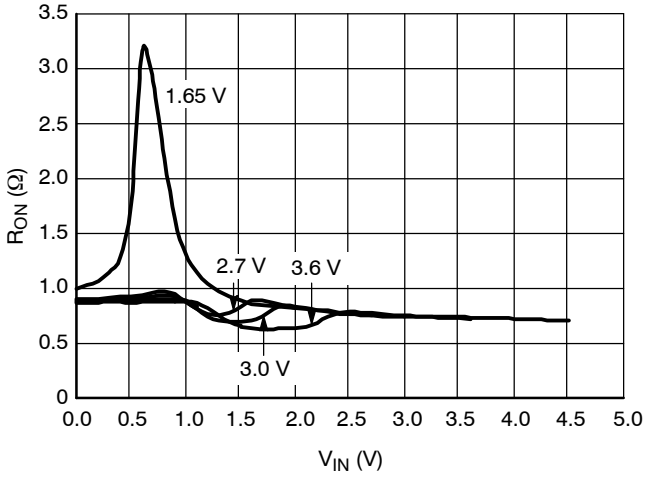



**Figure 7. On−Resistance vs. Input Voltage**

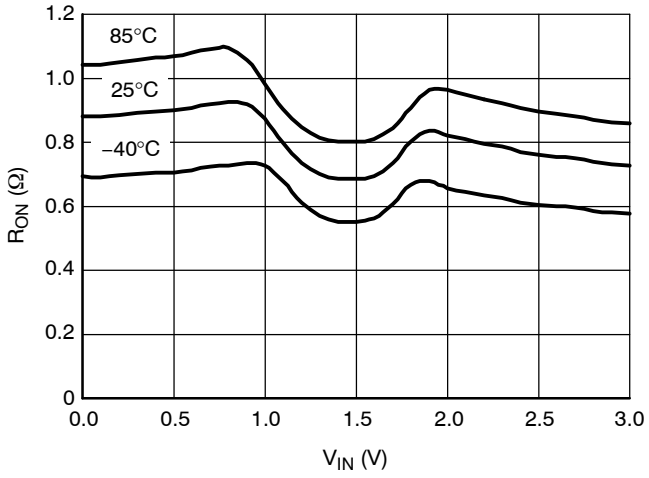



**Figure 8. $R_{ON}$ vs. $V_{IN}$ vs. Temperature @ $V_{CC}$ = 3.0 V**

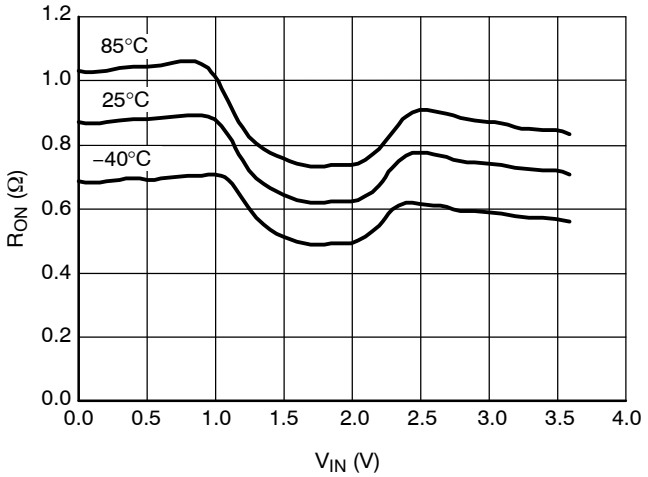



**Figure 9. $R_{ON}$ vs. $V_{IN}$ vs. Temperature @ $V_{CC}$ = 3.6 V**

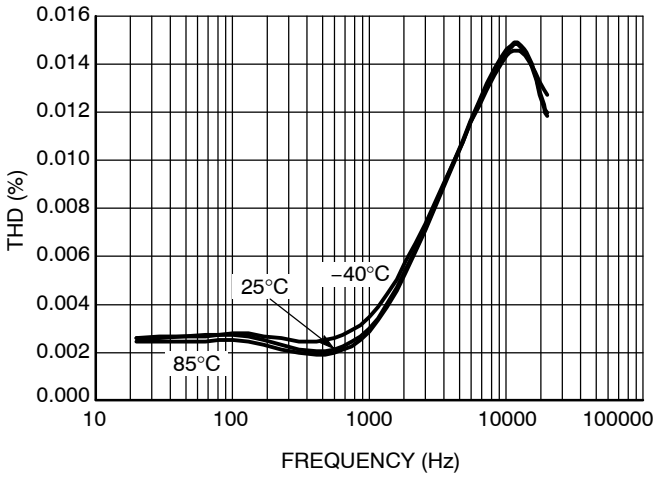



**Figure 10. Total Harmonic Distortion vs. Frequency**

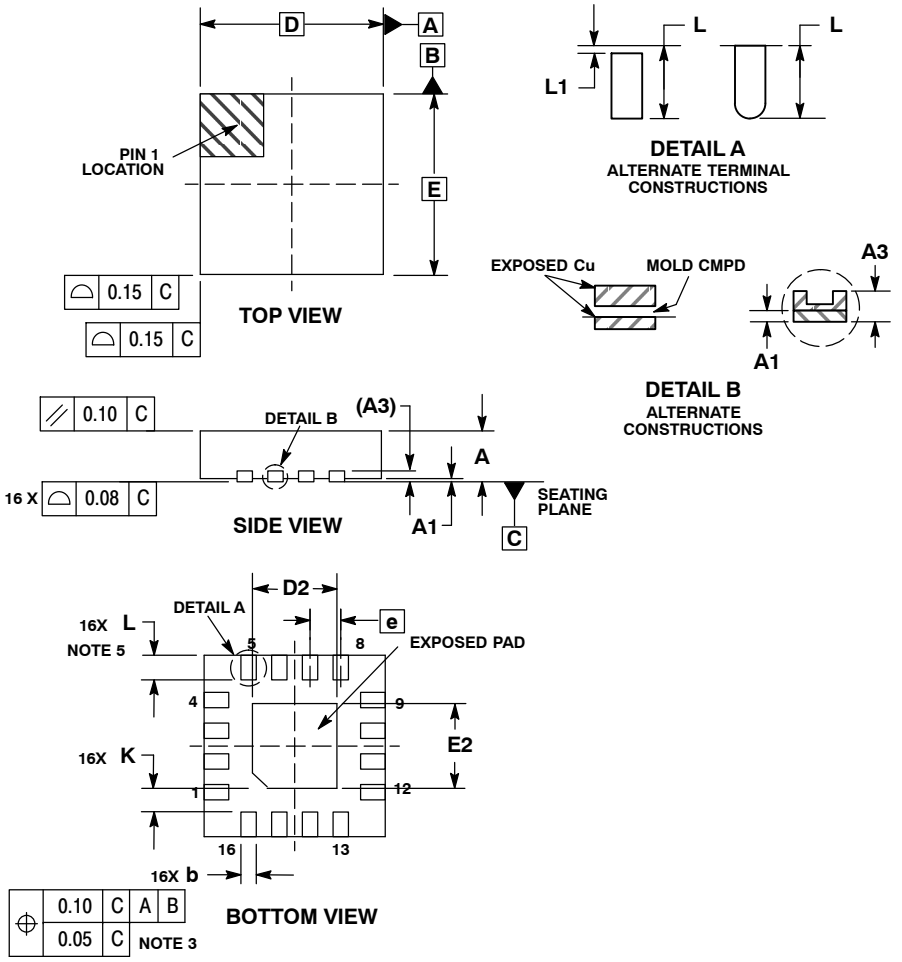
## ORDERING INFORMATION

| Device Order Number | Device Nomenclature | | | | Package Type | Tape & Reel Size† |
|---|---|---|---|---|---|---|
| | Circuit Indicator | Technology | Device Function | Tape & Reel Suffix | | |
| NLAS4783MN1R2G | NL | AS | 4783 | R2 | QFN (Pb−Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**QFN16 3x3, 0.5P**
CASE 485AE−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OUTLINE MEETS JEDEC DIMENSIONS PER MO−220, VARIATION VEED−6.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.03 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 3.00 BSC | |
| D2 | 1.25 | 1.40 | 1.55 |
| E | | 3.00 BSC | |
| E2 | 1.25 | 1.40 | 1.55 |
| e | | 0.50 BSC | |
| K | 0.20 | −−− | −−− |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.00 | −−− | 0.15 |

**ON Semiconductor** and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5773−3850

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative