NL17SHT04

Inverting Buffer / CMOS Logic Level Shifter
LSTTL−Compatible Inputs

The NL17SHT04 is a single gate inverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL−type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high−voltage power supply.

The NL17SHT04 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the NL17SHT04 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: t_{PD} = 3.8 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2 V
- CMOS−Compatible Outputs: V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @ Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- These are Pb−Free Devices

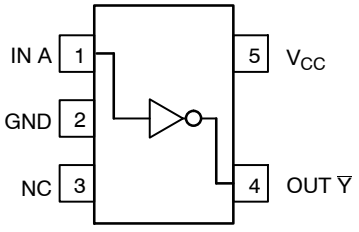


Figure 1. Pinout (Top View)

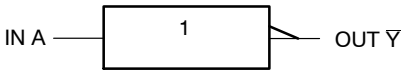


Figure 2. Logic Symbol

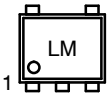
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



SOT−953
CASE 527AE



L = Specific Device Code
M = Month Code

PIN ASSIGNMENT	
1	IN A
2	GND
3	NC
4	OUT $\overline{Y}$
5	V_{CC}

FUNCTION TABLE

A Input	$\overline{Y}$ Output
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

© Semiconductor Components Industries, LLC, 2011

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	−0.5 to 7.0 −0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	±20	mA
I_{OUT}	DC Output Current		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		50	mA
P_D	Power dissipation in still air		50	mW
T_L	Lead temperature, 1 mm from case for 10 s		260	°C
T_J	Junction temperature under bias		+150	°C
T_{stg}	Storage temperature		−65 to +150	°C
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 1)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		3.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	0.0 0.0	5.5 V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

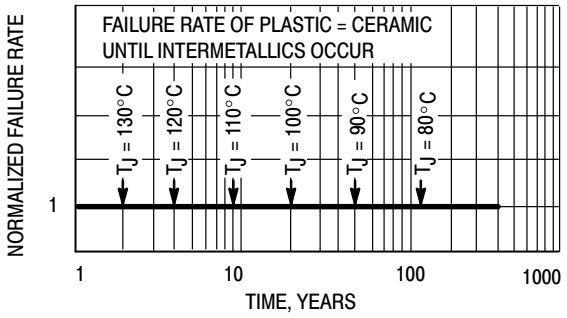


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		−55 ≤ $T_A \le$ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low−Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4.0 mA I_{OL} = 8.0 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C			$T_A \le$ 85°C		−55 ≤ $T_A \le$ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to $\overline{Y}$	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		5.0 6.2	10.0 13.5		11.0 15.0		13.0 17.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		3.8 4.2	6.7 7.7		7.5 8.5		8.5 9.5	
C_{IN}	Maximum Input Capacitance			5.0	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 2)	10	pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no−load dynamic power consumption; P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}.

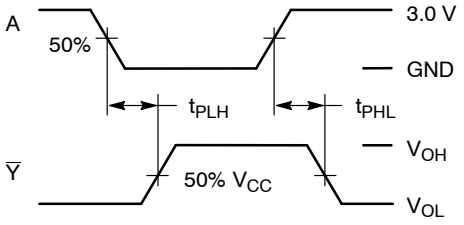
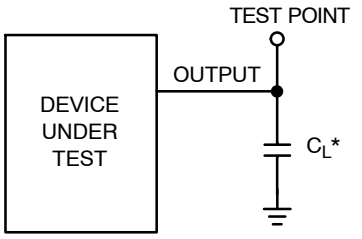


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

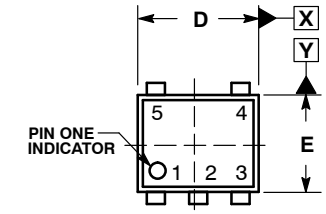
ORDERING INFORMATION

Device	Package Type	Package†
NL17SHT04P5T5G	SOT−953 (Pb−Free)	4000 / Tape & Reel

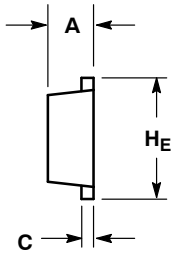
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

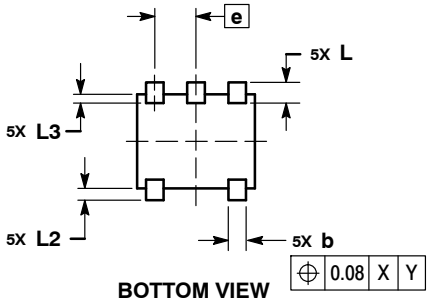
SOT−953
CASE 527AE
ISSUE E



TOP VIEW



SIDE VIEW

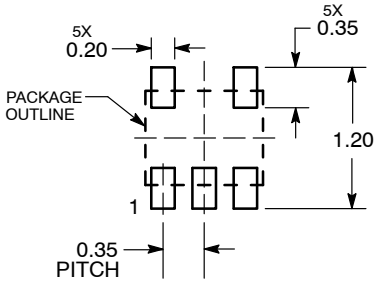


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NL17SHT04/D