NGD15N41CL, NGB15N41CL, NGP15N41CL

Preferred Device

Ignition IGBT 15 Amps, 410 Volts

N−Channel DPAK, D²PAK and TO−220

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over−Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil−on−Plug Applications
- DPAK Package Offers Smaller Footprint and Increased Board Space
- Gate−Emitter ESD Protection
- Temperature Compensated Gate−Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor (R_G) and Gate−Emitter Resistor (R_{GE})
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

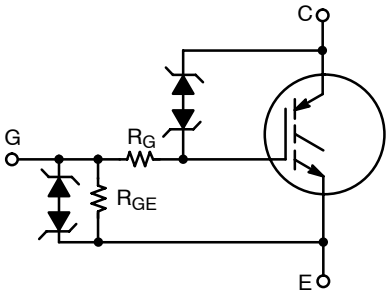
Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CES}	440	V_{DC}
Collector−Gate Voltage	V_{CER}	440	V_{DC}
Gate−Emitter Voltage	V_{GE}	15	V_{DC}
Collector Current−Continuous @ T_C = 25°C − Pulsed	I_C	15 50	A_{DC} A_{AC}
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	800	V
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	107 0.71	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +175	°C

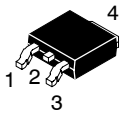
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ON Semiconductor®

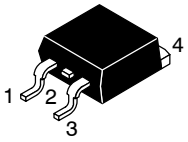
http://onsemi.com

15 AMPS
410 VOLTS
$V_{CE(on)}$ ≤ 2.1 V @
I_C = 10 A, V_{GE} ≥ 4.5 V

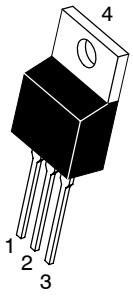




DPAK
CASE 369C
STYLE 2



D²PAK
CASE 418B
STYLE 4



TO−220AB
CASE 221A
STYLE 9

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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UNCLAMPED COLLECTOR−TO−EMITTER AVALANCHE CHARACTERISTICS ($-55° \le T_J \le 175°C$)

Characteristic	Symbol	Value	Unit
Single Pulse Collector−to−Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 16.6 A, L = 1.8 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 15 A, L = 1.8 mH, Starting T_J = 125°C	E_{AS}	 250 200	mJ

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$	1.4	°C/W
Thermal Resistance, Junction to Ambient	DPAK (Note 1)	$R_{\theta JA}$	100	
	D^2PAK (Note 1)	$R_{\theta JA}$	50	
	TO−220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector−Emitter Clamp Voltage	BV_{CES}	I_C = 2.0 mA	T_J = −40°C to 150°C	380	410	440	V_{DC}
		I_C = 10 mA	T_J = −40°C to 150°C	380	410	440	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 350 V, V_{GE} = 0 V	T_J = 25°C	−	2.0	20	μA_{DC}
			T_J = 150°C	−	10	40*	
			T_J = −40°C	−	1.0	10	
Reverse Collector−Emitter Leakage Current	I_{ECS}	V_{CE} = −24 V	T_J = 25°C	−	0.7	2.0	mA
			T_J = 150°C	−	12	25*	
			T_J = −40°C	−	0.1	1.0	
Reverse Collector−Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = −75 mA	T_J = 25°C	27	33	37	V_{DC}
			T_J = 150°C	30	36	40	
			T_J = −40°C	25	31	35	
Gate−Emitter Clamp Voltage	BV_{GES}	I_G = 5.0 mA	T_J = −40°C to 150°C	11	13	15	V_{DC}
Gate−Emitter Leakage Current	I_{GES}	V_{GE} = 10 V	T_J = −40°C to 150°C	384	640	1000	μA_{DC}
Gate Resistor	R_G	−	T_J = −40°C to 150°C	−	70	−	Ω
Gate Emitter Resistor	R_{GE}	−	T_J = −40°C to 150°C	10	16	26	kΩ
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GE(th)}$	I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = 25°C	1.1	1.4	1.9	V_{DC}
			T_J = 150°C	0.75	1.0	1.4	
			T_J = −40°C	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	−	−	−	−	3.4	−	mV/°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

*Maximum Value of Characteristic across Temperature Range.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
ON CHARACTERISTICS (continued) (Note 3)							
Collector−to−Emitter On−Voltage	$V_{CE(on)}$	I_C = 6.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.0	1.6	1.8	V_{DC}
			T_J = 150°C	0.9	1.5	1.8	
			T_J = −40°C	1.1	1.65	1.9*	
		I_C = 8.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.3	1.8	2.0*	
			T_J = 150°C	1.2	1.7	1.9	
			T_J = −40°C	1.4	1.8	2.0*	
		I_C = 10 A, V_{GE} = 4.0 V	T_J = 25°C	1.4	2.0	2.2	
			T_J = 150°C	1.5	2.0	2.3*	
			T_J = −40°C	1.4	2.0	2.2	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = 25°C	1.3	1.9	2.1	
			T_J = 150°C	1.3	1.9	2.1	
			T_J = −40°C	1.4	1.95	2.1*	
Forward Transconductance	gfs	V_{CE} = 5.0 V, I_C = 6.0 A	T_J = −40°C to 150°C	8.0	15	25	Mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{ISS}	V_{CC} = 25 V, V_{GE} = 0 V f = 1.0 MHz	T_J = −40°C to 150°C	400	650	1000	pF
Output Capacitance	C_{OSS}			30	55	100	
Transfer Capacitance	C_{RSS}			3.0	4.5	8.0	
SWITCHING CHARACTERISTICS							
Turn−Off Delay Time (Inductive)	$t_{d(off)}$	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, L = 300 μH	T_J = 25°C	–	4.0	10	μSec
			T_J = 150°C	–	4.5	10	
Fall Time (Inductive)	t_f	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, L = 300 μH	T_J = 25°C	–	6.0	12	
			T_J = 150°C	–	10	12	
Turn−Off Delay Time (Resistive)	$t_{d(off)}$	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	–	3.0	10	μSec
			T_J = 150°C	–	3.5	10	
Fall Time (Resistive)	t_f	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	–	8.0	15	
			T_J = 150°C	–	12	15	
Turn−On Delay Time	$t_{d(on)}$	V_{CC} = 10 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 1.5 Ω	T_J = 25°C	–	0.7	4.0	μSec
			T_J = 150°C	–	0.7	4.0	
Rise Time	t_r	V_{CC} = 10 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 1.5 Ω	T_J = 25°C	–	4.0	7.0	
			T_J = 150°C	–	5.0	7.0	

3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
*Maximum Value of Characteristic across Temperature Range.

TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

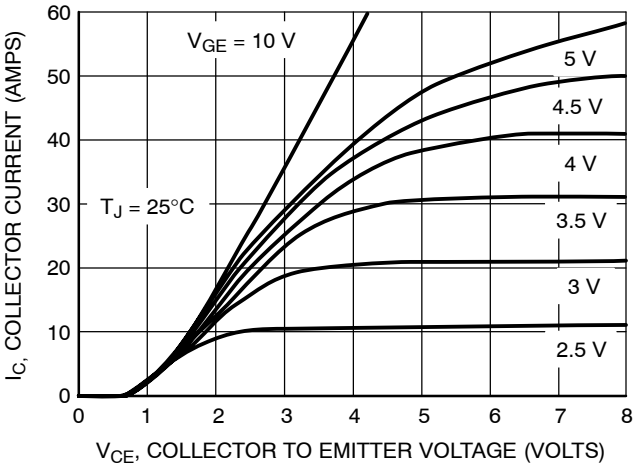


Figure 1. Output Characteristics

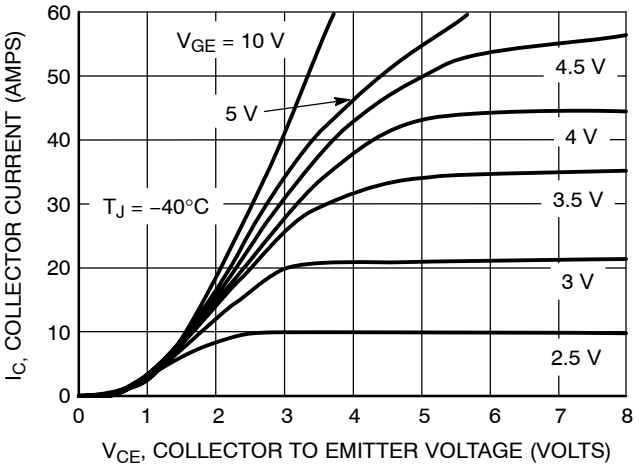


Figure 2. Output Characteristics

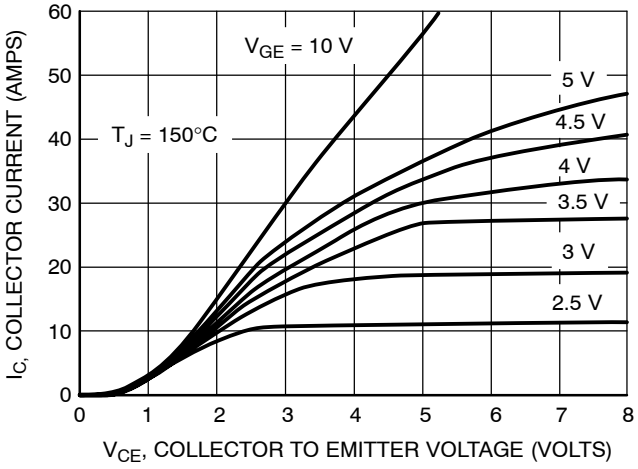


Figure 3. Output Characteristics

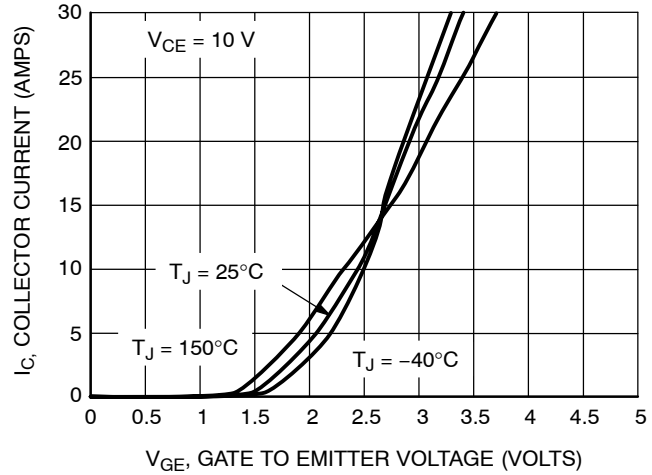


Figure 4. Transfer Characteristics

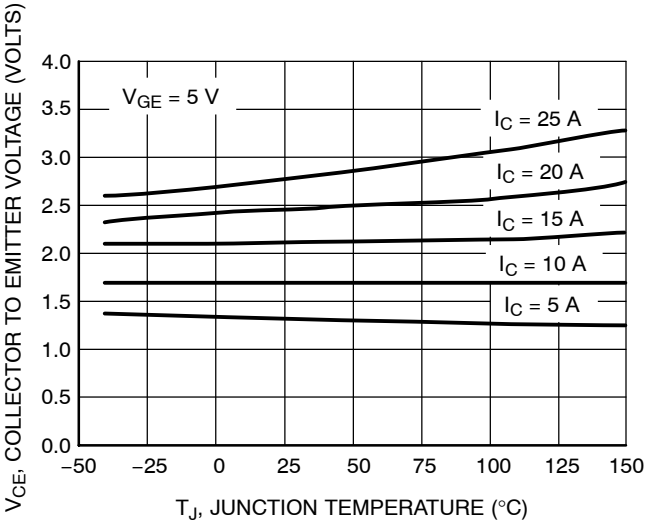


Figure 5. Collector−to−Emitter Saturation Voltage versus Junction Temperature

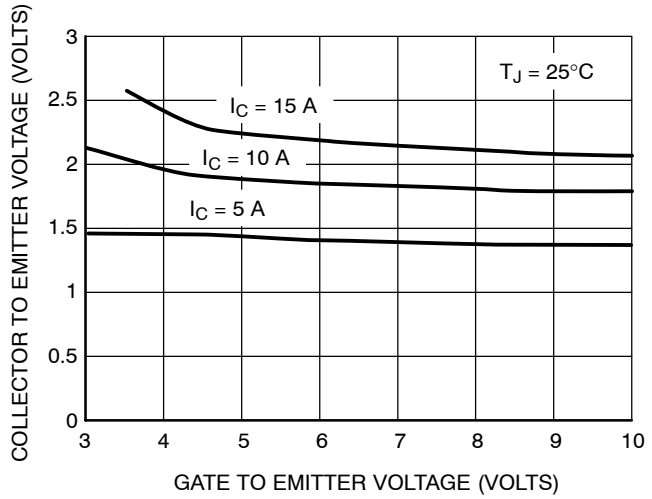


Figure 6. Collector−to−Emitter Voltage versus Gate−to−Emitter Voltage

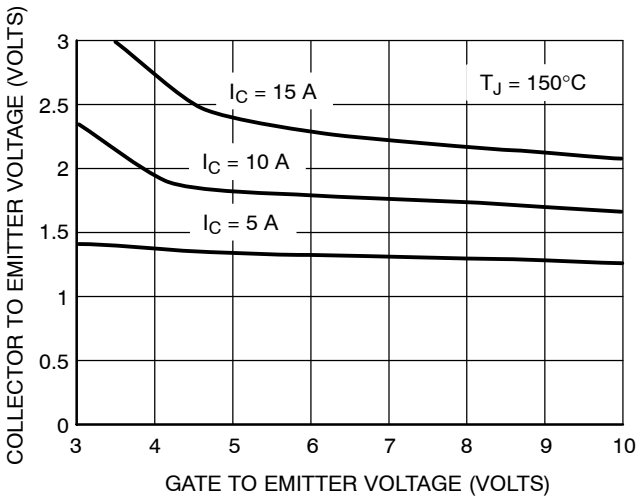


Figure 7. Collector−to−Emitter Voltage versus Gate−to−Emitter Voltage

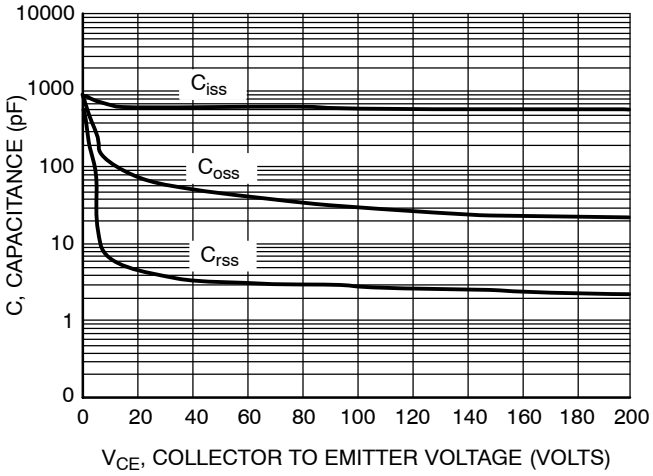


Figure 8. Capacitance Variation

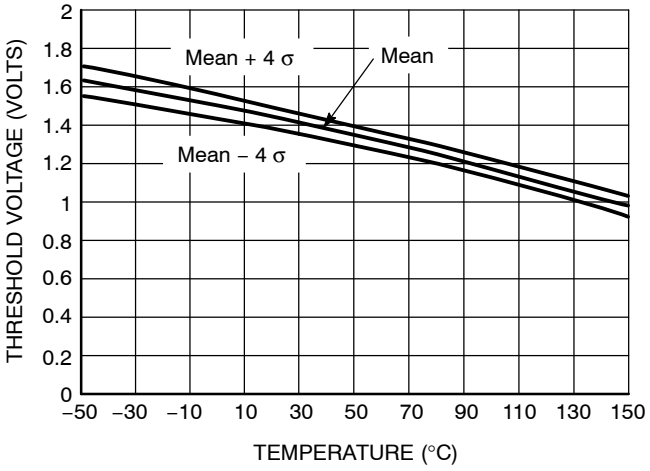


Figure 9. Gate Threshold Voltage versus Temperature

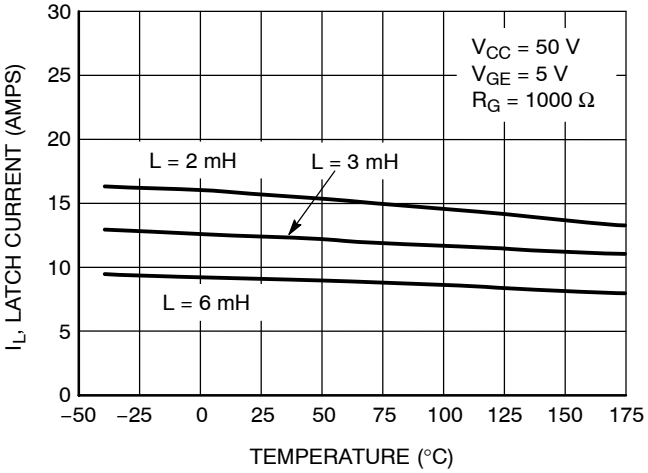


Figure 10. Minimum Open Secondary Latch Current versus Temperature

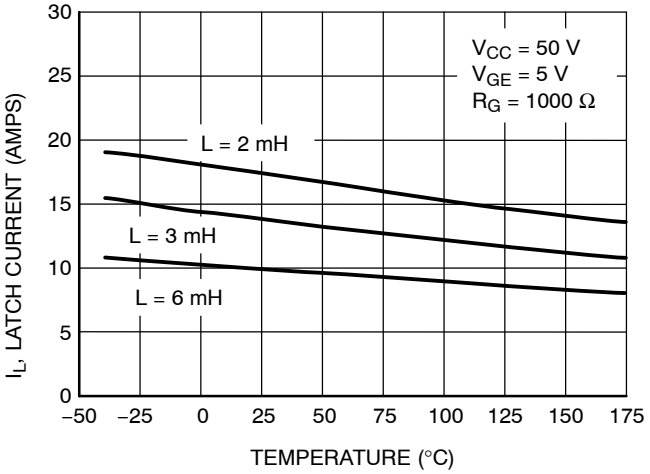


Figure 11. Typical Open Secondary Latch Current versus Temperature

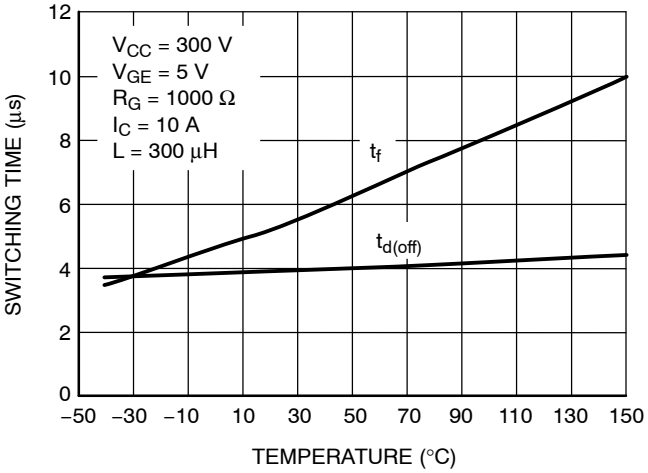


Figure 12. Inductive Switching Fall Time versus Temperature

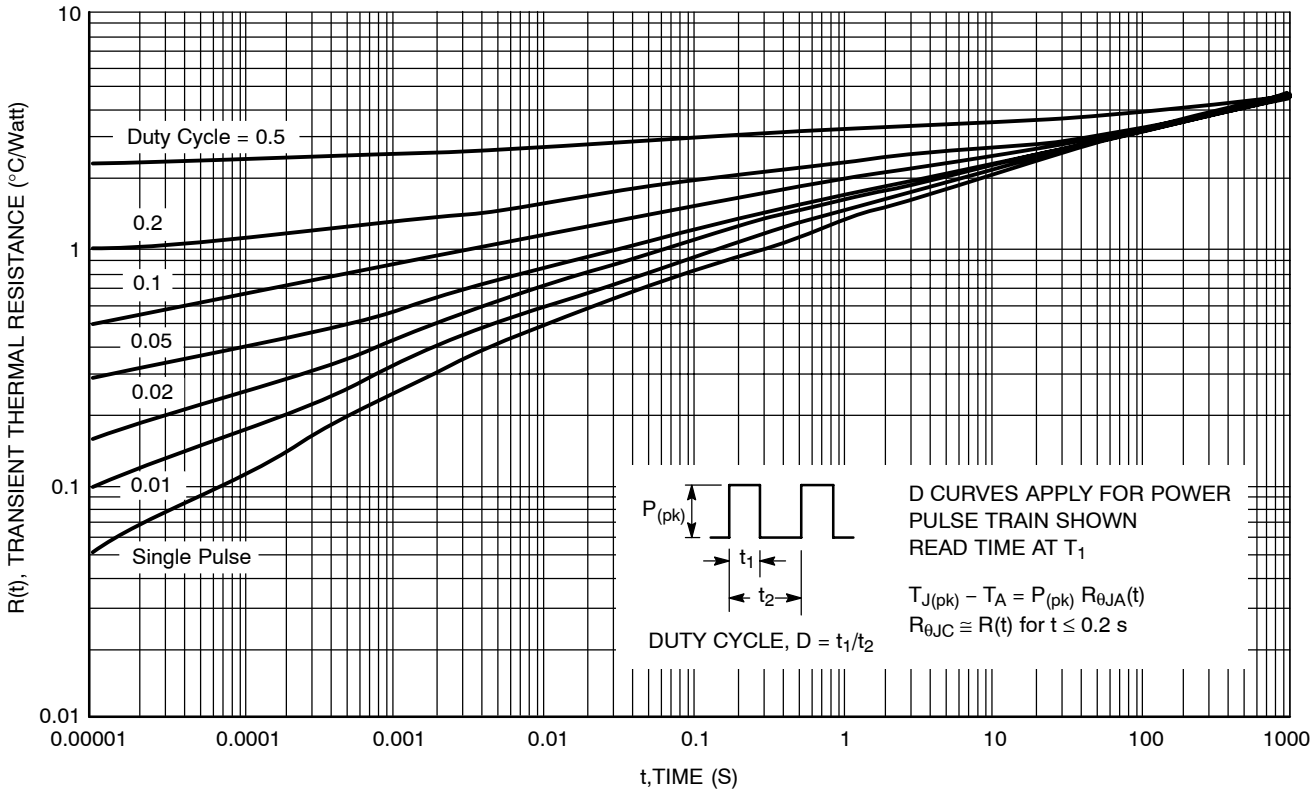


Figure 13. Transient Thermal Resistance (Non−normalized Junction−to−Ambient mounted on fixture in Figure 14)

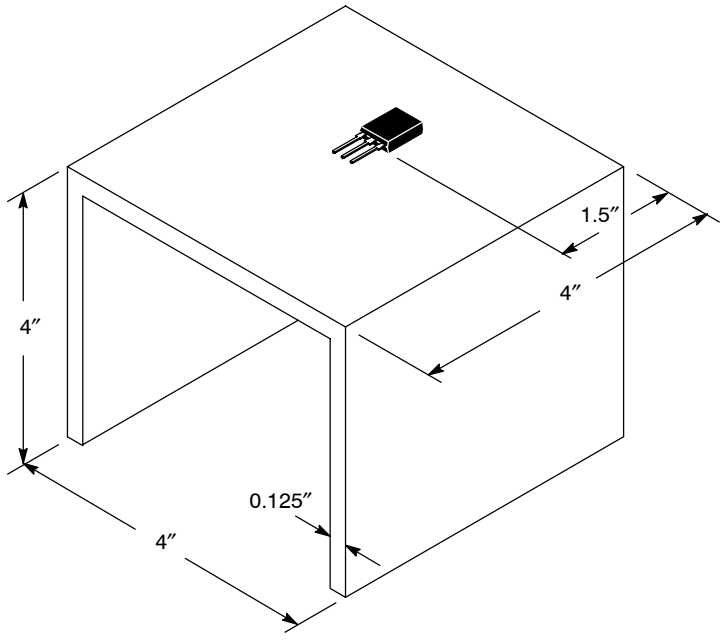


Figure 14. Test Fixture for Transient Thermal Curve (48 square inches of 1/8″ thick aluminum)

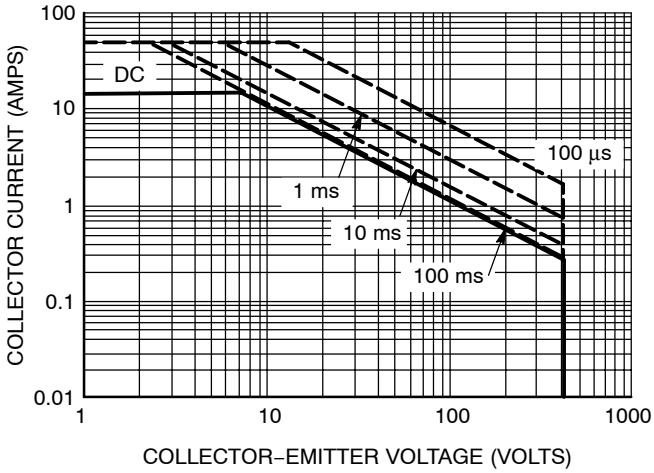


Figure 15. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_A = 25°C)

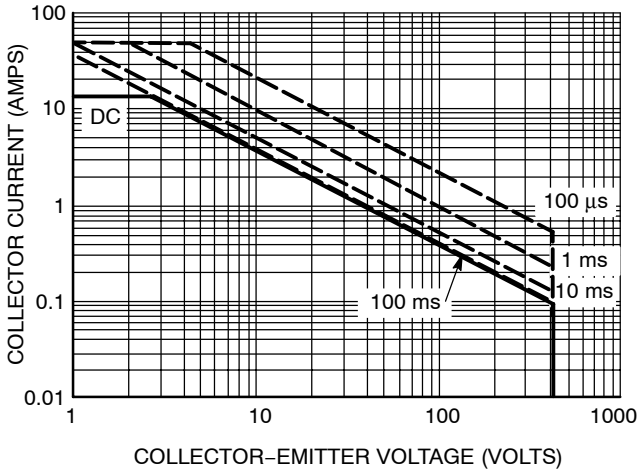


Figure 16. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_A = 125°C)

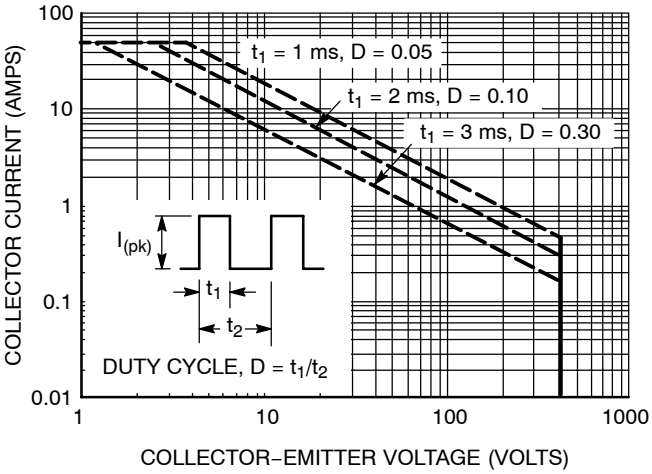


Figure 17. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 25°C)

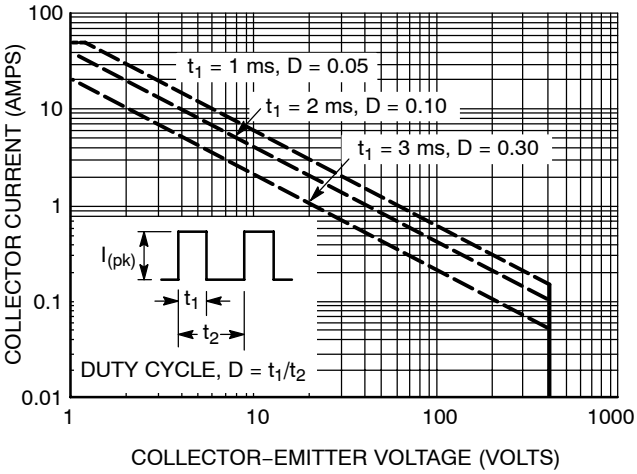


Figure 18. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 125°C)

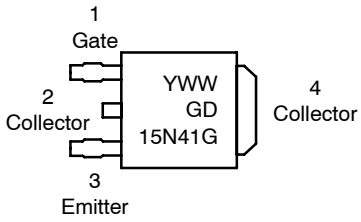
ORDERING INFORMATION

Device	Package Type	Shipping†
NGD15N41CLT4	DPAK	2500/Tape & Reel
NGD15N41CLT4G	DPAK (Pb−Free)	2500/Tape & Reel
NGB15N41CLT4	D^2PAK	800/Tape & Reel
NGB15N41CLT4G	D^2PAK (Pb−Free)	800/Tape & Reel
NGP15N41CL	TO−220	50 Units/Rail
NGP15N41CLG	TO−220 (Pb−Free)	50 Units/Rail

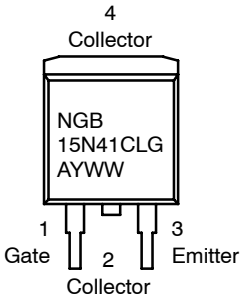
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MARKING DIAGRAMS

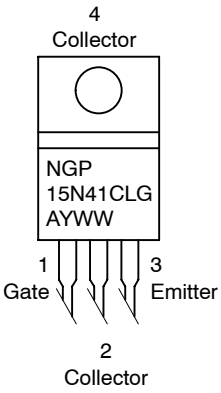
DPAK
CASE 369C
STYLE 7



D^2PAK
CASE 418B
STYLE 4



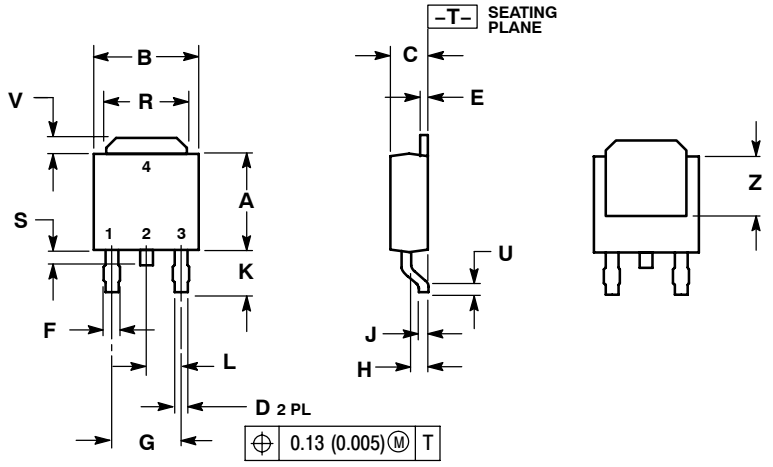
TO−220AB
CASE 221A
STYLE 9



A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Device

PACKAGE DIMENSIONS

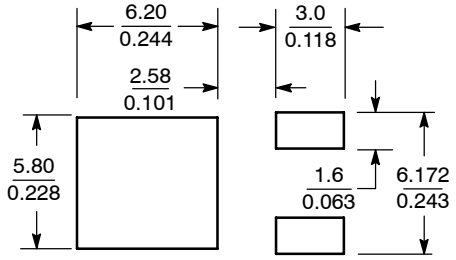
DPAK
CASE 369C−01
ISSUE O



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*

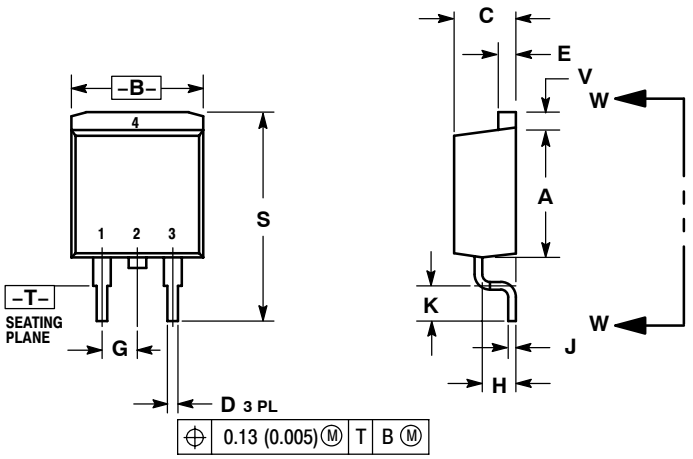


SCALE 3:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

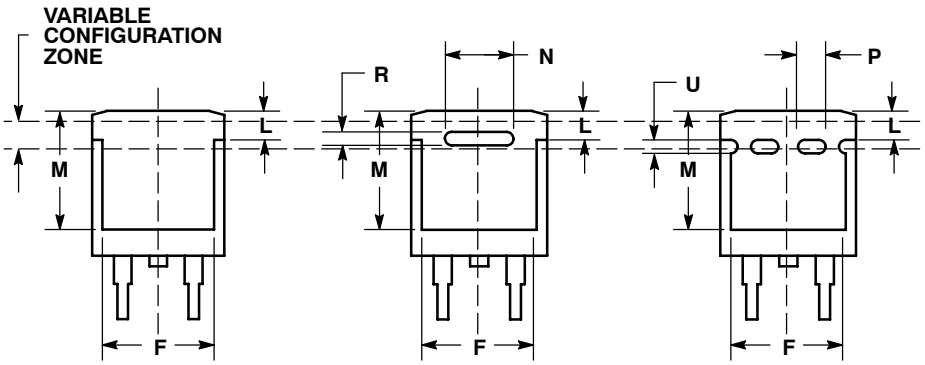
D²PAK
CASE 418B−04
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

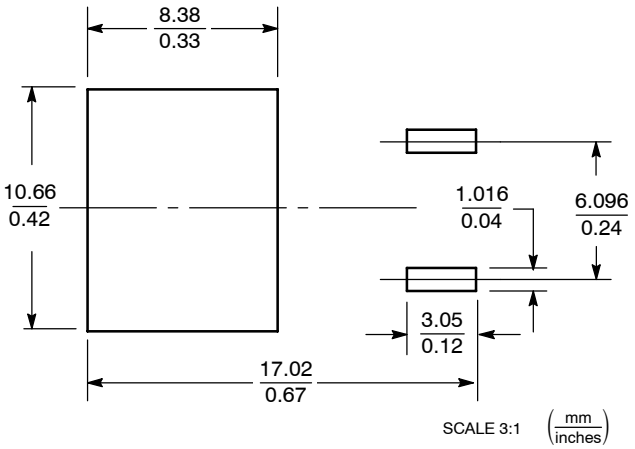
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

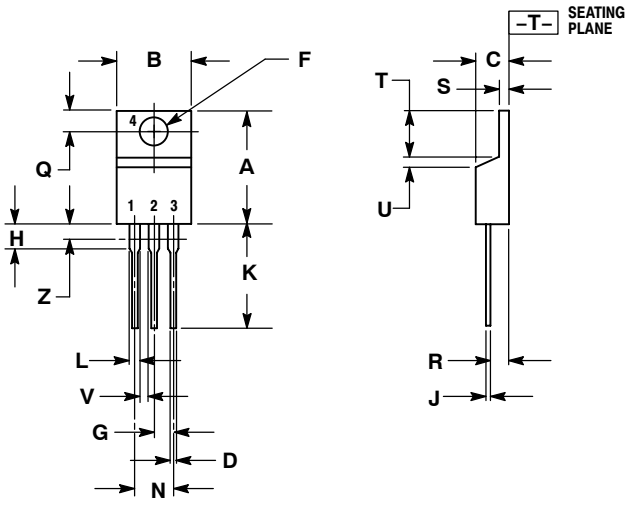
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.055	0.508	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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