NBSG14

2.5 V/3.3 V SiGe Differential 1:4 Clock/Data Driver with RSECL* Outputs

*Reduced Swing ECL

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QFN−16
MN SUFFIX
CASE 485G

Description

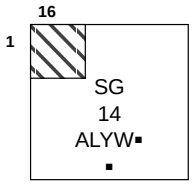
The NBSG14 is a 1-to-4 clock/data distribution chip, optimized for ultra-low skew and jitter.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV. All outputs loaded with 50 Ω to V_{CC} − 2 V.

Features

- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- These are Pb-Free Devices

MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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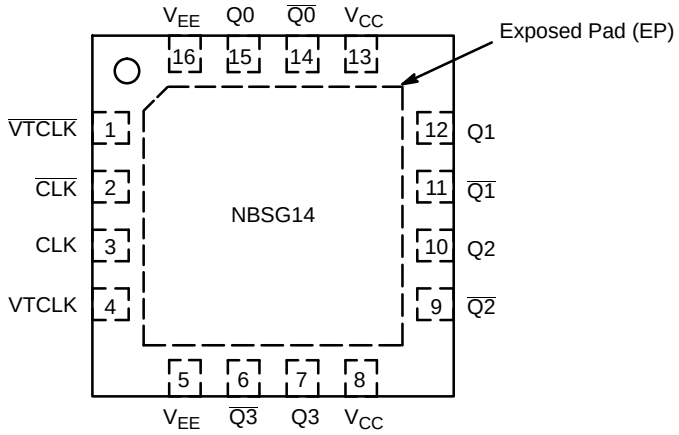


Figure 1. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{\text{VTCLK}}$	−	Internal 50 Ω Termination pin. See Table 2.
2	$\overline{\text{CLK}}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
3	CLK	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Internal 75 kΩ to VEE.
4	VTCLK	−	Internal 50 Ω Termination Pin. See Table 2.
5, 16	V_{EE}	−	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
6	$\overline{\text{Q3}}$	RSECL Output	Inverted Differential Output 3. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
7	Q3	RSECL Output	Noninverted Differential Output 3. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
8, 13	V_{CC}	−	Positive Supply Voltage. All V_{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
9	$\overline{\text{Q2}}$	RSECL Output	Inverted Differential Output 2. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
10	Q2	RSECL Output	Noninverted Differential Output 2. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
11	$\overline{\text{Q1}}$	RSECL Output	Inverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
12	Q1	RSECL Output	Noninverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
14	$\overline{\text{Q0}}$	RSECL Output	Inverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
15	Q0	RSECL Output	Noninverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pins (VTCLK, $\overline{\text{VTCLK}}$) are connected to a common termination voltage, if no signal is applied then the device will be susceptible to self-oscillation.

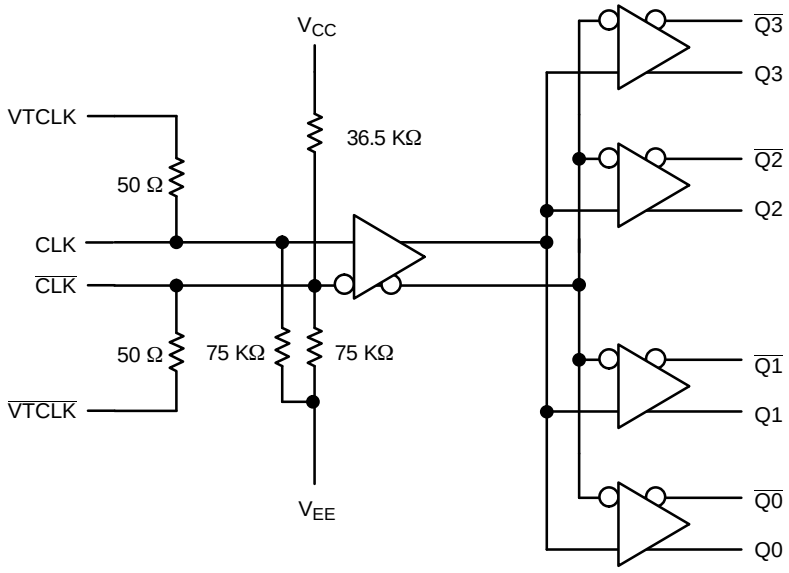


Figure 2. Logic Diagram

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and $\overline{VTCLK}$ to V_{CC}
LVDS	Connect VTCLK and $\overline{VTCLK}$ Together
AC−COUPLED	Bias VTCLK and $\overline{VTCLK}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An External Voltage (V_{th}) should be Applied to the Unused Differential Input. Nominal V_{th} is 1.5 V for LVTTL and V_{CC}/2 for LVCMOS Inputs. This Voltage must be within the V_{th} Specification.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (CLK, $\overline{CLK}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{CLK}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	Pb-Free	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		158
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V
V_{INPP}	Differential Input Voltage |CLK−$\overline{CLK}$|	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\|V_{CC}-V_{EE}\|$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA
I_{OUT}	Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			−40 to +70 −40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 2)	0 lfpm 500 lfpm		41.6 35.2	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 2)		4.0	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT
(V_{CC} = 2.5 V; V_{EE} = 0 V) (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
RSPECL OUTPUTS (Note 4)											
V_{OH}	Output HIGH Voltage	1525	1575	1625	1550	1610	1650	1575	1635	1675	mV
V_{OUTPP}	Output Voltage Amplitude	315	405	495	315	405	495	315	405	495	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 5)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 6)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 7)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 8) (Figure 9)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@V_{IL})		25	100		25	100		25	100	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}.
4. All outputs loaded with 50 Ω to V_{CC} − 2.0 V.
5. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
6. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT
(V_{CC} = 3.3 V; V_{EE} = 0 V) (Note 9)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
RSPECL OUTPUTS (Note 10)											
V_{OH}	Output HIGH Voltage	2325	2375	2425	2350	2410	2450	2375	2435	2475	mV
V_{OUTPP}	Output Voltage Amplitude	350	440	530	350	440	530	350	440	530	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 11)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 12)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 13)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14) (Figure 9)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@V_{IL})		25	100		25	100		25	100	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with V_{CC}.
10. All outputs loaded with 50 Ω to V_{CC} − 2.0 V.
11. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
12. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
13. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
14. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, NECL or RSNECL INPUT WITH NECL OUTPUT
(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V) (Note 15)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
RSPECL OUTPUTS (Note 16)											
V_{OH}	Output HIGH Voltage	−975	−925	−875	−950	−890	−850	−925	−865	−825	mV
V_{OUTPP}	Output Voltage Amplitude −3.465 V ≤ V_{EE} ≤ −3.0 V −3.0 V < V_{EE} ≤ −2.375 V	 350 315	 440 405	 530 495	 350 315	 440 405	 530 495	 350 315	 440 405	 530 495	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 17)											
V_{IH}	Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 18)	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 19)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 20) (Figure 9)	V_{EE} + 1200		0	V_{EE} + 1200		0	V_{EE} + 1200		0	mV
I_{IH}	Input HIGH Current (@V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@V_{IL})		25	100		25	100		25	100	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

15. Input and output parameters vary 1:1 with V_{CC}.
16. All outputs loaded with 50 Ω to V_{CC} − 2.0 V.
17. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
18. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
19. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. AC CHARACTERISTICS

(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Input Clock Frequency (See Figure 3) (Note 21)	10.5	12		10.5	12		10.5	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
t_{SKEW}	Duty Cycle Skew (Note 22) Within-Device Skew (Note 23) Device-to-Device Skew (Note 24)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
t_{JITTER}	RMS Random Clock Jitter (Figure 3) (Note 26) f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter (Note 27) f_{in} < 10 Gb/s		0.2	1		0.2 10	1		0.2	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 25)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%) @ 1 GHz	15	30	55	20	30	55	20	30	55	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

21. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%)
22. See Figure 10. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.
23. Within-Device skew is measured between outputs under identical transitions and conditions on any one device.
24. Device-to-Device skew for identical transitions at identical V_{CC} levels.
25. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (applicable only when $V_{CC}-V_{EE}$ < 2600 mV).
26. Additive RMS Jitter with 50% duty cycle clock signal at 10 GHz.
27. Additive Peak-to-Peak data dependent jitter with NRZ PRBS 2^{31}–1 data at 10 Gb/s.

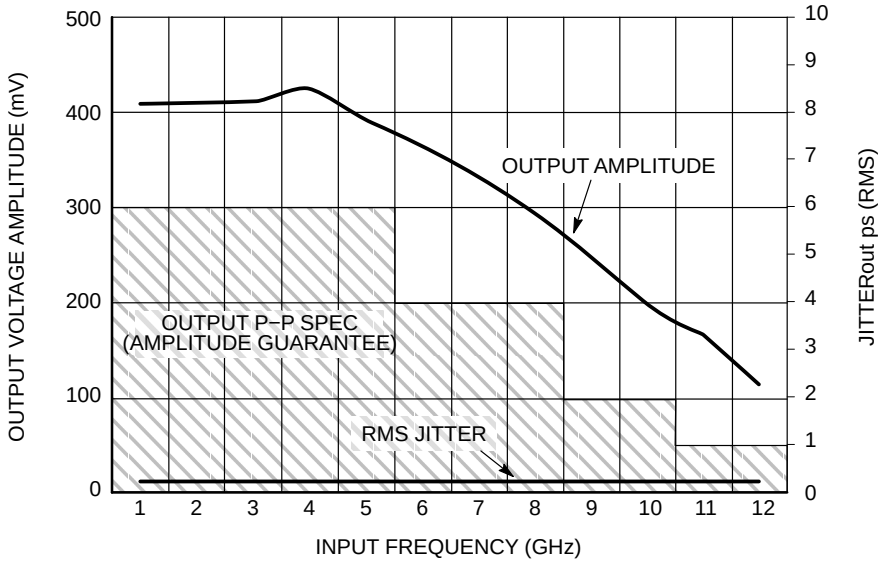
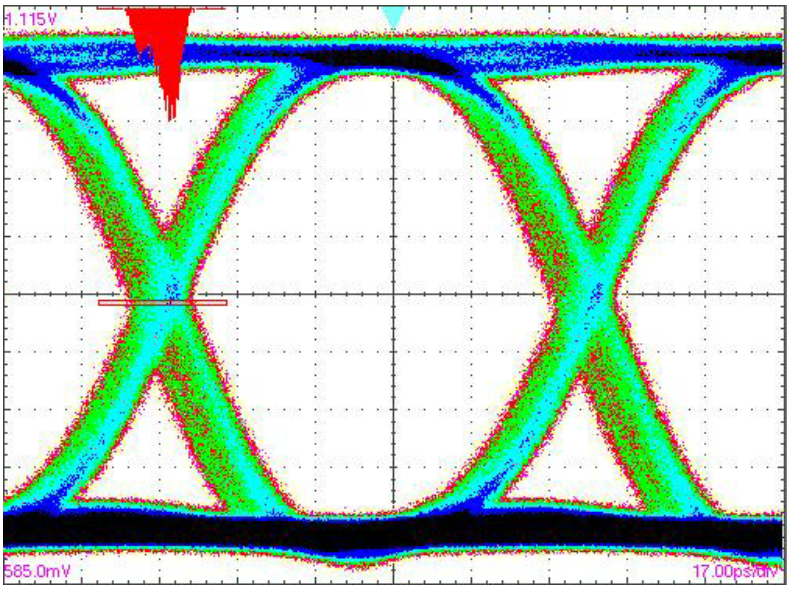


Figure 3. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)



X = 17 ps/DIV, Y = 53 mV/DIV

Figure 4. Eye Diagram at 10.8 Gbps (V_{CC} − V_{EE} = 3.3 V @ 25°C with Input Data Pattern of 2^31−1 PRBS. Total Pk−Pk System Jitter Including Signal Generator is 18 ps. This Data was taken by Acquiring 7000 Waveforms.)

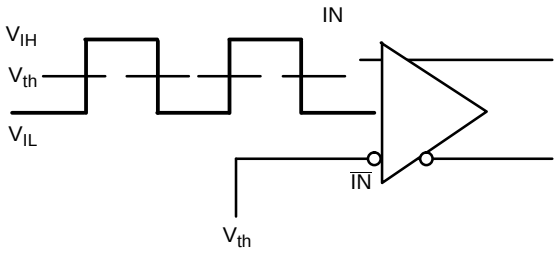


Figure 5. Differential Input Driven Single-Ended

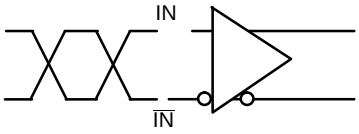


Figure 6. Differential Inputs Driven Differentially

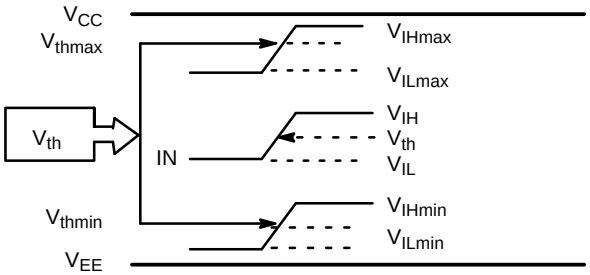


Figure 7. V_{th} Diagram

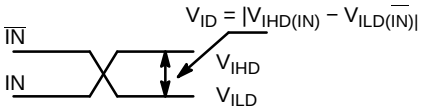


Figure 8. Differential Inputs Driven Differentially

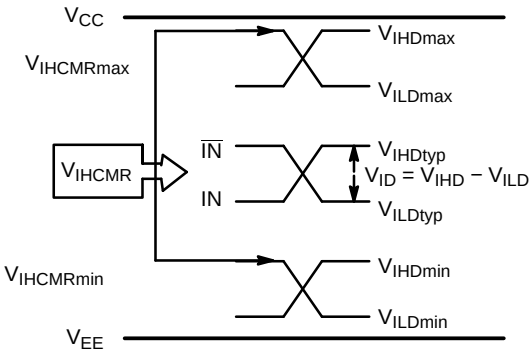


Figure 9. V_{IHCMR} Diagram

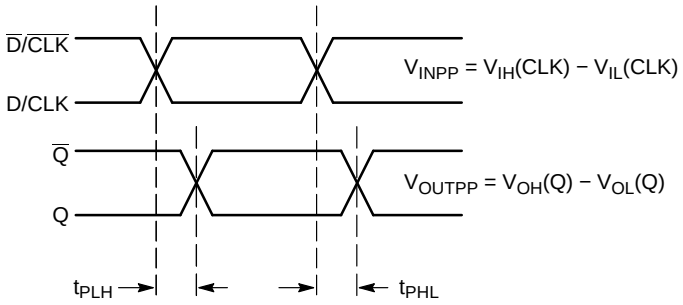


Figure 10. AC Reference Measurement

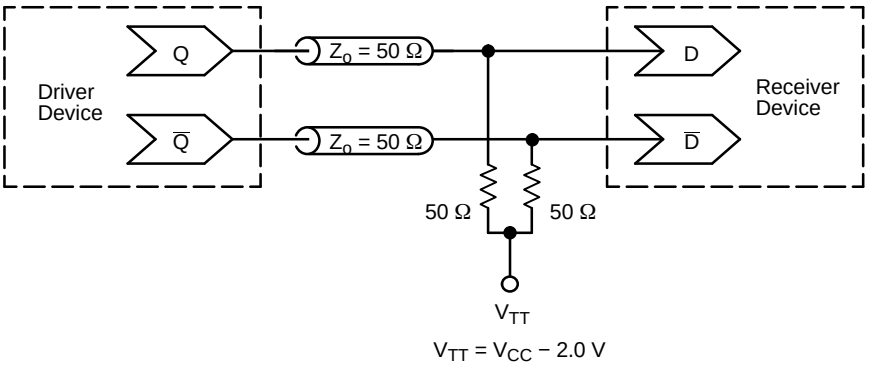


Figure 11. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

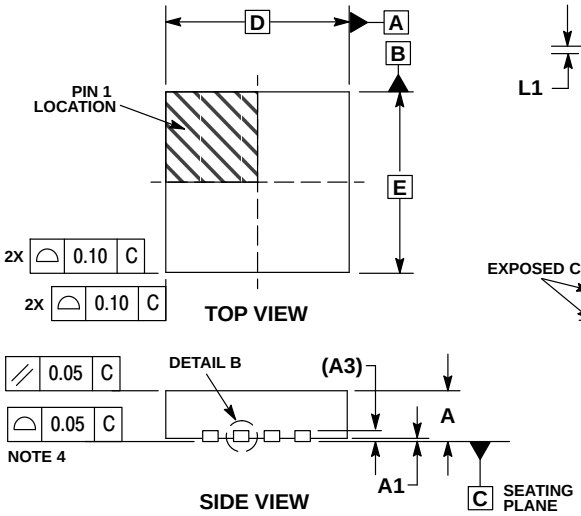
ORDERING INFORMATION

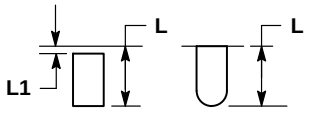
Device	Package	Shipping†
NBSG14MNG	QFN-16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG14MNR2G	QFN-16 (Pb-Free / Halide-Free)	3000 / Tape & Reel
NBSG14MNHTBG	QFN-16 (Pb-Free / Halide-Free)	100 / Tape & Reel

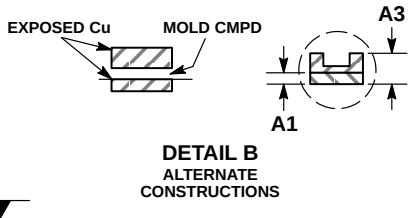
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

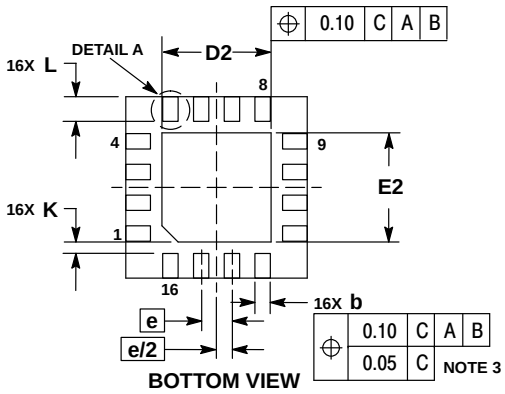




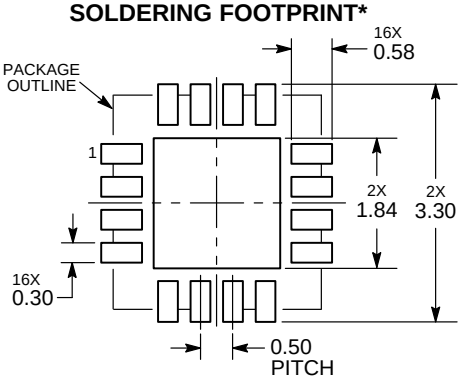


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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