NB100ELT23L

3.3V Dual Differential LVPECL/LVDS to LVTTL Translator

The NB100ELT23L is a dual differential LVPECL/LVDS to LVTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23L makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23L is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the ELT23L does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the NB100ELT23L can accept any standard differential LVPECL/LVDS input referenced from a V_{CC} of +3.3 V.

Features

- 2.1 ns Typical Propagation Delay
- Maximum Operating Frequency > 160 MHz
- 24 mA LVTTL Outputs
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

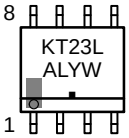
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS*

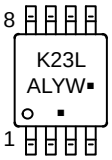


SOIC−8
D SUFFIX
CASE 751





TSSOP−8
DT SUFFIX
CASE 948R



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

© Semiconductor Components Industries, LLC, 2015

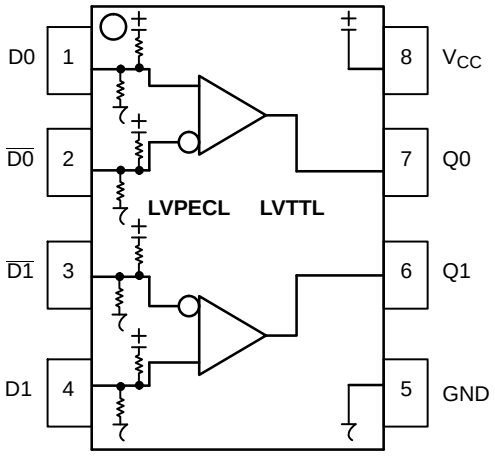


Figure 1. 8−Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	LVTTL Outputs
D0*, D1* $\overline{D0}$**, $\overline{D1}$**	Differential LVPECL Inputs
V_{CC}	Positive Supply
GND	Ground

*Pins will default to $V_{CC}/2$ when left open. If connected to a common termination voltage under no signal conditions, then the device will be susceptible to self−oscillation.

**Pins will default to 2/3 V_{CC} when left open. If connected to a common termination voltage under no signal conditions, then the device will be susceptible to self−oscillation. See AND8020, Section 6 for options.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	D $\overline{D}$	50 kΩ 75 kΩ
Internal Input Pullup Resistor		50 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb−Free Pkg
	SO−8 TSSOP−8	Level 1 Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 1.25 in
Transistor Count		91 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Power Supply	GND = 0 V		3.8	V
V_I	Input Voltage	GND = 0 V	$V_I \le V_{CC}$	3.8	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SO−8 SO−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SO−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	°C/W
T_{sol}	Wave Solder Pb−Free	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. PECL DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0 V (Note 2)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	23	30	10	23	30	10	24	30	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	26	35	15	26	35	15	27	35	mA
V_{IH}	Input HIGH Voltage	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	−150			−150			−150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. All values vary 1:1 with V_{CC}.
3. V_{IHCMR} minimum varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. TTL DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V, T_A = −40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{OS}	Output Short Circuit Current		−180		−50	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 6. AC CHARACTERISTICS V_{CC} = 3.3 V ± 5%, GND = 0.0 V (Note 4)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Frequency	160			160			160			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (Note 5) C_L = 20 pF	1.55	1.9	2.95	1.55	1.9	2.95	1.55	1.9	3.25	ns
t_{SK++} t_{SK--} t_{SKPP}	Output−to−Output Skew++ Output−to−Output Skew− − Part−to−Part Skew (Note 6)			60 25 500			60 25 500			60 25 500	ps
t_{JITTER}	Random Clock Jitter (RMS)		6.0	20		6.0	20		6.0	20	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times C_L = 20 pF (0.8 V to 2.0 V)	700 300	900	1700 1250	700 300	900	1700 1250	700 300	900	1700 1250	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 500 Ω to GND, C_L = 20 pF.
5. Reference (V_{CC} = 3.3 V ± 5%; GND = 0 V).
6. Skews are measured between outputs under identical conditions.

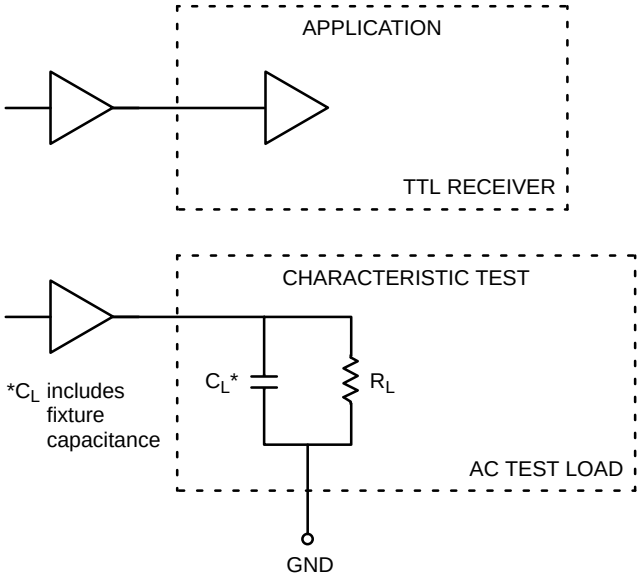


Figure 2. TTL Output Loading Used for Device Evaluation

ORDERING INFORMATION

Device	Package	Shipping†
NB100ELT23LDG	SO−8 (Pb−Free)	98 Units / Rail
NB100ELT23LDR2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NB100ELT23LDTG	TSSOP−8 (Pb−Free)	100 Units / Rail
NB100ELT23LDTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

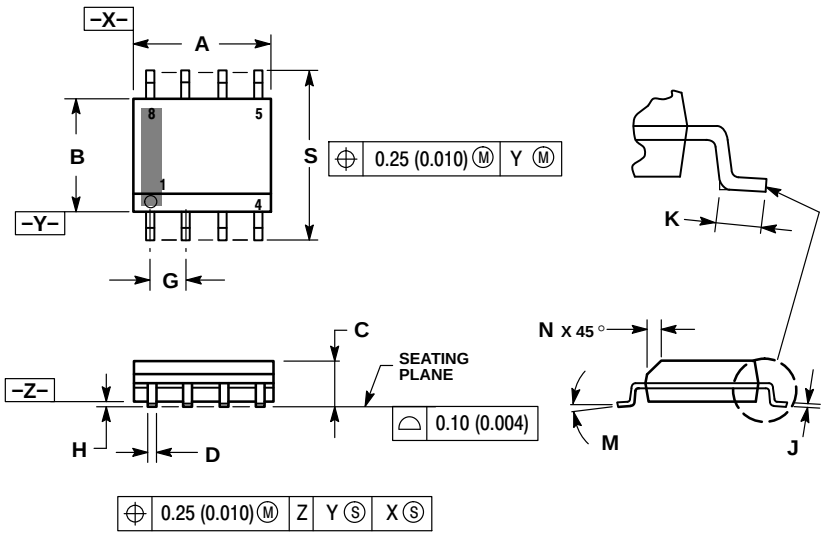
AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

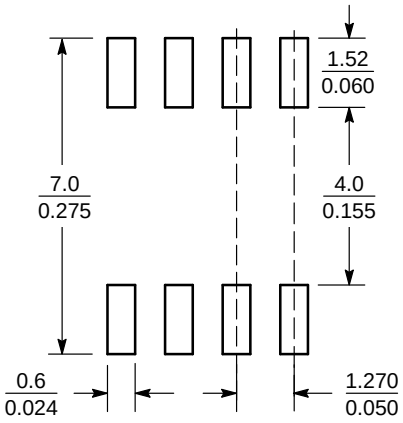
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

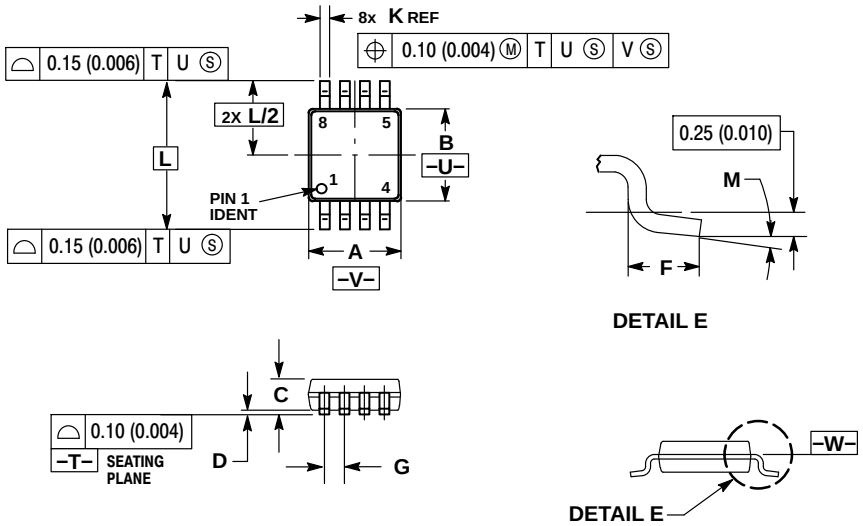


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−8
DT SUFFIX
CASE 948R−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and the ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative