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NAU83P20
20W Stereo Class-D Audio Amplifier

1 Description

The NAU83P20 is single supply, 20W, high efficiency, Class-D audio power stage for driving Stereo bridge-tied speakers. Operating from a single VDD 8V-24V supply, the design includes under-voltage, over-current and over-temperature detection.

NAU83P20 is available in the QFN 48 package.

Key Features

- Class D power 2x20W into 8Ohms (10% THD)
- Typical power efficiency of 90%
- 105dB SNR
- Slew control
- 3V LDO to power PWM controller
- Supports multiple output configurations:
  - 2-CH Bridged outputs (20Wx2)
  - 4-CH single ended outputs (10Wx4)
  - 2-CH single ended + 1-CH bridged (10Wx2 + 20Wx1)
- Fault Detection:
  - Over-Temperature
  - Under-Voltage
  - Over-Current

Applications

- LCD TV's
- TV sound bars
- Car Audio
- Portable Media "Boom Boxes"
- Home entertainment systems

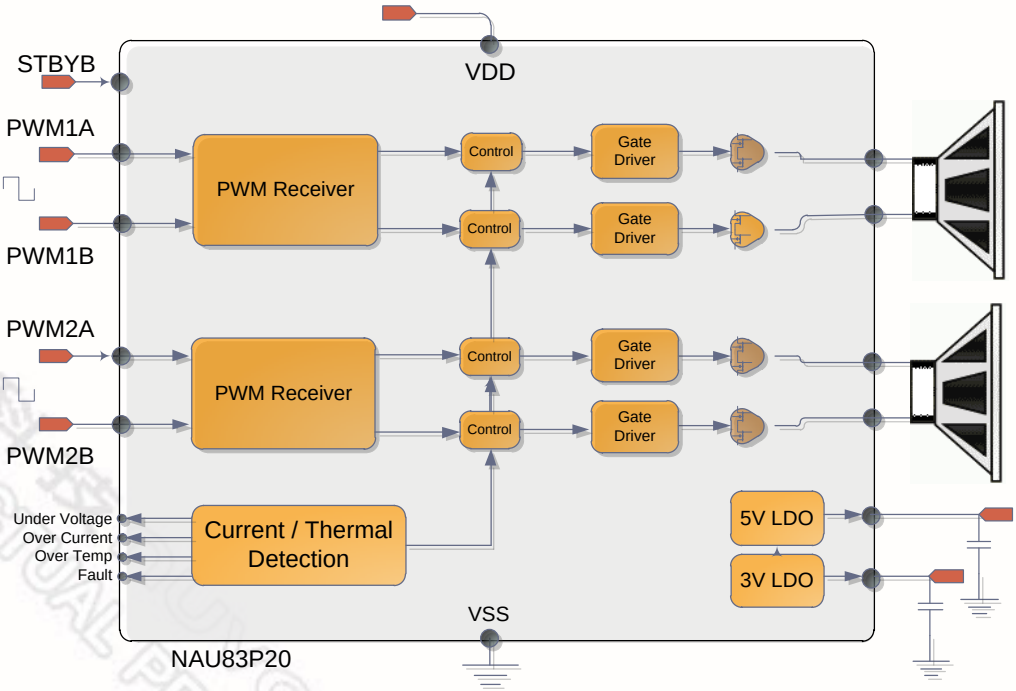
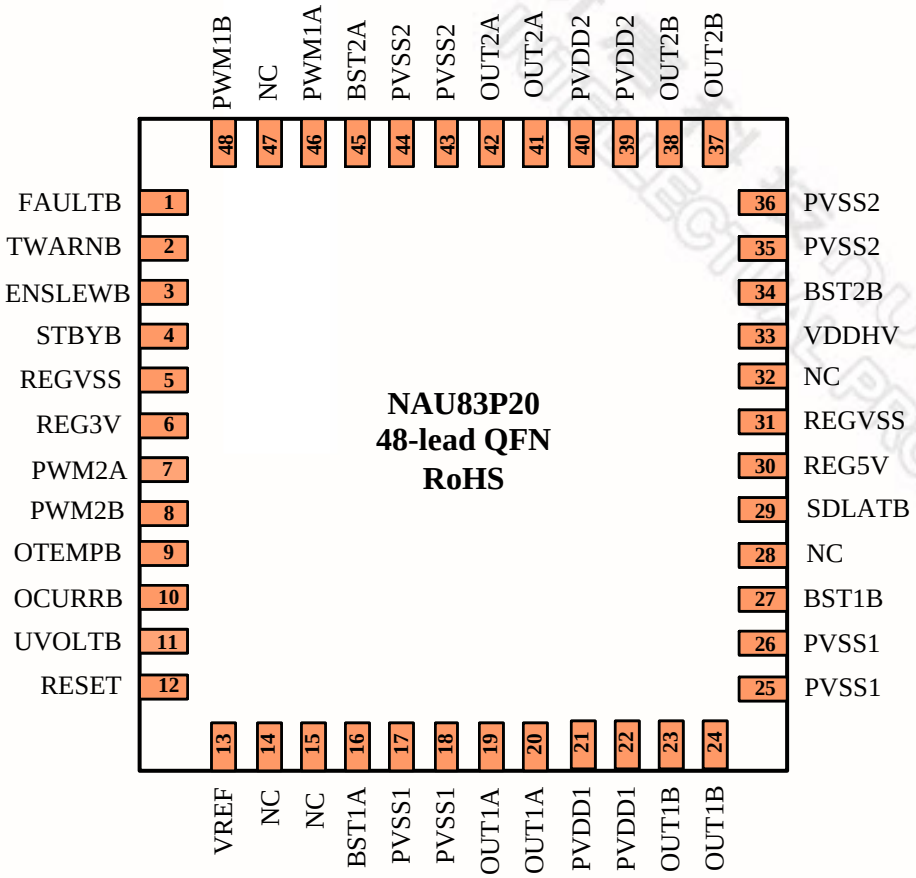


Figure 1: NAU83P20 Block Diagram

2 Pinout



Part Number	Dimension	Package	Package Material
NAU83P20YG	7 x 7 mm	48-QFN	Green

3 Pin Descriptions

Pin #	Name	Type	Functionality
1	FAULTB	Digital Output	Device Error Signal. Active Low if Over current, Under Voltage or Over temperature faults occur.
2	TWARNB	Digital Output	Over Temperature Warning Signal. Active Low if device internal temperature is 120°C
3	ENSLEWB	Digital Input	Enable Slew rate control on the output drivers. Change Slew Rate of PWM Output
4	STBYB	Digital Input	Standby Bar, Disables all 4 PWM Outputs.
5	REGVSS	Supply	3V Regulator Ground
6	REG3V	Supply Output	3V Regulator Supply Output
7	PWM2A	PWM Input	Channel 2A Pulse Width Modulation Signal Input
8	PWM2B	PWM Input	Channel 2B Pulse Width Modulation Signal Input
9	OTEMPB	Digital Output	Over Temperature Fault Signal. Active Low if device internal temperature is 145°C.
10	OCURRB	Digital Output	Over Current Fault Signal. Active Low if current drawn from any of the output drivers is > 6 A.
11	UVOLTB	Digital Output	Under Voltage Fault Signal. Active Low if the supply voltage is under 4.75V.
12	RESET	Digital Input	Reset, Resets SDLATB
13	VREF	I	Internal Reference Voltage
14	N/C	-	No Connect
15	N/C	-	No Connect
16	BST1A	Supply	Channel 1A High Side Bootstrap Supply
17	PVSS1	Supply	Channel 1 Power Ground
18	PVSS1	Supply	Channel 1 Power Ground
19	OUT1A	PWM Output	Channel 1A Pulse Width Modulation Signal Output
20	OUT1A	PWM Output	Channel 1A Pulse Width Modulation Signal Output
21	PVDD1	Supply	Channel 1 Power Supply
22	PVDD1	Supply	Channel 1 Power Supply
23	OUT1B	PWM Output	Channel 1B Pulse Width Modulation Signal Output
24	OUT1B	PWM Output	Channel 1B Pulse Width Modulation Signal Output
25	PVSS1	Supply	Channel 1 Power Ground
26	PVSS1	Supply	Channel 1 Power Ground
27	BST1B	Supply	Channel 1B High Side Bootstrap Supply
28	N/C	-	No Connect
29	SDLATB	Digital Output	Device Shutdown Latch Signal, This signal will latch low, if the Over current fault occurs. This flag is cleared by RESET.
30	REG5V	Supply Output	5V Regulator Supply Output
31	REGVSS	Supply	5V Regulator Ground

32	N/C	-	No Connect
33	VDDHV	Supply	Supply for Regulators
34	BST2B	Supply	Channel 2B High Side Bootstrap Supply
35	PVSS2	Supply	Channel 2 Power Ground
36	PVSS2	Supply	Channel 2 Power Ground
37	OUT2B	PWM Output	Channel 2B Pulse Width Modulation Signal Output
38	OUT2B	PWM Output	Channel 2B Pulse Width Modulation Signal Output
39	PVDD2	Supply	Channel 2 Power Supply
40	PVDD2	Supply	Channel 2 Power Supply
41	OUT2A	PWM Output	Channel 2A Pulse Width Modulation Signal Output
42	OUT2A	PWM Output	Channel 2A Pulse Width Modulation Signal Output
43	PVSS2	Supply	Channel 2 Power Ground
44	PVSS2	Supply	Channel 2 Power Ground
45	BST2A	Supply	Channel 2A High Side Bootstrap Supply
46	PWM1A	PWM Input	Channel 1A Pulse Width Modulation Signal Input
47	N/C	-	No Connect
48	PWM1B	PWM Input	Channel 1B Pulse Width Modulation Signal Input

Table 1: NAU83P20 Pin description

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4 Electrical Characteristics

4.1 AC Characteristics (Bridge Tied Load)

Conditions: PVDDx = 18V, R_{load} = 8 Ohms, Audio Frequency = 1KHz, AES17 filter, F_PWM = 300KHz, Slew disabled, Ambient temp = 25C. NAU82011 are used as input device unless otherwise stated

Parameter	Symbol	Comments/Conditions		Min	Typ	Max	Units
Power Delivered							
Power Output per Channel	P_o	Z_L = 8Ω + 68μH THD + N = 10%	PVDDx = 18V		20		W
			PVDDx = 12V		9		
		Z_L = 8Ω + 68μH THD + N = 1%	PVDDx = 18V		18		
			PVDDx = 12V		8		
Total Harmonic Distortion + Noise	THD+ N	Po=10W (Half Power)	PVDDx = 18V		0.15		%
		Po=4.5W(Half Power)	PVDDx = 12V		0.08		
Output Integrated Noise*	V_n	A-Weighted			50		uVrms
Signal to Noise Ratio*	SNR	A-Weighted			105		dB
Dynamic Range*	DNR	A-Weighted Input=-60dbFS			105		dB
Power Dissipation Due to Idle Losses	P_D	P_o=0W, 4 channels switching			0.6		W

* Using a signal generator with the same input applied to all channels

4.2 AC Characteristics (Single Ended)

Conditions: PVDDx = 18V, R_{load} = 8 Ohms, Audio Frequency = 1KHz, AES17 filter, F_PWM = 300KHz, Ambient temp = 25C NAU82011 are used as input device unless otherwise stated.

Parameter	Symbol	Comments/Conditions		Min	Typ	Max	Units
Power Delivered							
Power Output per Channel	P_o	Z_L = 8Ω + 68μH THD + N = 10%	PVDDx = 18V		10		W
			PVDDx = 12V		4.5		
		Z_L = 8Ω + 68μH THD + N = 1%	PVDDx = 18V		9		
			PVDDx = 12V		4		
Total Harmonic Distortion + Noise	THD+ N	Po=10W (Half Power)	PVDDx = 18V		0.2		%
		Po=4.5W(Half Power)	PVDDx = 12V		0.2		
Output Integrated Noise	V_n	A-Weighted			50		uVrms
Signal to Noise Ratio*	SNR	A-Weighted			105		dB
Dynamic Range*	DNR	A-Weighted Input=-60dbFS			105		dB
Power Dissipation Due to Idle Losses	P_D	P_o=0W, 4 channels switching			0.6		W

*Using a signal generator with the same input applied to all channels

Electrical Characteristics (continued)

4.3 DC Characteristics

Conditions: PVDDX = 18V R_{load} = 8Ohms, F_PWM = 300KHz

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Half-bridge supply	PVDDX		8	18	24	V
Internal Supply for Regulators	VDDHV		8	18	24	V
Quiescent Current Consumption	I_{QUI}	STBYB= 1 Input at 50% duty cycle with output filter		60		mA
		STBYB= 0 Input at 50% duty cycle with output filter		13		mA
I/O Detection						
Under voltage detection limit, falling	V_{uvp}			5.5		V
Under voltage detection limit, rising	V_{uvp}			7		V
Over temperature warning	OTW			125		ºC
Over temperature Error	OTE			150		ºC
Over temperature Hysteresis	OTW_{HYST}			30		ºC
Overcurrent Limit detection	I_{OC}			4.5		A
Overcurrent Response Time	I_{OCT}			1		us
High-level input voltage	V_{IH}	PWM1A/1B/2A/2B, STBY		2		V
Low-level input voltage	V_{IL}			0.8		V
Input leakage Current, High	I_{lkg}	PWM1A/1B/2A/2B, STBY			**100**	uA
Input leakage Current, Low			-10		10	

Conditions: PVDDX = 18v R_{load} = 8Ohms, F_PWM = 300KHz

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Internal Voltage Regulator and Current Consumption						
Regulator output	REG3V			3		V
Supply Current 3 VREG	$I_{(Load)}$	With 100ohm Load: REG3V typ. 3.3V		30		mA
		Standby mode no Switching		6.5		mA

4.4 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply	-0.50	25	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C
Junction temperature range	-40	+150	°C

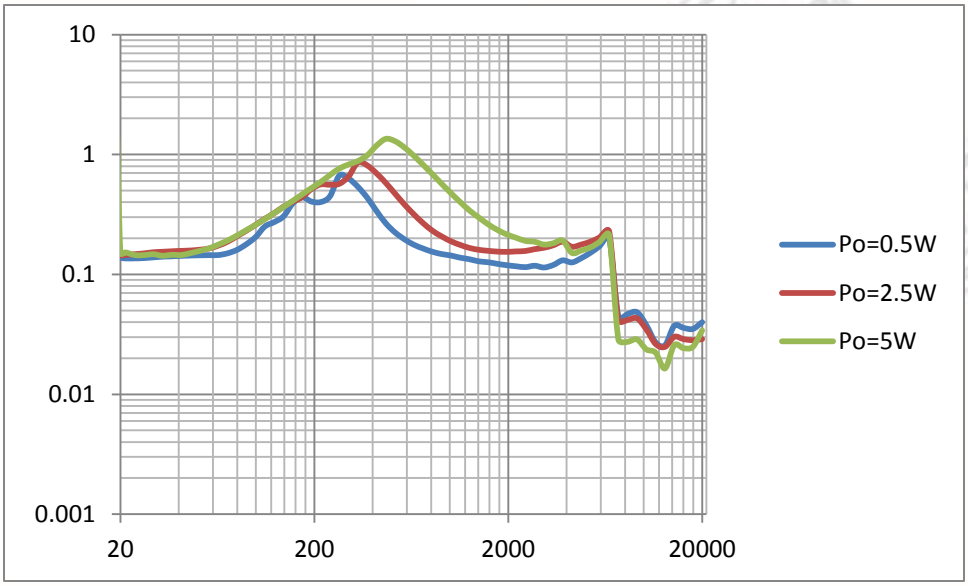
CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

4.5 Recommended Operating Conditions

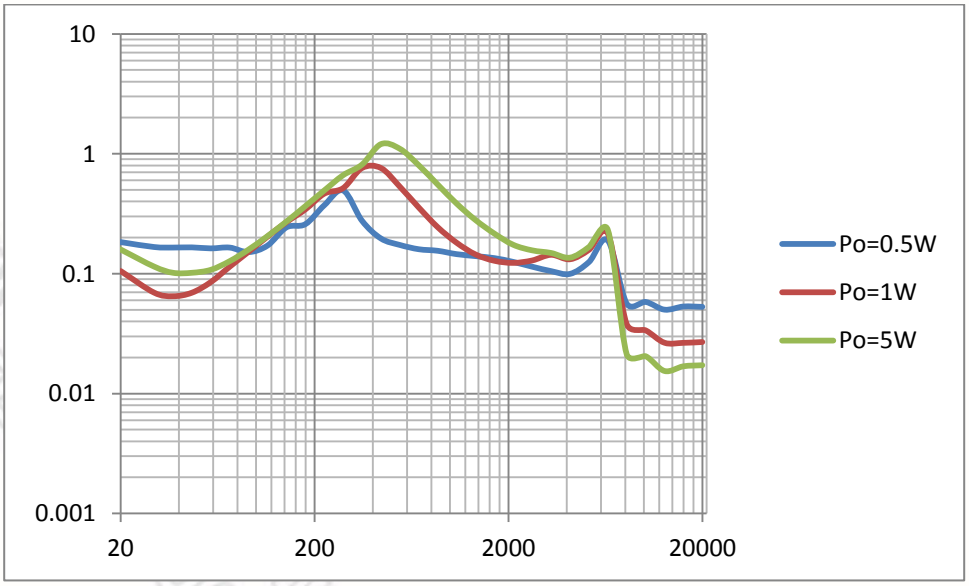
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply range	PVDD1,2	DC supply voltage	8	18	24	V
Digital Input Supply Voltage	REG3V	DC supply voltage	3	3.3	3.6	V
Ground	VSS	DC Ground		0		V
PWM frame rate	F_{pwm}		192	384	432	Khz
Junction Temperature	Tj		0		125	ºC
Load Impedance	RL(BTL)	Output filter: L =10µH, C= 470nF Output AD modulation switching frequency >350Khz		6-8		Ω
	RL(SE)			3-4		Ω
	RL(PBTL)			3-4		Ω
Output Filter inductance	Lo(BTL)	Minimum output inductance under short circuit condition		200		nH
	Lo(SE)			200		nH
	Lo(PBTL)			200		nH

5 Typical Operating Characteristics

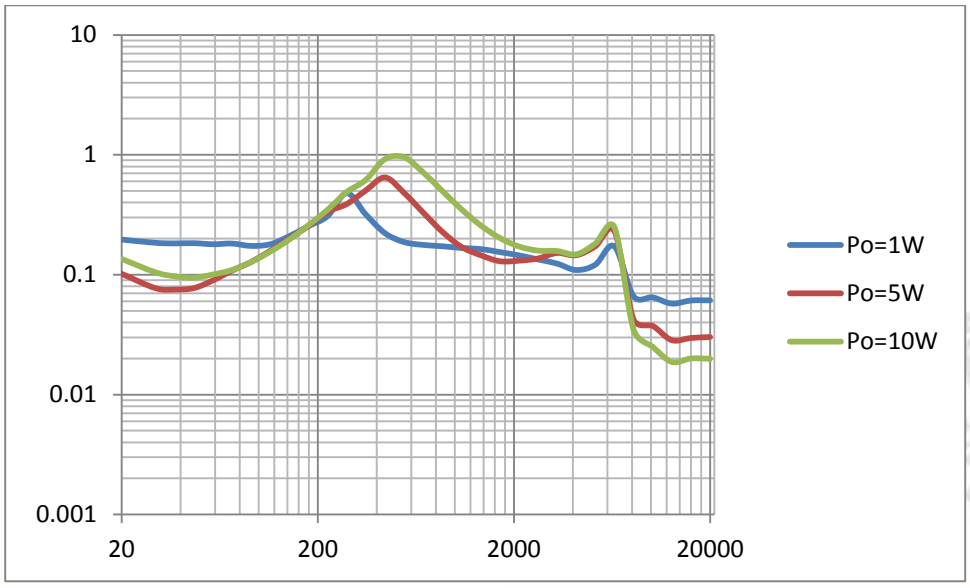
5.1 BTL



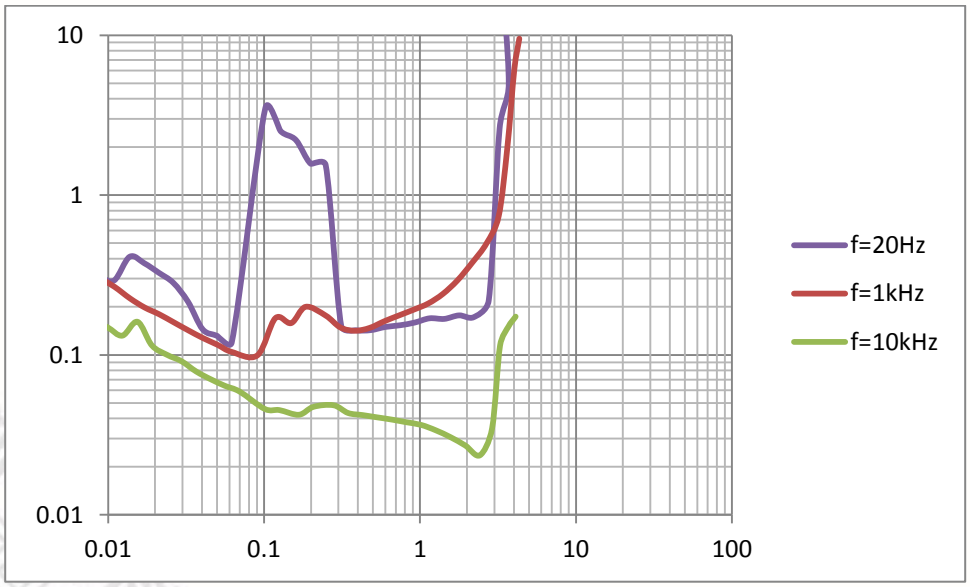
THD+N vs Frequency, Vcc=8V, Rl= 8 BTL



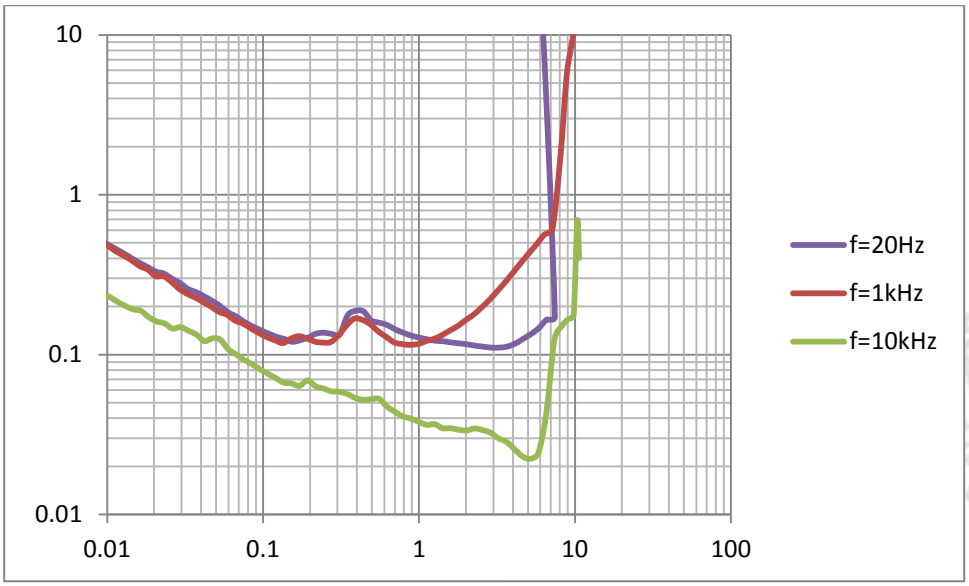
THD+N vs Frequency, Vcc=12V, Rl= 8 BTL



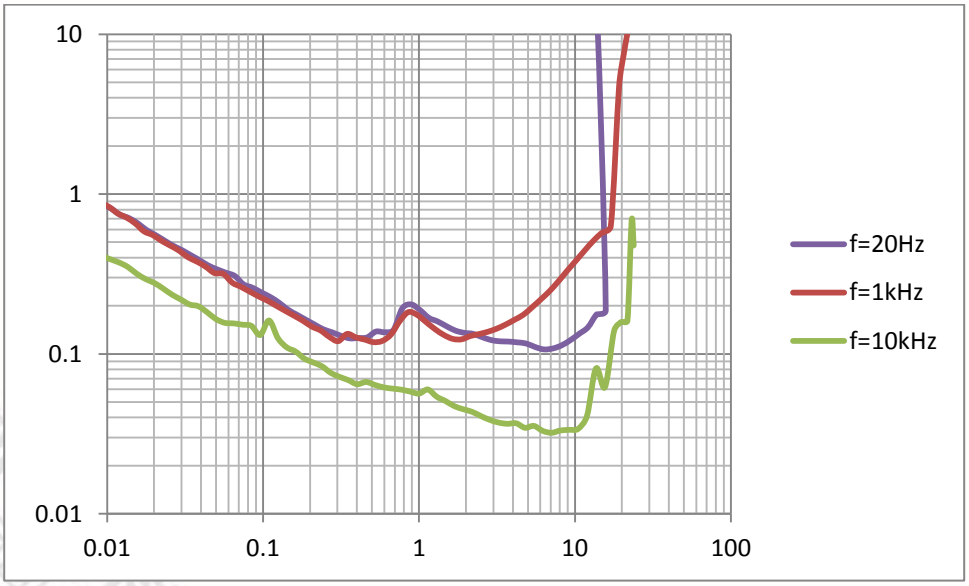
THD+N vs Frequency, Vcc=18V, Rl= 8 BTL



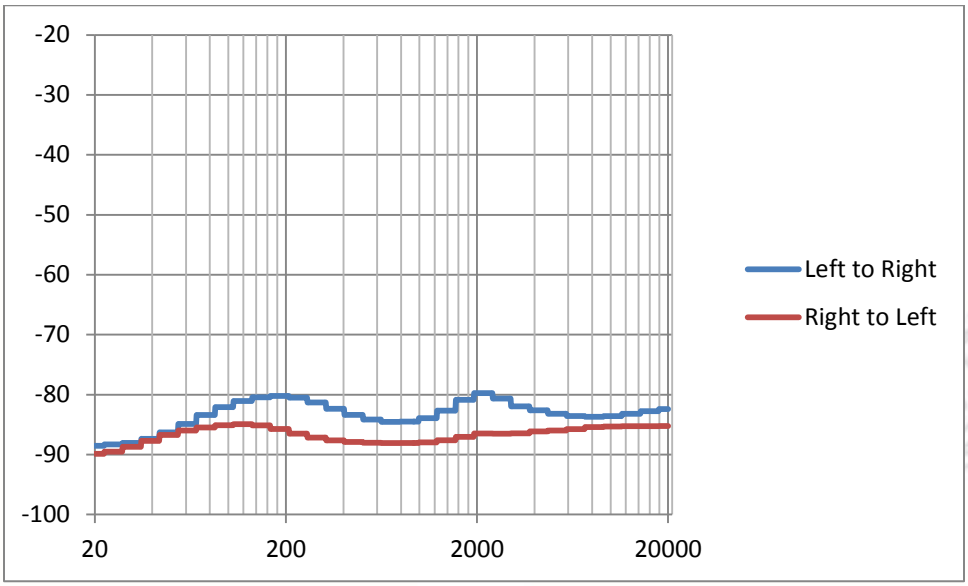
THD+N vs Output Power Vcc=8V, Rl= 8 BTL



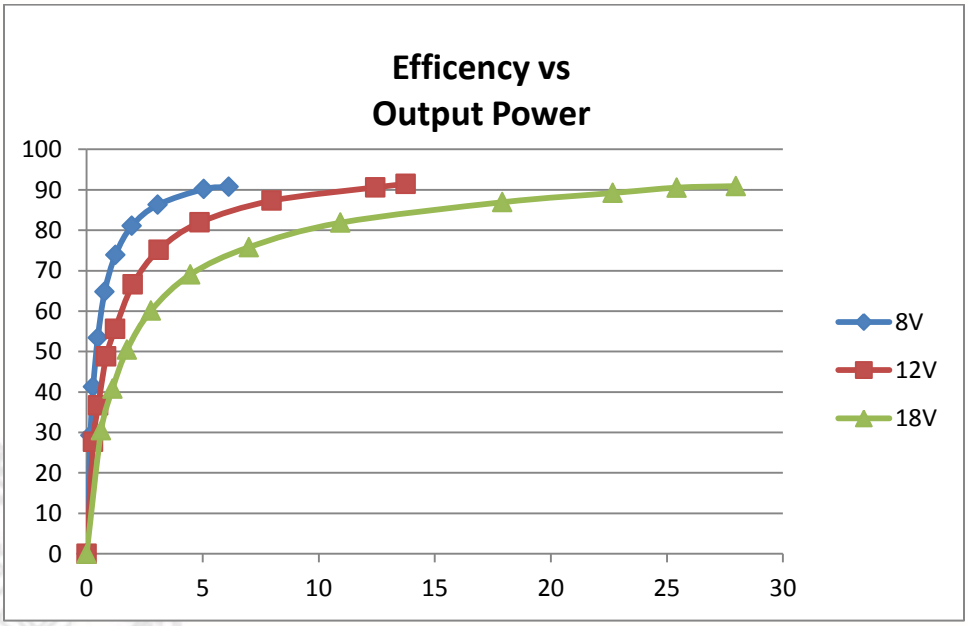
THD+N vs Output Power Vcc=12V, Rl= 8 BTL



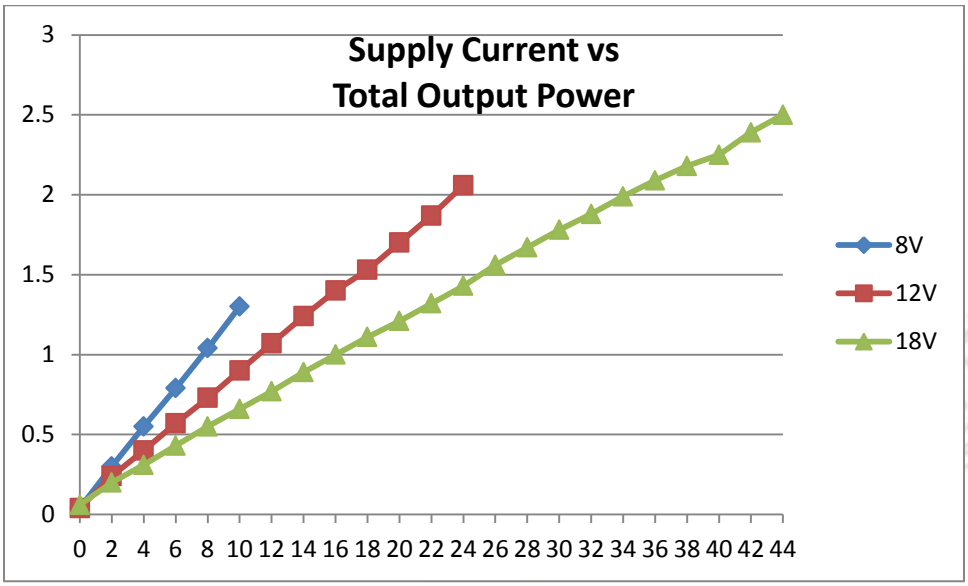
THD+N vs Output Power Vcc=8V, Rl= 8 BTL



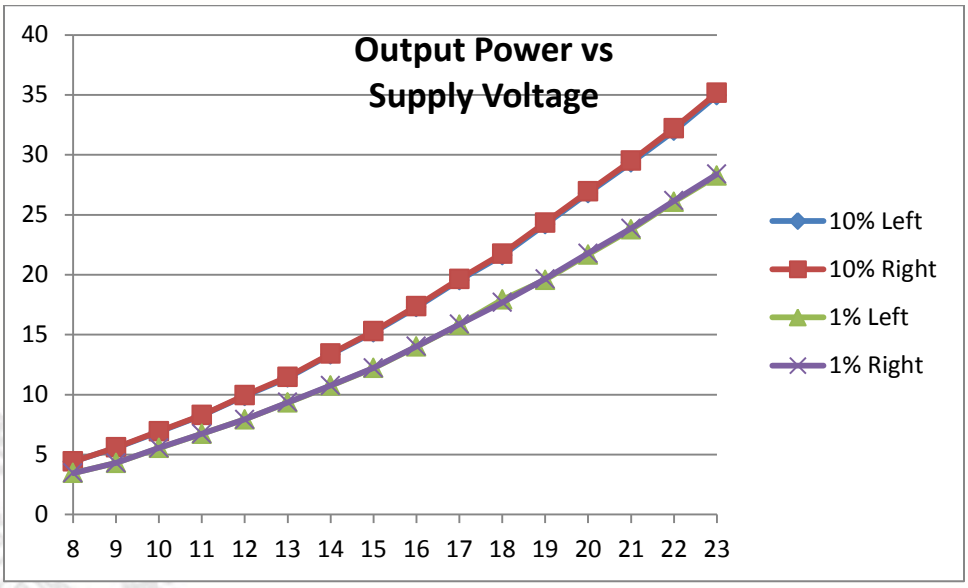
Crosstalk vs Frequency Vcc=18V Rl=4 Po=0.25W SE



F=1kHz Rl=8 BTL



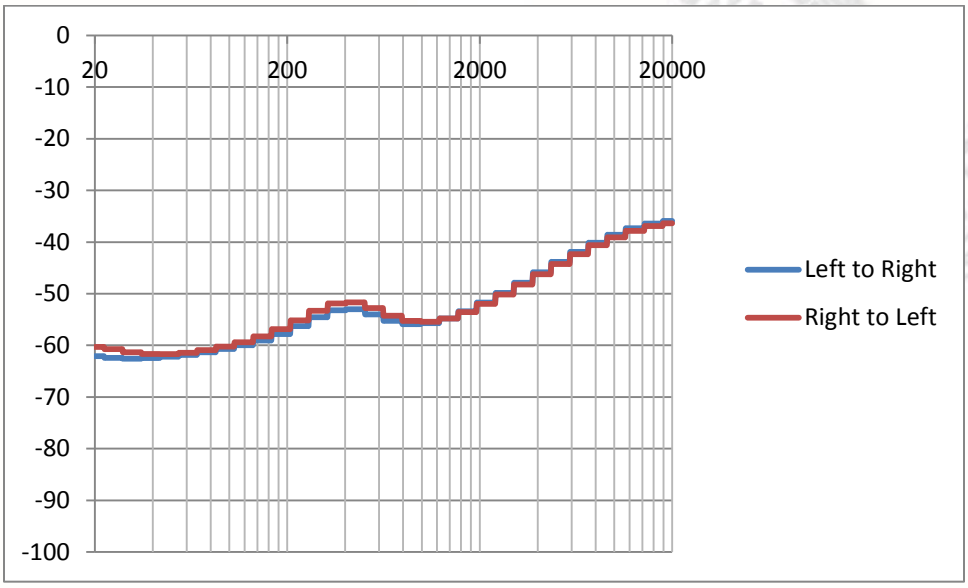
F=1kHz Rl=8 BTL



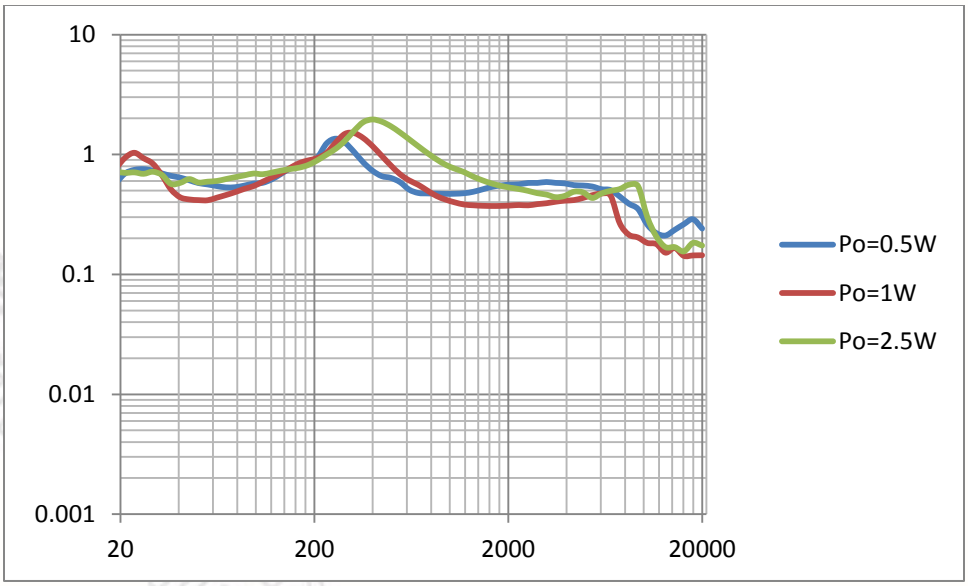
F=1kHz Rl=8 SE

6 Typical Operating Characteristics

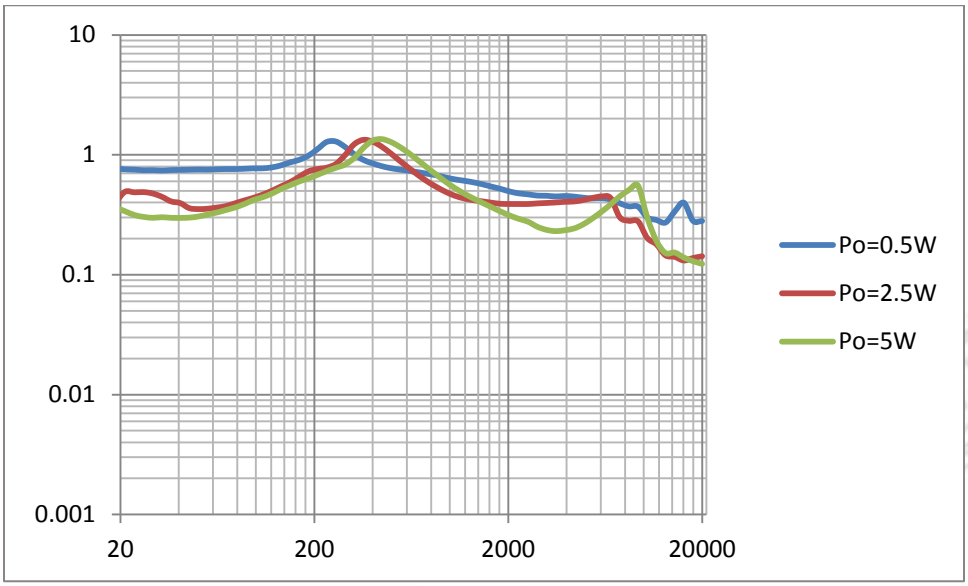
6.1 SE



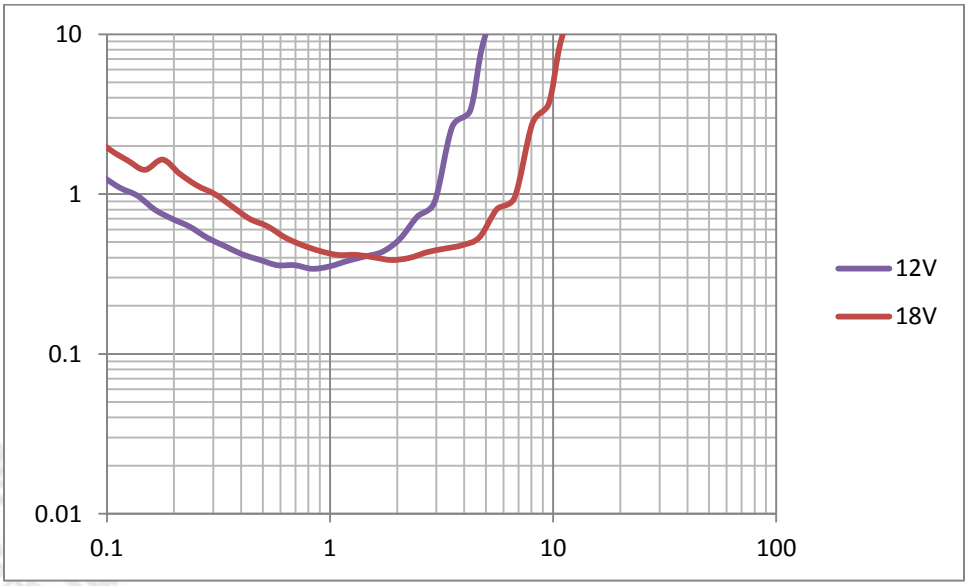
Crosstalk vs Frequency, Vcc=18V Rl=4 Po=0.25W SE



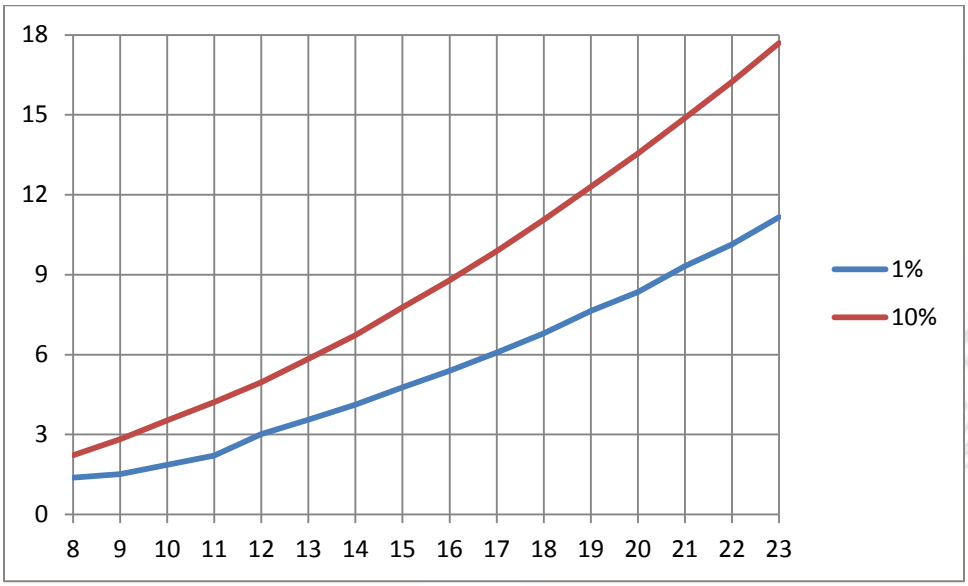
THD+N vs Frequency, Vcc=12V Rl=4 SE



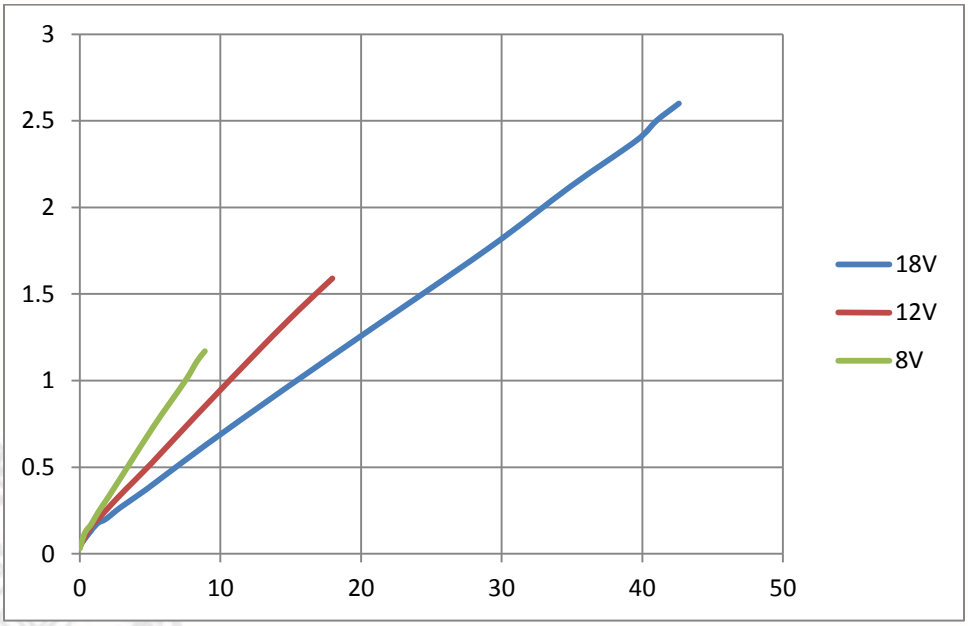
THD+N vs Frequency, Vcc=18V Rl=4 SE



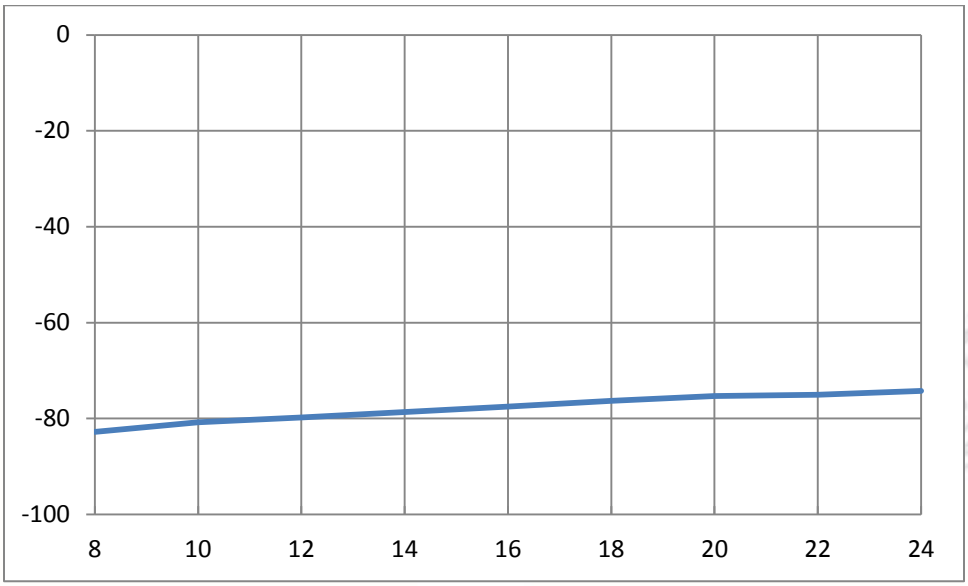
THD+N vs Output Power, F=1kHz Rl=4 SE



Output Power vs Supply Voltage , F=1kHz Rl=8 SE



Supply Current vs Output Power, F=1kHz Rl=4 SE



A-Weighted Noise vs Supply Voltage, F=1kHz Rl=4 SE

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7 Special Feature Description

The NAU83P20, in addition to high efficiency, also provides the following protection features.

7.1 Device Fault Detection

The NAU83P20 includes device fault detection for three operating scenarios. They are

1. Thermal Overload
2. Short circuit
3. Supply under voltage

7.1.1 Thermal Overload Detection

When the device internal junction temperature reaches 125°C, the NAU83P20 will force the TWARNB digital output low. If the temperature continues to rise to 150°C, the NAU83P20 will force the OTEMPB digital output low. When the device cools down and a safe operating temperature of 125°C has been reached, the TWARNB and OTEMPB digital outputs will return to their default states, high.

7.1.2 Short Circuit Detection

If a short circuit condition is detected on any of the output drivers the NAU83P20 will force the OCURRB digital output low. The OCURRB digital output will remain low until the short circuit condition has been removed. The short circuit threshold is 4.5A.

7.1.3 Supply under Voltage Detection

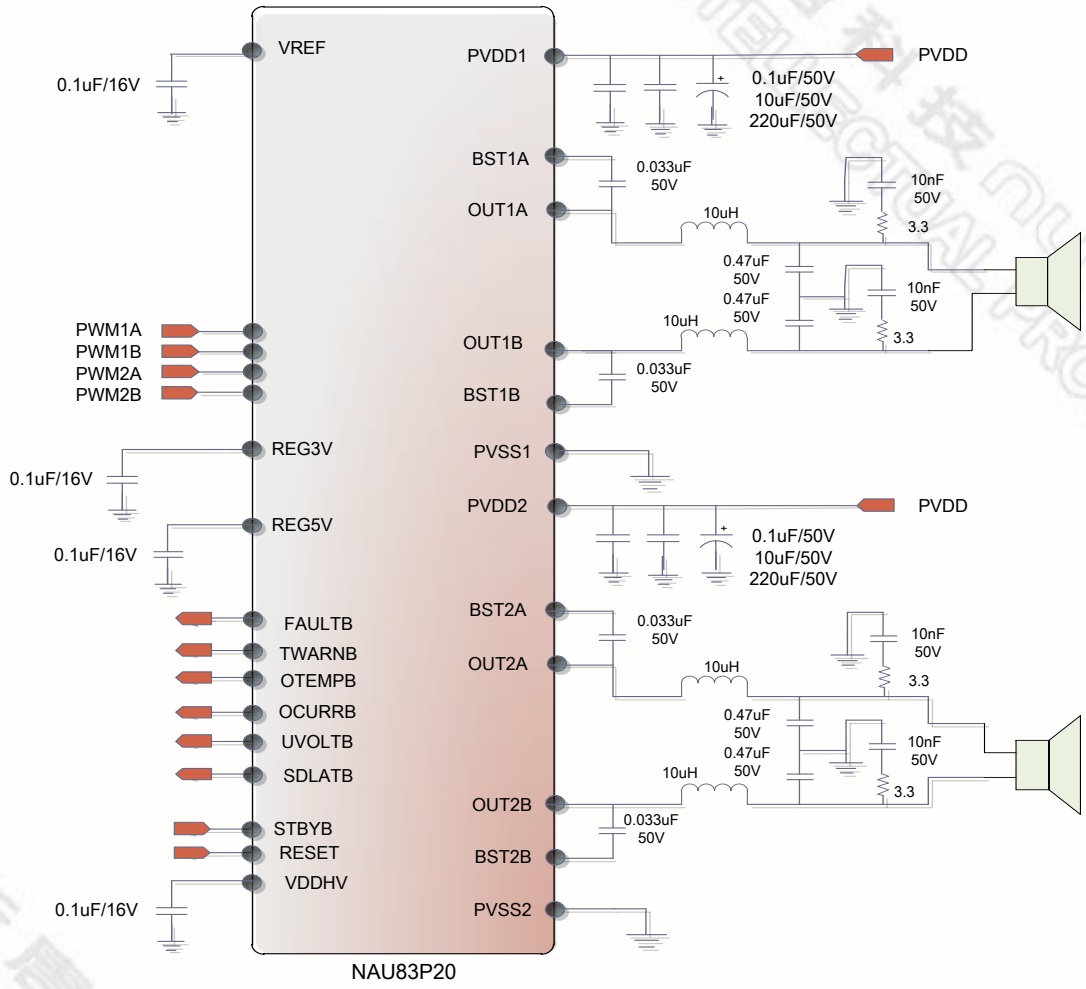
If the supply voltage drops under 5.5 V, the NAU83P20 will force the UVOLTB digital output low. UVOLTB digital output will remain low until the supply voltage returns to a level > 7V.

7.2 Power up and Power down Control

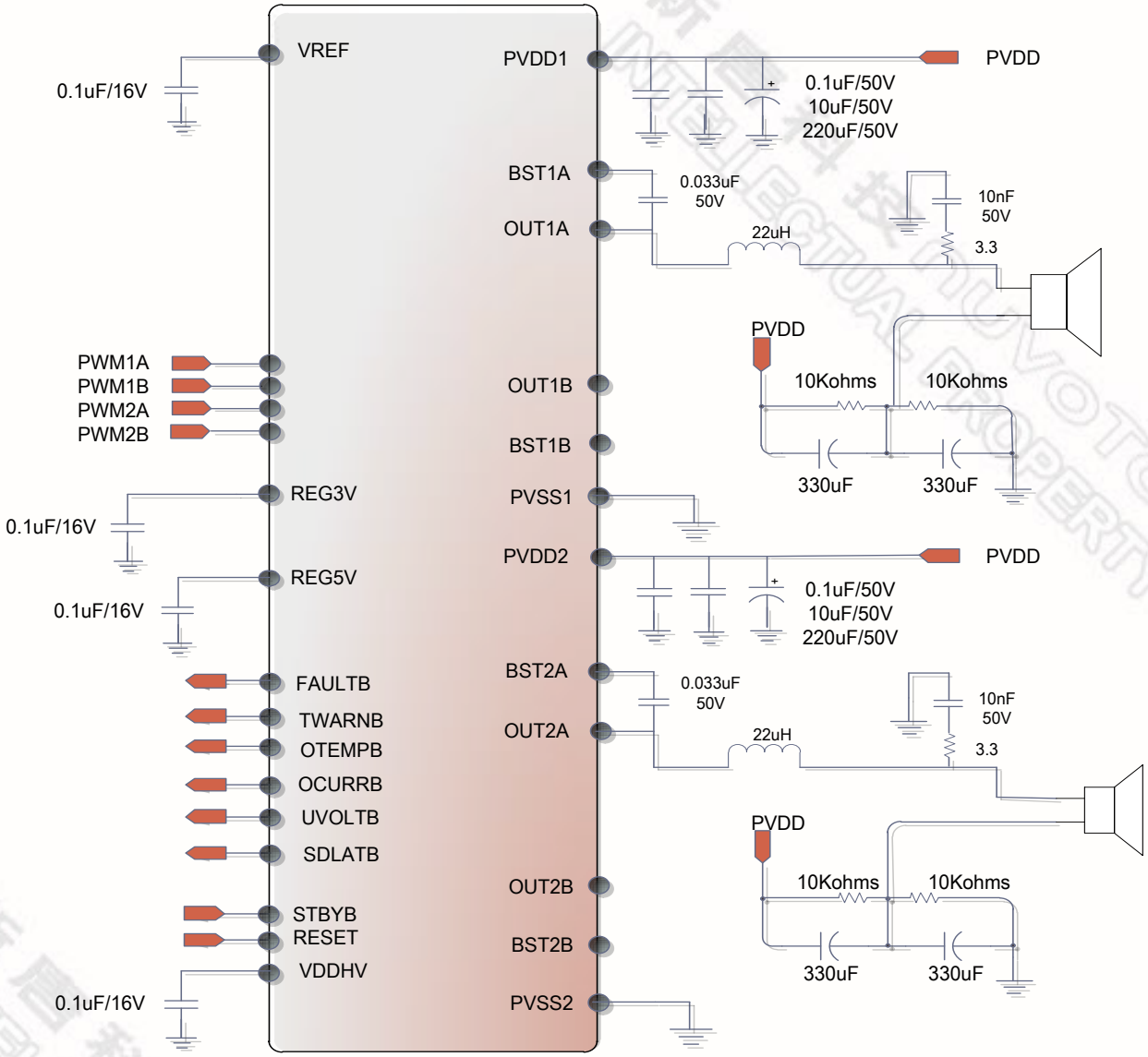
When the PVDD supply voltage ramps up, the 3V and the 5V LDOs also power up. The STBYB pin only controls the operation of the 4 half bridge drivers. When STBYB is low, the 4 half bridge drivers are in the high impedance state. STBYB is high, enables the 4 half bridge drivers. The recommended power up sequence is to hold the STBYB pin low, apply the PVDD supply, wait until the 3V and 5V LDO's are stable, apply STBYB=1 and then start driving the PWM input signals.

8 Application Information

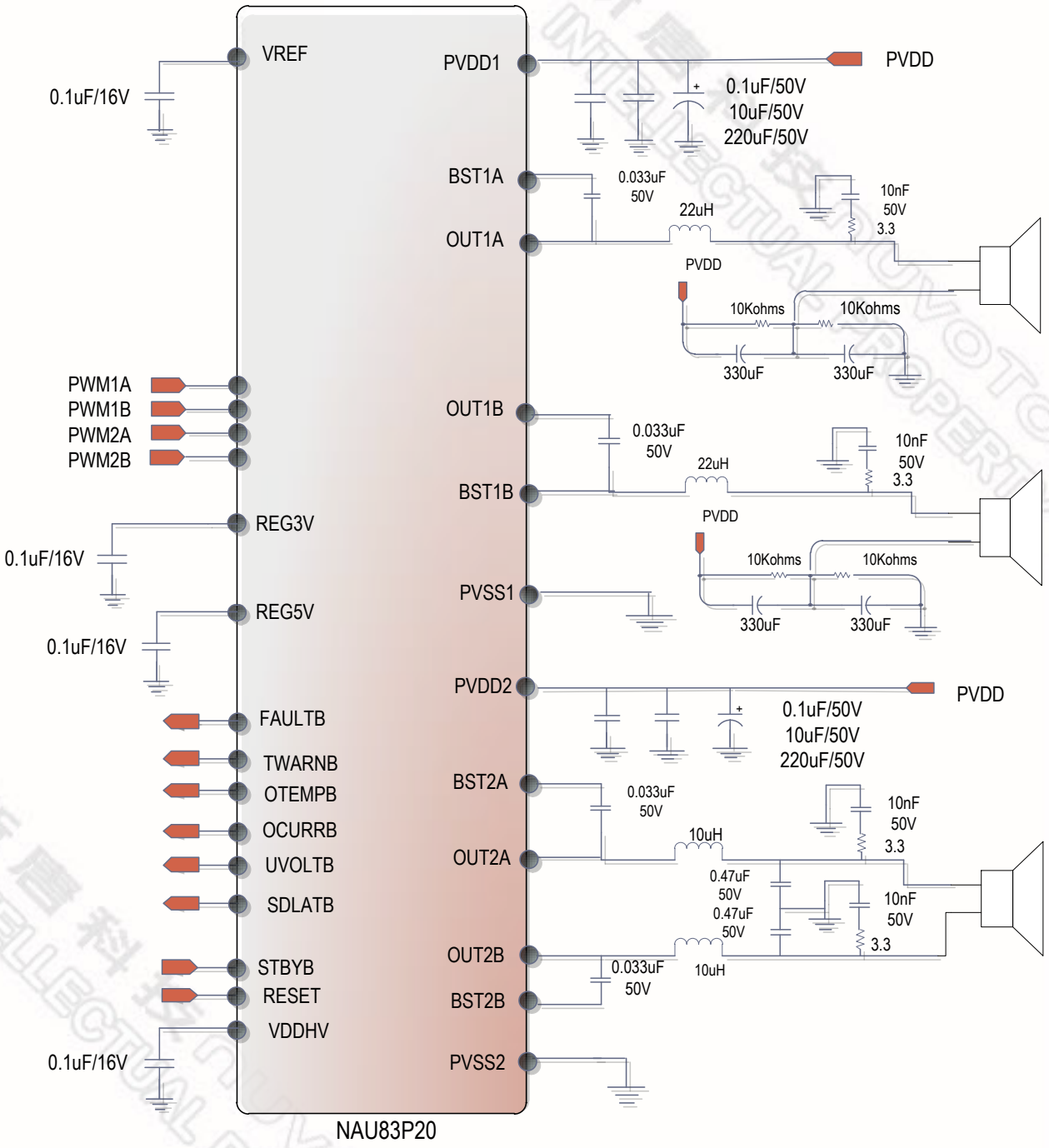
Differential BTL Application with Modulation Filters



Single Ended Application with Modulation Filters



Sub-Woofer Application with Modulation Filters



8.1 Component Selection

8.1.1 Bypass Capacitors

Bypass capacitors are required to remove the ac ripple on the PVDDx pins. The value of these capacitors depends on the length of the PVDDx trace. In most cases, 10uF and 0.1uF are sufficient to ensure optimum performance. In addition, 220uF capacitors should be added to remove the additional ripple on the high current PVDDx inputs.

8.1.2 Bootstrap Circuit (BSTxx)

In order for the bootstrap circuit to function correctly, a ceramic capacitor must be added between BSTx and OUTx. In applications with PWM switching frequencies of 300kHz a 0.22uF capacitor is recommended. If the application involves a higher or lower PWM switching frequency, the capacitor size may need to be decreased or increased respectively.

8.1.3 3V and 5V LDOs

In order for the internal regulators to function more efficiently, a 0.1uF capacitor needs to be placed between the REG3V, REG5V pins and ground.

8.2 Layout considerations

Good PCB layout and grounding techniques are essential to get the good audio performance. It is recommended to use low resistance traces for the outputs as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

9 Operation

9.1 Power Supplies

The NAU83P20 requires one 8-24V supply in order to operate. The boost voltage supplies required by the high-side gate driver is realized by mostly built-in circuitry requiring only a few external capacitors. The power supply should be low output impedance and low noise.

In order to provide high quality electrical and audio characteristics the output stages are identical but independent half-bridges. Each half-bridge has separate bootstrap power supply pin and voltage regulator for efficient gate drive operation. The supply for the common logic circuits is derived from internal voltage regulators, which translate the VDDHV pin supply, allowing for single supply operation.

In order for the bootstrap circuit to function correctly, a ceramic capacitor is added between the BSTxx and the OUTxx pins. When the output of the power stage is low, the capacitor is charged and when the output is high, the capacitor potential is shifted above the output potential providing a full rail to rail output. Refer to Section 7 for recommended capacitor values.

9.2 System Power Up and Power Down Sequence

9.2.1 Power Up

It is recommended that the STBYB be held low to tri-state the output drivers until the PVDDx voltage rises above the under voltage detection threshold of 7V. Holding STBYB in a low state while powering up also helps to ensure that the bootstrap capacitors are fully charged before the chip begins operation.

9.2.2 Recommended Power up Sequence

1. With PVDDx Low
2. Hold STBYB LOW
3. Apply Power to PVDDx
4. Wait 10ms for the chip to power up
5. Apply input modulation signal at 50% duty cycle
6. Hold STBYB HIGH
7. The device will begin to modulate

9.2.3 Power Down

The device will remain fully powered on as long as PVDDx remain above the under voltage detection threshold. It is recommended to hold STBY low during power down; this will prevent clicks and pops.

9.2.4 Recommended Power down Sequence

1. With STBYB and PVDDx High
2. Hold STBYB Low tri-stating the drivers
3. Wait 10ms while the drivers tri-state
4. Remove all input signals
5. Remove power from PVDDx

9.3 Error Reporting

The FAULTB pin is an active-low, open-drain output. The over temperature, over current, and under voltage pins are active-low, open-drain outputs. The function of these pins is to report errors in the chip to the PWM controller, micro controller, or other system control device.

Pin	Causes
FAULTB (FAULTB= 0)	Any low transition on OTEMPB, OCRURB, UVOLTB
OTEMPB (FAULTB= 1)	Device junction temperature above 145°C
OCURRB (FAULTB)	The Current limit is set at 4.5A
UVOLTB (FAULTB=1)	PVDDx has fallen below the minimal 5.5V required for chip operation

9.4 Device Exception Handling System

The NAU83P20 has several error reporting signals used for device fault detection. The system has been designed so that it can be easily integrated into a system that will be able to adjust operating parameters in order to allow the device to operate within its specified limits.

There are six signals related to the exception handling system, which are output to device pins:

1. Fault (FAULTB)
2. Temperature Warning (TWARNB)
3. Over Temperature (OTEMPB)
4. Over Current (OCURRB)
5. Under Voltage (UVOLTB)
6. Shutdown Latch (SDLATB)

All 6 signal pins are open drain, active low outputs.

9.4.1 Device Standby and Reset

The STBYB pin controls the half-bridges. Setting STBYB low forces the half-bridges into a high impedance state. The device will also be in a low current state. The STBYB pin can also be used for hard muting the power stage.

For stand-alone fault protection, it is possible to tie the FAULTB pin to STBYB. In this configuration any fault detection reported by the FAULTB pin going low will force STBYB low, therefore, minimizing any possible damage to the device from over-current or over-temperature issues.

In BTL modes driving the STBYB pin low will enable weak pull down of the half-bridge circuits causing the bootstrap capacitors to charge.

RESET pin resets the SDLATB pin.

9.4.2 Thermal Information

The QFN-48 package is intended to be interfaced with an exposed heat-sink pad on the underside of the PCB. This can be accomplished by passing plugged thermal vias from pin 49 (exposed pad) of the package through all of the PCB layers to an exposed metal layer on the opposite side. If additional thermal management is required, a heat sink can be attached to this exposed metal layer allowing for additional heat dissipation.

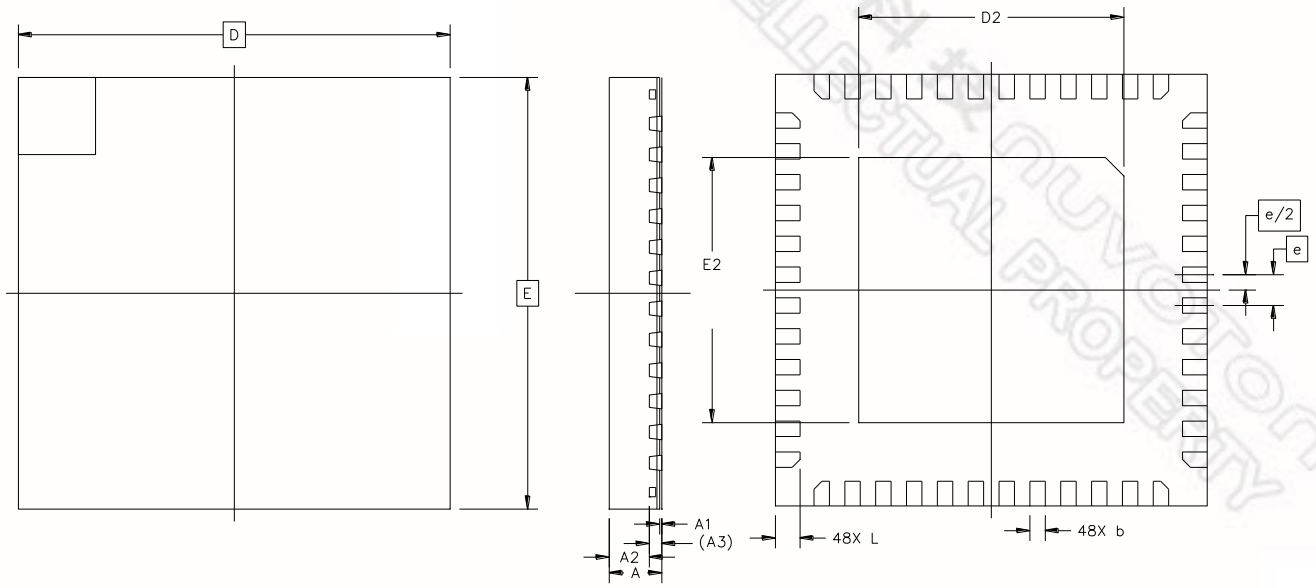
9.4.3 Slew Rate Configuration

The ENSLEWB pin is used to change the slew rate of the output drivers. There are 2 settings:

1. ENSLEWB **=** 0 (Default) : Output Driver Slew rate **=** 5ns
2. ENBSLEWB **=** 1 : Output Driver Slew rate = 2ns

10 Package Dimensions

48-lead plastic QFN 48L; 7X7mm^2, 0.8mm thickness, 0.5mm lead pitch



COPLANARITY	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0.00	0.04	0.05
MOLD THICKNESS	A2	---	0.65	0.67
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.20	0.25	0.30
BODY SIZE	D	7.0 BSC		
	E	7.0 BSC		
LEAD PITCH	e	0.5 BSC		
LEAD LENGTH	L	0.30	0.40	0.50
PACKAGE EDGE TOLERANCE	aaa	0.10		
MOLD FLATNESS	bbb	0.10		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.10		
EXPOSED PAD OFFSET	eee	0.10		

11 Ordering Information

Nuvoton Part Number Description

NAU83P20YG

Package Material:

G=Green Package

Package Type:

Y = QFN package

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Version History

VERSION	DATE	PAGE	DESCRIPTION
NAU83P20 Datasheet Rev1.0	Jan., 2013	NA	Revision1.0
NAU83P20 Datasheet Rev1.1	April, 2013	1, 2, 3,4, 10 12 15 16	Change block diagram Input labels to PWM## Update Single Chip Pin-out Diagram Update Single Chip Pin description Change Fault Protection to Fault Detection and update action description. Remove OC_ADJ and STTIMER descriptions. These are not available. Update Package drawing to QFN48 Saw Type. Change Pkg type designator to Y = QFN
NAU83P20 Datasheet Rev1.3	Oct., 2013	2 7 12 14 All	Package material changed from Pb-free to Green Remove Over Current Resistor Update Signal Ended configuration circuit Updated recommended power up/down sequence
NAU83P20 Datasheet Rev1.4	August,25,14	All	AC/DC parameters were updated, Changed pin-out by deleting a test pin. Made changes to Application diagrams.
Rev 1.6	Oct, 14, 2014	All	Updated application diagrams, added table contents
Rev 1.7	Oct, 24, 2014	10-18	Updated Performance Graphs
Rev1.8	January 21,2015	26	Updates package information.

Table 1: Version History

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

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