DATA SHEET

74F1245
Octal transceiver (3-State)

Product specification

IC15 Data Handbook

1995 Mar 01

Philips Semiconductors

PHILIPS

Octal transceiver (3-State) 74F1245

FEATURES

- Same function and pinout as 74F245
- High impedance NPN base inputs for reduced loading (70µA in Low and High states)
- Useful in applications where light loading bus loading or direct interface with output of a MOS microprocessor is desired
- Octal bidirectional bus interface
- Glitch free during 3-State power up and power down
- 3-State buffer outputs sink 64mA and source 15mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	5.0ns	115mA

DESCRIPTION

The 74F1245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive (T/$\overline{R}$) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

ORDERING INFORMATION

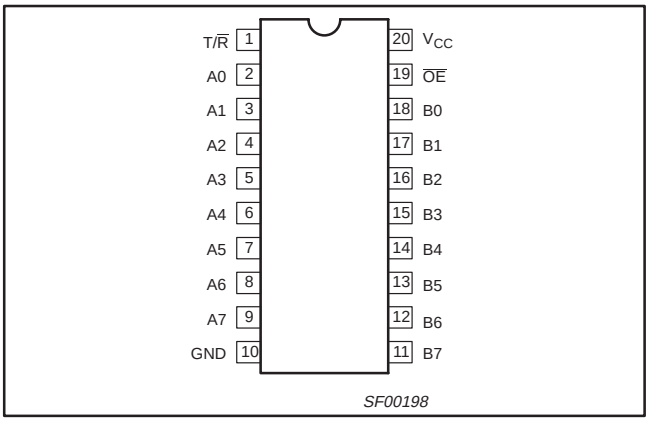
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-Pin Plastic DIP	N74F1245N	SOT146-1
20-Pin Plastic SOL	N74F1245D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

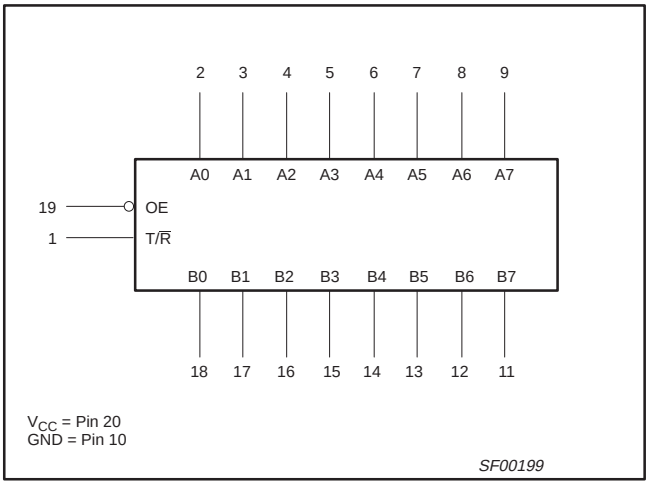
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7, B0–B7	A and B port inputs	3.5/0.117	70µA/70µA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.033	40µA/20µA
T/$\overline{R}$	Transmit/Receive input	2.0/0.033	40µA/20µA
A0–A7	A port outputs	150/40	3.0mA/24mA
B0–B7	B port outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

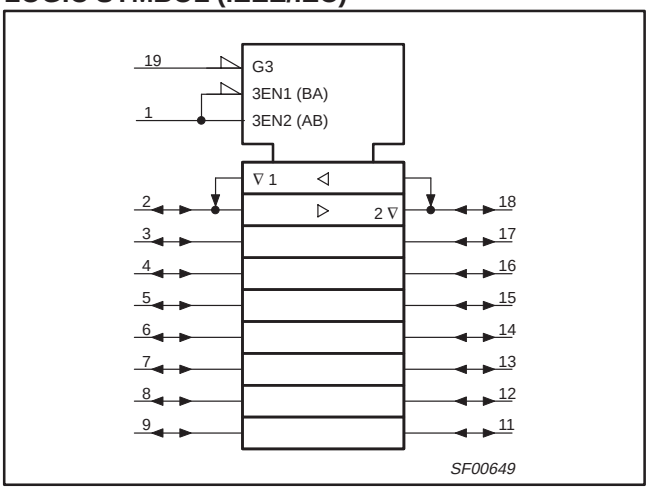
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

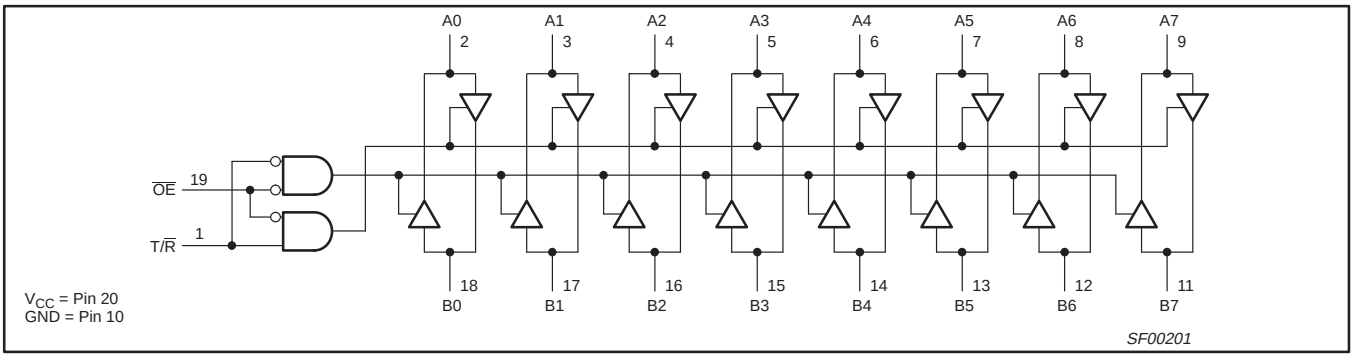


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	An	Bn
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0–A7			–3	mA
		B0–B7			–15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage	A0–A7, B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10% V_{CC}		0.30	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 0.0V, V_I = 5.5V					100	µA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short-circuit output current[NO TAG]	A0–A7	V_{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	155	mA
		I_{CCL}					116	150	mA
		I_{CCZ}					110	165	mA

NOTES:

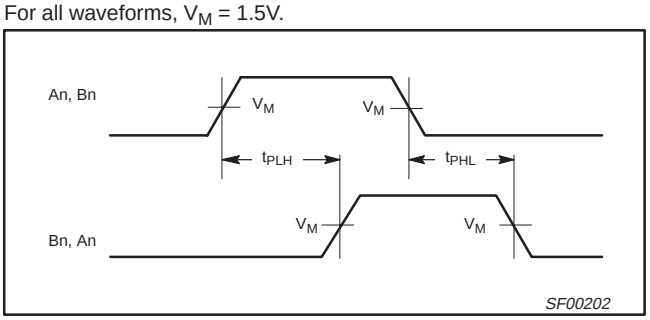
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

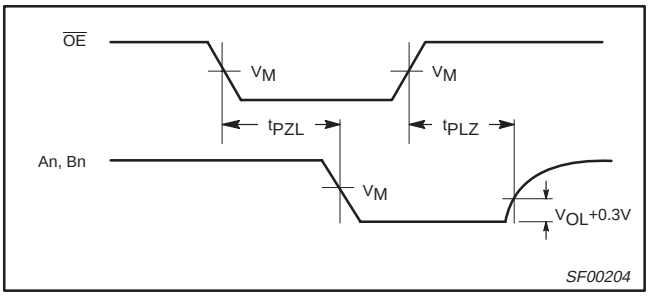
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform NO TAG	2.0 2.5	4.0 5.0	6.5 7.5	1.5 2.0	7.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to An or Bn	Waveform NO TAG Waveform NO TAG	3.0 4.0	6.0 7.5	8.0 10.0	2.5 3.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to An or Bn	Waveform NO TAG Waveform NO TAG	2.0 4.0	5.0 7.0	8.0 10.0	1.5 4.0	9.0 11.0	ns

AC WAVEFORMS

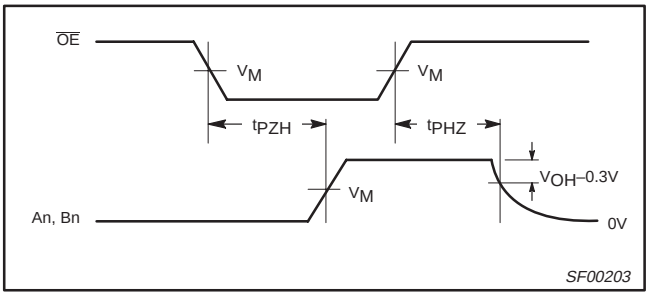
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Non-Inverting Output

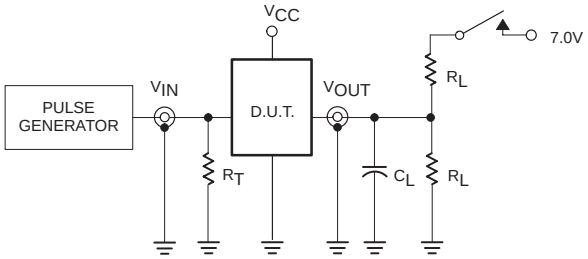


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

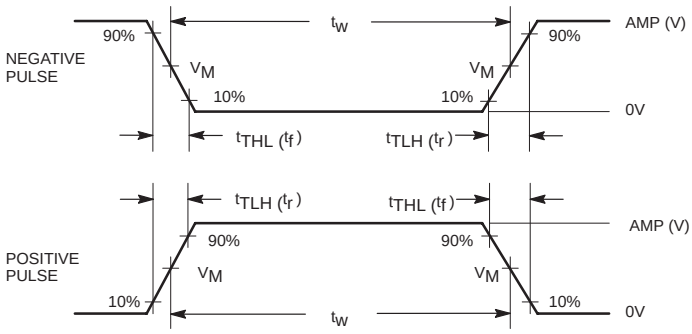


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

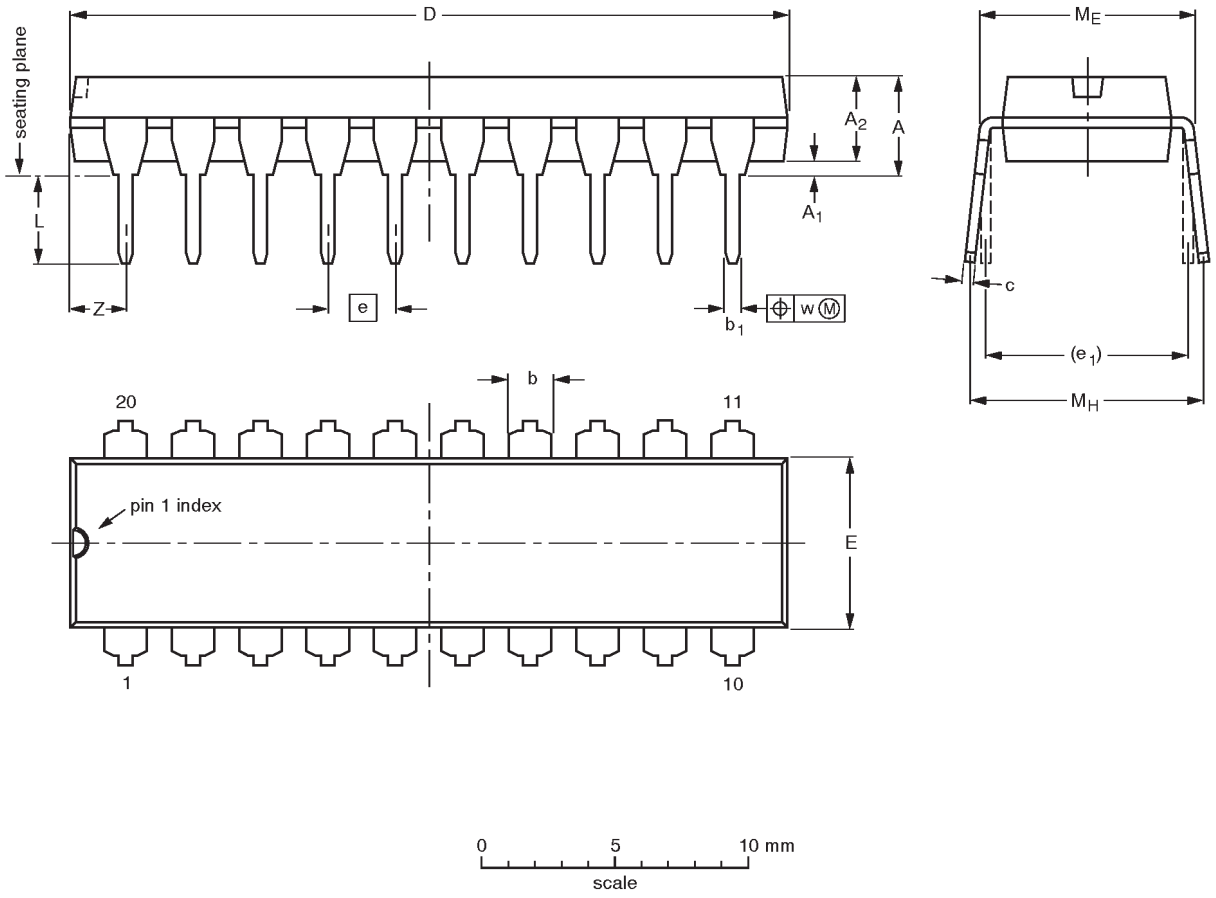
DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

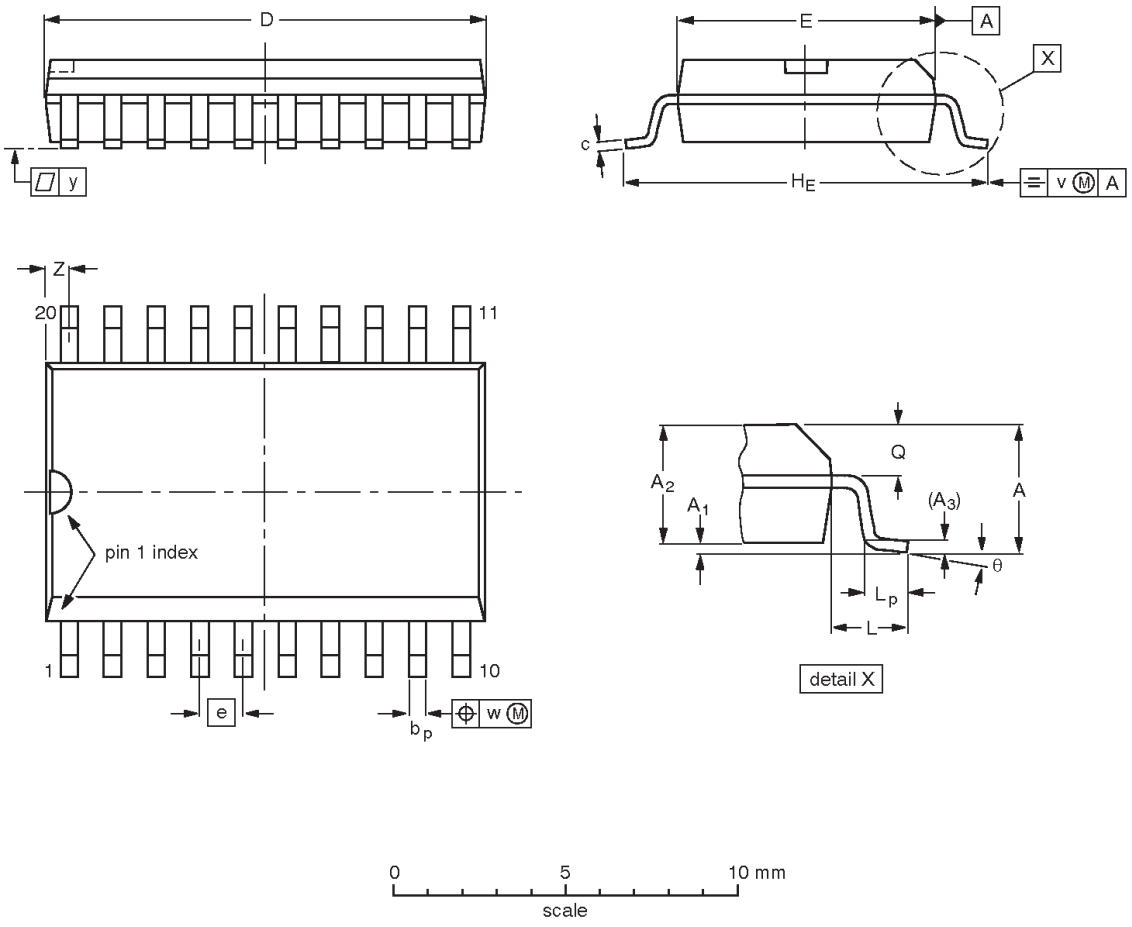
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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