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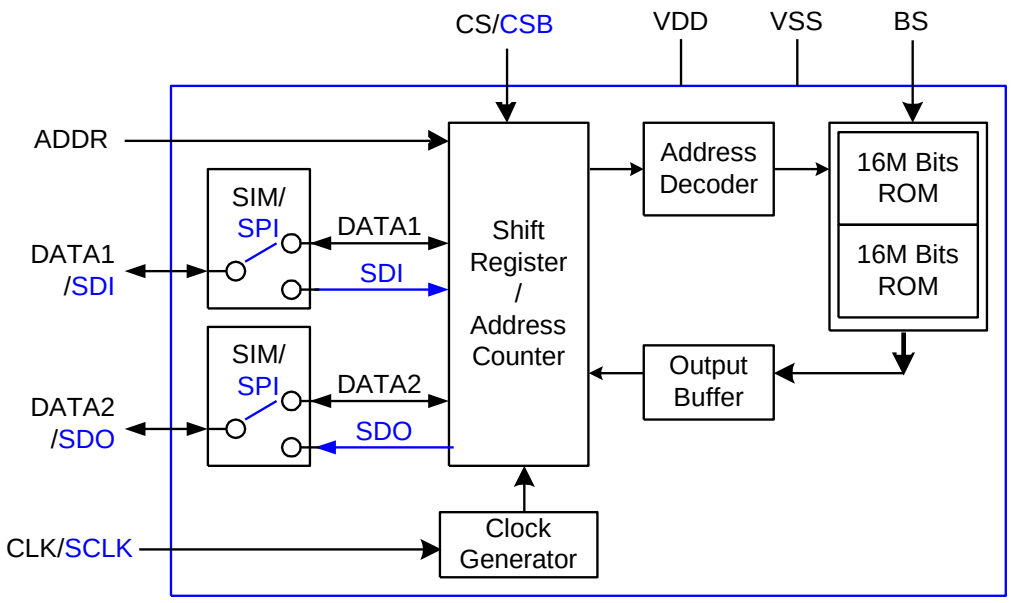
1. GENERAL DESCRIPTION

The N551C321 is an 32Mbit Mask ROM with interface with Nuvoton PowerSpeech, BandDirector and ViewTalk series products to extend the memory size for long duration applications.

2. FEATURES

- Wide range of operation voltage: 2.4 ~ 5.5V @ normal read mode
- ROM size: 32Mbit
- Interface: W551C interface or SPI ROM interface by mask option
- Normal read access time: 500 nS
- Low power consumption
  - Operating current:
    - 2.5mA (max.) for SPI mode
    - 1.0mA (max.) for W551C mode
- Available package form:
  - COB is essential

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1.1 W551C interface pad

SYMBOL	I/O	FUNCTION
BS	I	Memory Bank selection "0": Lower 16Mbit; "1": Higher 16Mbit
ADDR	I	Clock input for shift-in the start address; The first rising edge signals will reset the address counter.
CLK	I	Clock input for Data read/write
DATA1	I/O	Bi-directional data pin with internal pull-high
DATA2	I/O	Bi-directional data pin with internal pull-high for cascade data through
CS	I	Chip select pin, active-low chip enable.
VSS	I	Microcontroller Negative power supply (-).
VDD	I	Microcontroller Positive power supply (+).

4.1.2 SPI interface pad

SYMBOL	I/O	FUNCTION
SDI	I	Command/address input
SDO	O	Data output
SCLK	I	Clock input

SYMBOL	I/O	FUNCTION
CSB	I	Chip select input, low active. When CSB is High, chip is in standby mode and SDO pin is at high impedance
VSS	I	Microcontroller Negative power supply (-).
VDD	I	Microcontroller Positive power supply (+).

5. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	$V_{DD} - V_{SS}$	-	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS}-0.3 ~ V_{DD}+0.3	V
Storage Temp.	T_{STG}	-	-55 ~ +150	°C
Operating Temp.	T_{OPR}	-	0 ~ +70	°C

NOTE: Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability

6. ELECTRICAL CHARACTERISTICS

DC Parameters

(VDD–VSS = 4.5V±10%, TA = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating voltage	VDD		2.4		5.5	V
Operation current	Iop1	W551C interface mode, data output rate 1MHz			1	mA
Operation current	Iop2	SPI interface mode, data output rate 2MHz			2.5	mA
Standby current	Isb	VDD=5.5V			4	μA
Output high current	Ioh	Vout=4.0V		-5		mA
Output low current	Iol	Vout=0.5V		5		mA
Input Low Voltage	V_{IL}	All input pins	-0.3	-	0.8	V
Input High Voltage	V_{IH}	All input pins	2.0	-	VDD	V
Pull-high resistor	Rph2	DATA1, DATA2		750		KΩ

AC Parameters

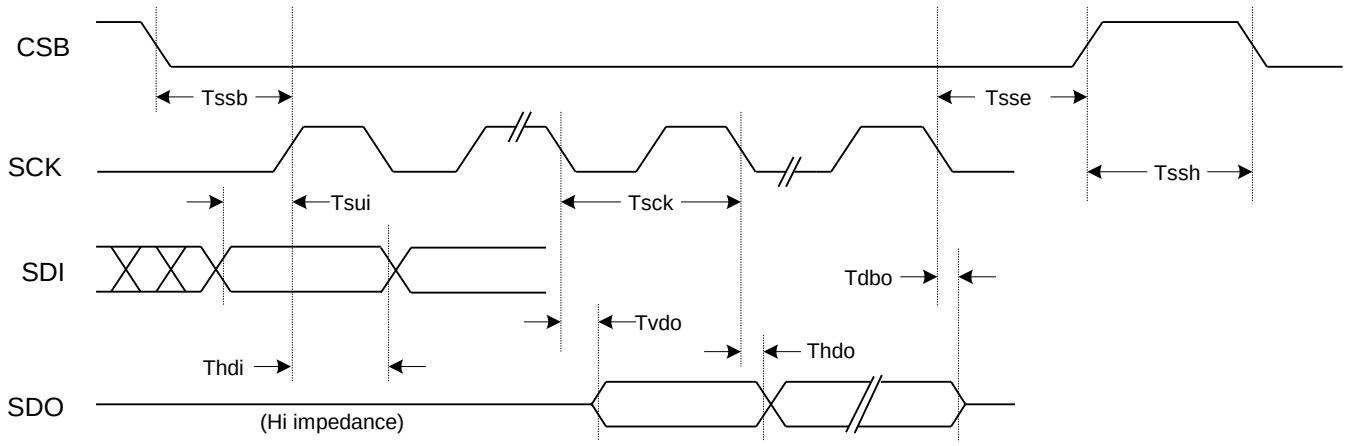
SPI mode interface

(VDD–VSS = 4.5V±10%, TA = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock period	Tsck	Data Read	500			nS
		Fast Data Read	250			nS

Select lead time	Tssb		100			nS
Data input setup time	Tsui		20			nS
Data input hold time	Thdi		20			nS
Data output valid time	Tvdo				85	nS

SPI Mode Interface

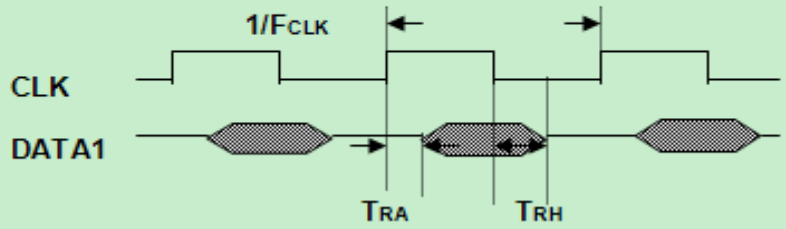


W551C Mode Interface

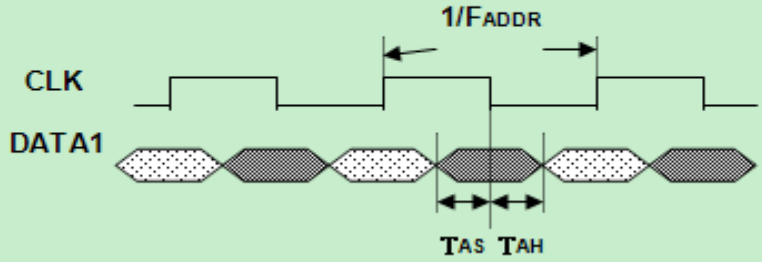
(VDD–VSS = 4.5V, TA = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock frequency of ADDR	F_{ADDR}	VDD = 3.0V	-	-	6	MHz
Clock frequency of CLK	F_{CLK}	VDD < 3.0V VDD ≧ 3.0V	-	-	1 1.5	MHz
Interval time between ADDR and CLK	T_I	Read mode	1	-	-	uS
Interval between DATA to another pin active	T_{CFA}	-	10	-	-	uS
Data access time	T_{RA}	Read mode	-	-	500	nS
Data setup time	T_{AS}	Address shift-in	40	-	-	nS
Data hold time	T_{RH}	Read mode	0	-	-	nS
	T_{AH}	Address shift-in	10	-	-	nS
Transmission time between DATA1 and DATA2	T_{D12} T_{D21}	Cascade Mode, V_{DD}=2.4V	35 20	-	-	nS
PS switch time	T_{PS1} T_{PS2}	Read mode	500 500	-	-	nS
CS switch time	T_{CS1} T_{CS2}	Read mode	500 500	-	-	nS

Read Mode

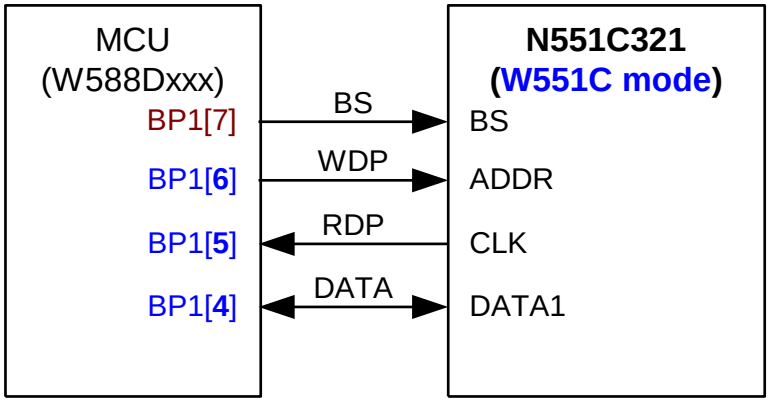


Address Shift-in Cycle

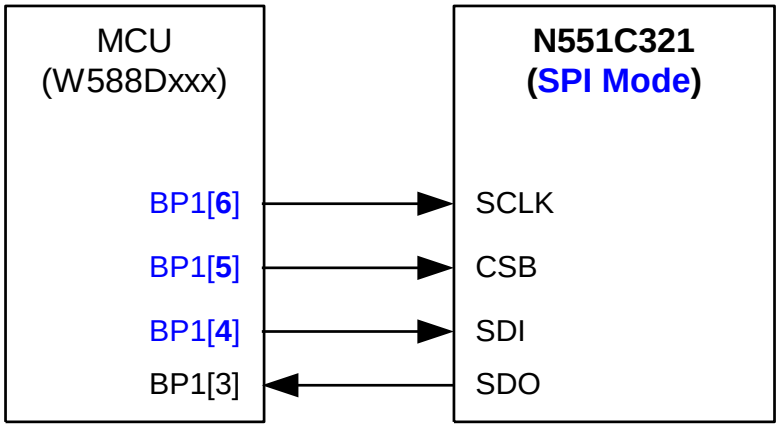


7. APPLICATION CIRCUIT

7.1 W551C Mode



7.2 SPI Mode



8. REVISION HISTORY

Version	Date	Reasons For Change
A1.0	Nov, 2010	First establishment
A2.0	Sep-2011	Revise ADDR, CLK spec in page 5

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