

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode

Silicon Gate

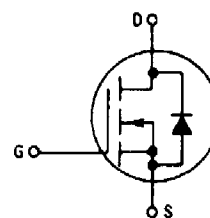
This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP15N05E

TMOS POWER FET
15 AMPERES
 $R_{DS(on)} = 0.1 \text{ OHM}$
50 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-repetitive ($t_p \leq 50 \mu s$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous	I_D	15	Adc
— Pulsed	I_{DM}	40	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	75	Watts
Derate above 25°C		0.6	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

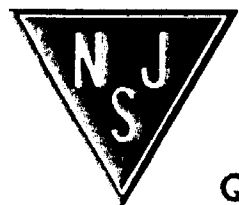
THERMAL CHARACTERISTICS

Thermal Resistance			
Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering	T_L	260	°C
Purposes, 1/8" from case for 5 seconds			



TO-220AB

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MTP15N05E

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V _{(BR)DSS}	50	—	V _{dc}
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)	I _{DSS}	— —	10 100	μA _{dc}
Gate-Body Leakage Current, Forward (V _{GSF} = 20 V _{dc} , V _{DS} = 0)	I _{GSSF}	—	100	nA _{dc}
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 V _{dc} , V _{DS} = 0)	I _{GSSR}	—	100	nA _{dc}

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	V _{GS(th)}	2 1.5	4.5 4	V _{dc}
Static Drain-Source On-Resistance (V _{GS} = 10 V _{dc} , I _D = 7.5 A _{dc})	R _{DS(on)}	—	0.1	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 15 A _{dc}) (I _D = 7.5 A _{dc} , T _J = 100°C)	V _{DS(on)}	— —	2.9 2.4	V _{dc}
Forward Transconductance (V _{DS} = 15 V, I _D = 7.5 A)	g _{FS}	3.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11	C _{iss}	—	700	pF
Output Capacitance		C _{oss}	—	400	
Reverse Transfer Capacitance		C _{rss}	—	200	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 9, 13 and 14	t _{d(on)}	—	50	ns
Rise Time		t _r	—	150	
Turn-Off Delay Time		t _{d(off)}	—	200	
Fall Time		t _f	—	100	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	Q _g	17 (Typ)	35	nC
Gate-Source Charge		Q _{gs}	8 (Typ)	—	
Gate-Drain Charge		Q _{gd}	9 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(I _S = Rated I _D V _{GS} = 0)	V _{SD}	1.8 (Typ)	2.5	V _{dc}
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	320 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _s	7.5 (Typ)	—	

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%