SXGA Flat Panel Controller

GENERAL DESCRIPTION

The MTL007 Flat Panel Display (FPD) Controller is a low-cost input format converter for TFT-LCD Monitor or LCD TV application which accepts 15-pin D-sub RGB graphic signals (through ADC), YUV signals from digital video decoder or digital RGB graphic signals from PanelLink TMDS receiver. It includes a RGB/YUV input processor, video scaling up processor, OSD input interface and output display processor in 128-pin PQFP.

FEATURES

General

- Auto configuration of sampling clock frequency, phase, H/V center, as well as white balance.
- Auto detection of present or non-present or over range sync signals and their polarities.
- Composite sync separation and odd/even field detection of interlaced video.
- No external memory required.
- On-chip output PLL provide clock frequency fine-tune (inverse, duty cycle and delay).
- Serial 2-wire I^2C host interface.
- Embedded power regulator.
- Embedded power on reset circuit.
- 3.3V supplier in 128-pin PQFP package.

Input Processor

- Single RGB (24-bit) input rates up to 135MHz.
- Support both non-interlaced and interlaced RGB graphic input signals.
- YUV 4:2:2 or YUV 4:1:1 (CCIR601/CCIR656) interlaced video input.
- Glue-less connection to Philips SAA711x digital video decoder.
- Built-in YUV to RGB color space converter.
- Compliant with digital LVDS/PanelLink TMDS input interface.
- PC input resolution up to SXGA 1280x1024 @ 75Hz.

Video Processor

- Independent programmable Horizontal and Vertical scaling up ratios from 1 to 32
- Flexible de-interlacing unit for digital YUV video input data.
- Zoom to full screen resolution of de-interlaced YUV video data stream.
- Built-in programmable gain control for white balance alignments.
- Built-in programmable 10-bit gamma correction table.
- Built-in programmable temporal color dithering.
- Built-in programmable interpolation look-up table.
- Built-in programmable sharpening & smoothing filters for edge enhancement.
- Support smooth panning under viewing window change.

Output Processor

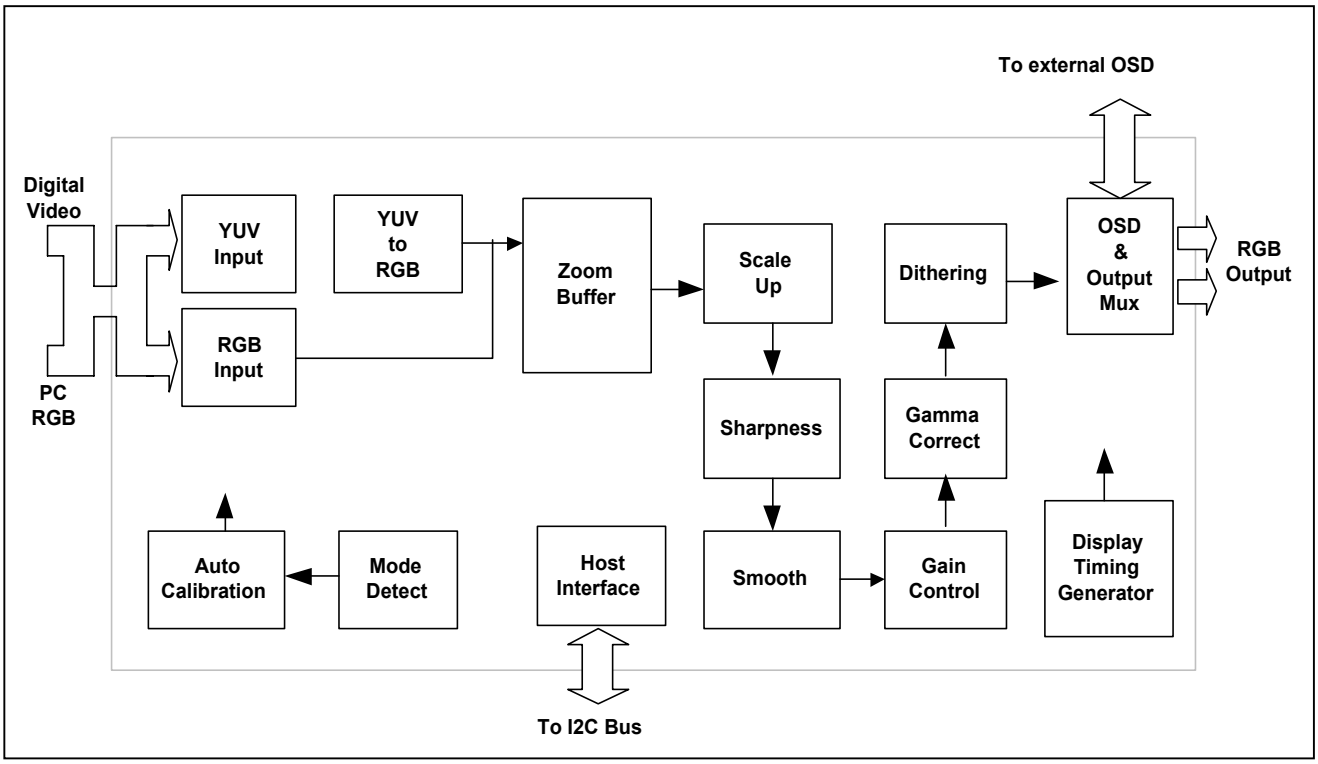
- Dual pixel (36/48-bit) per clock digital RGB output.
- Built-in output timing generator with programmable clock and H/V sync.
- Support VGA/SVGA/XGA/SXGA display resolution.
- Overlay input interface with external OSD controller.
- Double scan capability for interlaced input.

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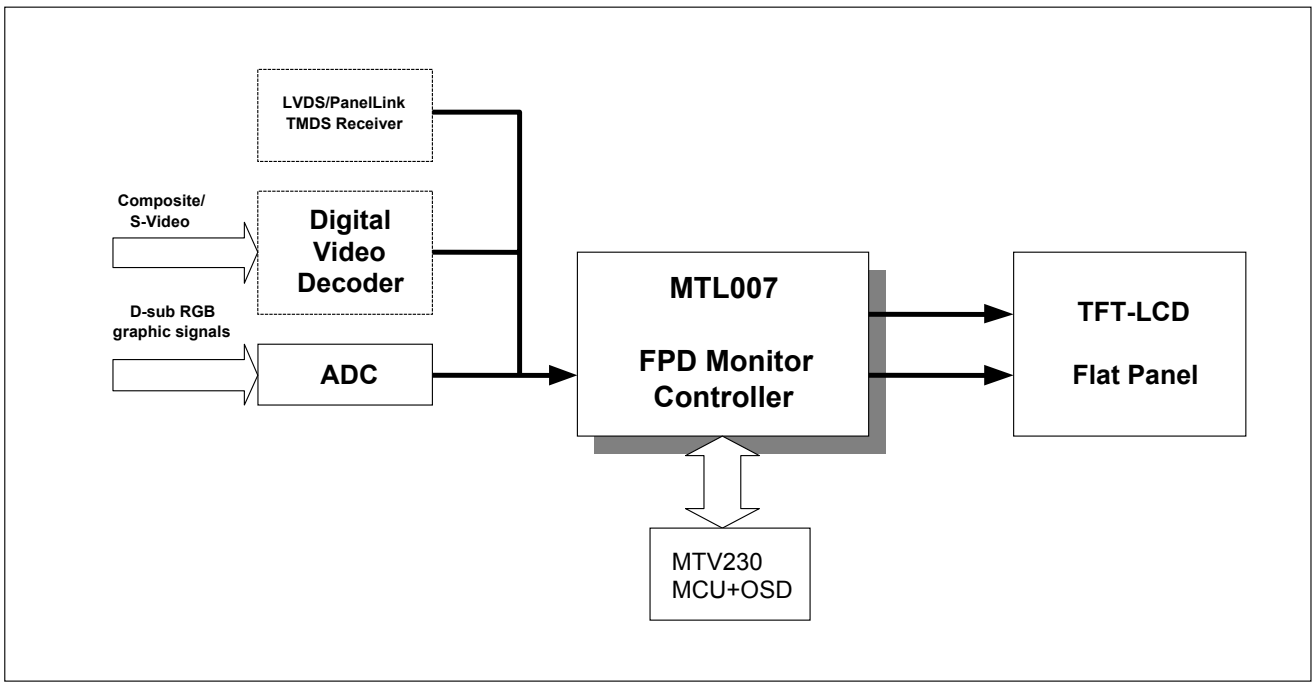
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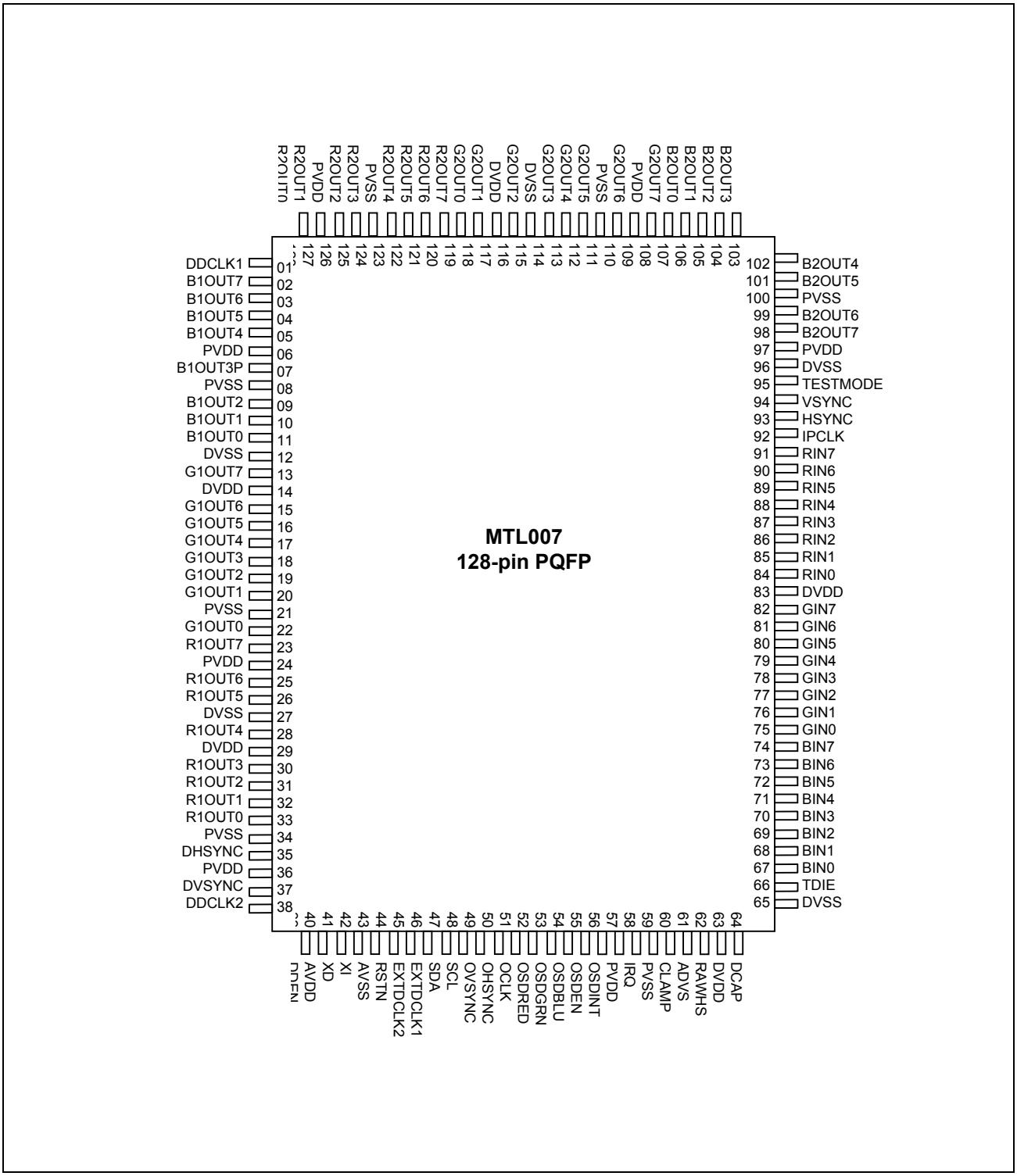
BLOCK DIAGRAM



APPLICATIONS



PIN CONNECTION



PIN DESCRIPTION

ADC Input Interface (RGB or YUV or TMDS Input Data)

Name	Type	Pin No.	Description
IPCLK	I	92	Input pixel clock
VSYNC	I	94	Input Vertical sync
HSYNC/CS	I	93	Input Horizontal or Composite sync
RIN[7:0]/YIN[7:0] (RIN[5:0])	I	91-84 (89-84)	Red or Y channel or TMDS input data (Red channel for 6-bit input)
GIN[7:0]/UVIN[7:0] (GIN[5:0])	I	82-75 (78-75, 91, 90)	Green or UV channel or TMDS input data (Green channel for 6-bit input)
BIN[7:0] (BIN[5:0])	I	74-67 (68, 67, 82-79)	Blue or TMDS input data, or Control bit for YUV video input Bit 4: VPHREF, Video input Horizontal reference signal Bit 3: VPVS, Video input VSYNC signal Bit 2: VPODD, Video input ODD/EVEN field signal Bit 1: VPHS, Video input HSYNC signal Bit 0: VPCLK, Video input clock signal (Blue channel for 6-bit input)
RAWHS	I	62	Input source HSYNC for measurement
TDIE	I	66	TMDS digital input enable
CLAMP	O	60	Clamp pulse output for ADC

Display Output Interface

Name	Type	Pin No.	Description
DDCLK1		1	Display output clock
DVSYNC	O	37	Display Vertical sync output
OE	O	39	Display output enable
DHSYNC	O	35	Display Horizontal sync output
DDCLK2	O	38	Display output clock
R1OUT[0:7]	O	33-30, 28, 26-25, 23	Red output even data , bit[7:2] for 6-rlogin rbit panel
G1OUT[0:7]	O	22, 20-15, 13	Green output even data , bit[7:2] for 6-bit panel
B1OUT[0:7]	O	11-9, 7, 5-3, 2	Blue output even data , bit[7:2] for 6-bit panel
R2OUT[0:7]	O	128-127, 125-124, 122-119	Red output odd data , bit[7:2] for 6-bit panel
G2OUT[0:7]	O	118,117, 115, 113-111, 109,107	Green output odd data , bit[7:2] for 6-bit panel
B2OUT[0:7]	O	106-101, 99-98	Blue output odd data , bit[7:2] for 6-bit panel

Host Interface

Name	Type	Pin No.	Description
RST#	I	44	System reset input, active low.
SCL	I	48	Serial bus clock

SDA	I/O	47	Serial bus data
TESTMODE	I	95	Test Mode, Normally grounded.
IRQ	O	58	Interrupt request output

OSD Interface

Name	Type	Pin No.	Description
OVSYNC	O	49	Vertical sync for external OSD
OHSYNC	O	50	Horizontal sync for external OSD
OCLK	O	51	Clock for external OSD
OSDRED	I	52	OSD red input
OSDGRN	I	53	OSD green input
OSDBLU	I	54	OSD blue input
OSDEN	I	55	OSD overlay enable
OSDINT	I	56	OSD intensity

Other Interface

Name	Type	Pin No.	Description
XI	I	42	Oscillator frequency input
XO	O	41	Oscillator frequency output
EXTDCLK1	I	46	External display clock input 1
EXTDCLK2	I	45	External display clock input 2
ADVS	O	61	Vertical sync for A/D converter

3.3V Power and Ground

Name	PIN No.	Description
DVDD	14,29,63,83,116	Digital power 3.3V
DCAP	64	External CAP for digital Power
DVSS	12,27,65,96,114	Digital ground
PVDD	6,24,36,57,97,108, 126	Pad power 3.3V
PVSS	8,21,34,59,100,110, 123	Pad ground
AVDD	40	Analog power 3.3V
AVSS	43	Analog ground

FUNCTIONAL DESCRIPTION

INPUT PROCESSOR

General Description

The function of Input Interface is to provide the interface between the MTL007 and external input devices. It can process both non-interlaced and interlaced RGB graphic input, YUV video input, and digital RGB input compliant with digital LVDS/PanelLink TMDS interface. It also contains the built-in YUV to RGB color space converter.

i) RGB Input Format

Since the MTL007 is a low cost solution, the RGB input port can only work in Single Pixel mode (24 bits). The R/G/BIN ports are sampled at the rising edge of the RGB input clock.

ii) TMDS Input Format

The Digital RGB input port works just in the same way as Sec 3.1.1 except one more input pin is needed: Digital Input Enable DIEN.

With a single pixel input interface, the supported format is up to true color, including 18 bit/pixel or 24 bit/pixel.

iii) YUV Input Format

The YUV input port supports interlaced video data from the most common video decoder ICs like SAA711x. The 16 bit data bus is shared with the ports RIN[7:0] and GIN[7:0]. The 16 bit data is sampled at the rising edge of the shared video clock VPCLK when the shared data enable HREF is active. The supported formats are YUV4:1:1 and YUV4:2:2 with CCIR601/CCIR656 standard.

iv) Input HSYNC Path

Besides the pin HSYNC, the MTL007 provides another pin RAWHS to support Sync Processor in the MTL007.

Generally, the HSYNC generated by an ADC may have a very narrow pulse width and a different polarity from the original HSYNC provided by the source. The RAWHS input provides the path of original HSYNC connection to the MTL007, which makes Sync Processor in the MTL007 work correctly.

v) YUV to RGB Converter

It is used to convert YCbCr format into RGB format. The basic equations are as follows:

$$R = Y + 1.371(Cr - 128)$$

$$G = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$$

$$B = Y + 1.732(Cb - 128)$$

vi) De-interlace mode

For interlace input, the MTL007 features de-interlacing algorithm for processing interlaced video data.In this mode, two fields are toggled displayed. The missing lines are calculated from interpolating the neighbor lines. This algorithm has an average good quality for still and moving picture.

vii) Sync Processor

The V/H SYNC processing block performs the functions of Composite signal separation/insertion, SYNC inputs presence check, frequency counting, polarity detection and control. It contains a de-glitch circuit to filter out any pulse shorter than one OSC period treated as noise on V/H SYNC pulses.

□ **V/H SYNC Frequency Counter**

The MTL007 can measure VSYNC/HSYNC frequency counted in proper clock and save the information in registers. Users can read out them to calculate VSYNC/HSYNC frequency as following formulas:

$f_{vsync} = f_{osc} / N_{vsync} \times 1/256$

$f_{hsync} = f_{osc} / N_{hsync} \times 8$

,Where f_{vsync} : VSYNC frequency

f_{hsync} : HSYNC frequency

f_{osc} : oscillator clock with 14.31818 MHz

N_{vsync} : counted number of VSYNC

N_{hsync} : counted number of HSYNC

□ **V/H SYNC Presence Check**

This function checks the input VSYNC, where Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz, and the input HSYNC, where Hpre flag is set when HSYNC is over 10Khz or cleared when HSYNC is under 10Hz.

□ **V/H Polarity Detect**

This function detects the input VSYNC/HSYNC high and low pulse duty cycles. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted.

□ **Composite SYNC separation/insertion**

The MTL007 continuously monitors the input HSYNC. If the input VSYNC can be extracted from it, a CVpre flag is set. The MTL007 can insert HSYNC pulse during Composite VSYNC's active time and the insertion frequency can adapt to original HSYNC's.

viii) Auto Tune

Auto Tune function consists of Auto Position automatically centering the screen and Auto Calibration containing Phase Calibration, Histogram, Min/Max Value, and Pixel Grab described as below. With this auto adjustment support, it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured. Firmware can adjust input image registers automatically by reading Auto Tune's registers in single or burst mode.

□ **Auto Position**

The MTL007 provides Horizontal/Vertical back porch and active region values. Users can use these values to set input sample registers to aid in centering the screen automatically.

□ **Phase Calibration**

The MTL007 provides Auto Calibration registers to measure the quality of current ADC's phase and frequency. The biggest Auto Calibration registers value means the right value of ADC's phase and frequency. The MTL007 has two kinds of algorithms to calculate Auto Calibration's value. One is traditional Difference method; the other is MYSON's proprietary method. It is suggested to use the latter one for better performance.

□ **Histogram**

Histogram means the total number of input pixels below/above one threshold value, for individual R, G, B colors. This advanced function helps firmware to analyze ADC performance. Usually Firmware can use this information to measure ADC's noise margin, adjust its offset and gain, or even aid in the mode detection.

□ **Min/Max Value**

Min/Max value means the minimum or maximum pixel value within the specified input active image region for each RGB channel. This information is usually used to adjust ADC's offset and gain.

□ **Pixel Grab**

Pixel Grab means users can grab a single input pixel at any one point. The position of the point can be programmed by users. This is another traditional method to measure ADC's phase and frequency.

VIDEO PROCESSOR

General Description

The MTL007 possesses a powerful and programmable video processor by providing the following functions: Scaling Up/Down, Edge Enhancement (Sharpness & Smooth Control), Gain Control, Brightness Control, Gamma Gamma Correction, and Dithering Control.

The block diagram of Video Processor is as follows:

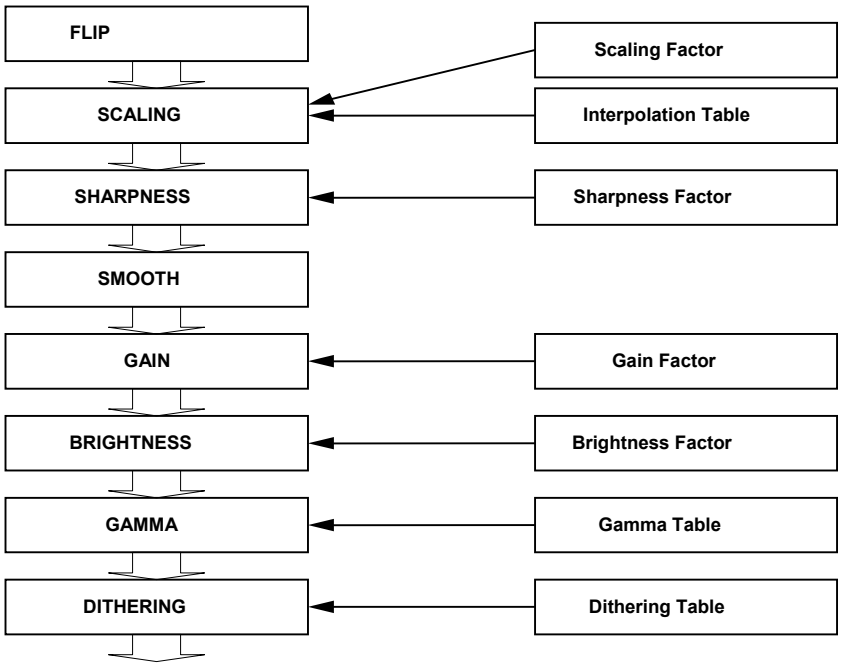


Figure-1 Video Processor Block Diagram

i) Scaling

The MTL007 provides scaling function up ranging from 1 to 32, and for both horizontal and vertical processing.

For scaling up, both horizontal and vertical processing, the MTL007 provides four methods:

- **Pass Mode**: Image will be passed through without considering any scaling factor.
- **Duplicate Mode**: Image will be scaled up based on scaling factor. Every point of output image comes from the input. By this method, Output image will have a good contrast but may be non-uniformed.
- **Bilinear Mode**: Image will be scaled up based on scaling factor. Every point of output image data will be filtered by bilinear filter. By this method, output image will have a good scaling quality but may be blurred.
- **Interpolation Table Mode**: Image will be scaled up based on scaling factor. Every point of output image data will be filtered by user-defined filter.

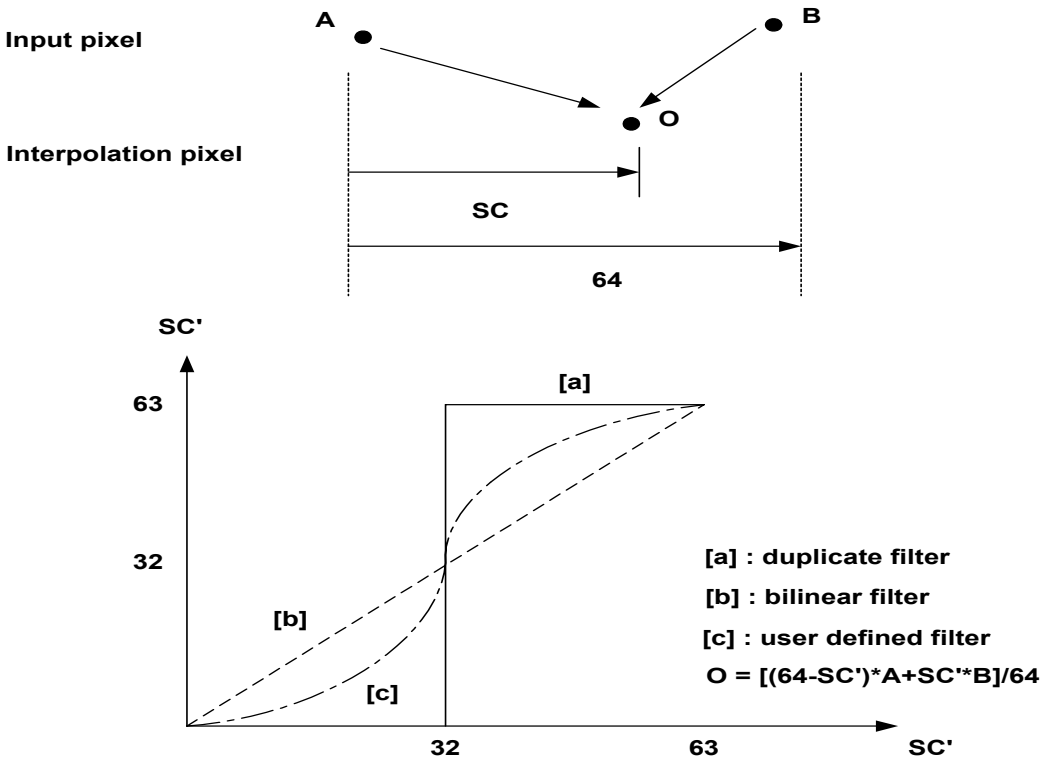


Figure-2 Scaling filter

ii) Edge Enhancement

The MTL007 uses a 5x1 Sharpening filter and a 5x1 Smoothing filter to improve edge effect. The coefficients of latter are fixed, but the other are programmable with eight steps.

iii) Gain/Brightness Control

The MTL007 provides Gain and Brightness control to adjust the contrast and brightness of output color by programming gain and brightness coefficients. This adjustment is applied to RGB colors individually. Auto-white balance is possible by using this function.

iv) Gamma Correction

Gamma Correction is used to compensate the non-linearity of LCD display panel. The MTL007 contains an 8-bit Gamma table to fix this phenomenon.

v) Color Dithering

The MTL007 supports true color (8 bits per color) or high color (6 bits per color) display.

In the latter case, users can turn on dithering function to avoid artificial contour due to truncation. For dithering, it supports two methods:

- □ **Static dithering**: Dithering coefficient is fixed.
- □ **Temporal dithering:** Dithering coefficient will change by time.

OUTPUT PROCESSOR

General Description

Output processor provides the interface for both LCD panel and OSD controller. Output frame rate must be equal to input frame rate and output display time must be equal to input display time, because of no frame buffer.

i) Display Timing Generation

Output frame rate is equal to input frame and external frame buffer is not needed.

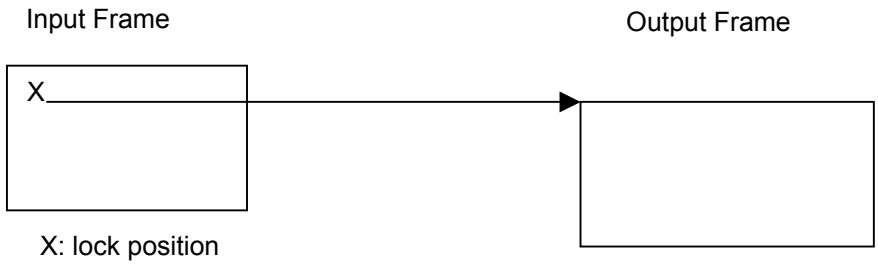


Figure-3 Display Timing modes

ii) OSD Overlay

The MTL007 allows the integration of overlay data with the scaled output pixel stream. It provides a fully compatible OSD interface. Individual OSD clock, OSD HSYNC and OSD VSYNC are sent to external OSD device. The MTL007 receives OSD Enable, OSD intensity, OSD Red, OSD Green, and OSD Blue from external OSD device. Another MTL007 provides OSD overlay-transparent function in two modes, each has 16 steps by programming weight factors.

iii) RGB Output Format

The MTL007 output interface consists of two pixel ports, each containing Red, Green, and Blue color information with a resolution of 6/8 bits per color. These two ports are mapped to PORT1 and PORT2.

The control signals for output port are display horizontal sync signal (DHSYNC), display vertical sync signal (DVSYNC) and display data enable signal (DDEN).

All the signals mentioned above are synchronous to the output clock. The output timing relative to the active edge of the output clock is programmable.

There are RGB output formats:

□ **Dual Pixel Mode**

It is designed to support TFT panels with dual pixel input. PORT1 and PORT2 are used. The first pixel is at PORT1, and the second at PORT2.

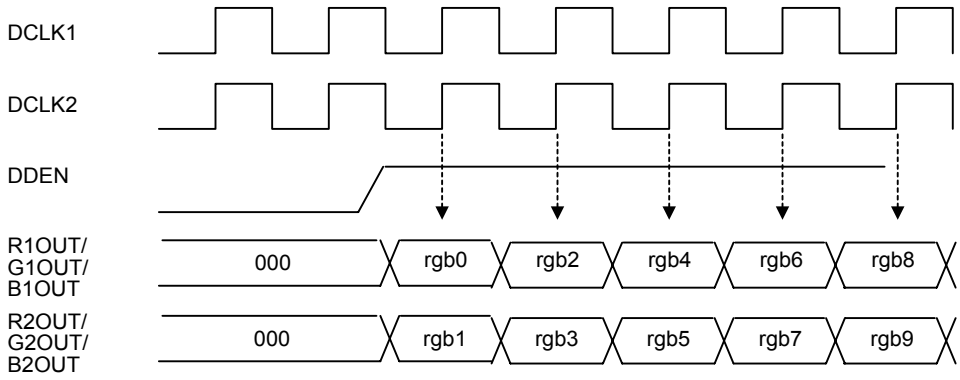


Figure-4 Display Data Timing

HOST INTERFACE

General Description

The main function of Host Interface is to provide the interface between the MTL007 and external CPU by 2-wire I2C Bus. It can generate all the I/O decoded control timing to control all the registers in the MTL007.

i) I2C Serial Bus

The I2C serial interface use 2 wires, SCK (clock) and SDA(data I/O). The SCK is used as the sampling clock and SDA is a bi-directional signal for data. The communication must be started with a valid START condition, concluded with STOP condition and acknowledged with ACK condition by receiver.

The I2C bus device address of the MTL007 is 0111010x.

SCK, serial bus clock.

SDA, bi-directional serial bus data.

The START condition means a HIGH to LOW transition of SDA when SCK is high, the STOP condition means a LOW to HIGH transition of SDA when SCK is high. And data of SDA only can change during SCK is low as shown in Figure-5.

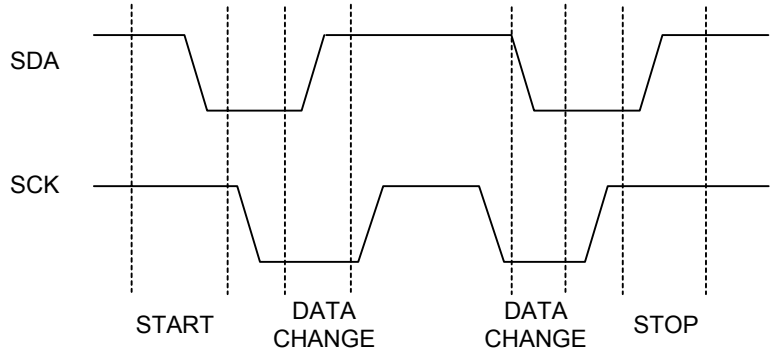


Figure-5 START, STOP and DATA definition

The I2C interface supports Random Write, Sequential Write, Current Address Read, Random Read and Sequential Read operations.

□ Random Write

For Random Write operation, it contains the slave address with R/W bit set to 0 and the word address that is comprised of eight bits and provides the access to any one of 256 bytes in the selected memory range. Upon receipt of the word address, the MTL007 responds with an Acknowledge, waits for the data bits again responding an Acknowledge, and then the master generates a stop condition as shown in Figure-6.

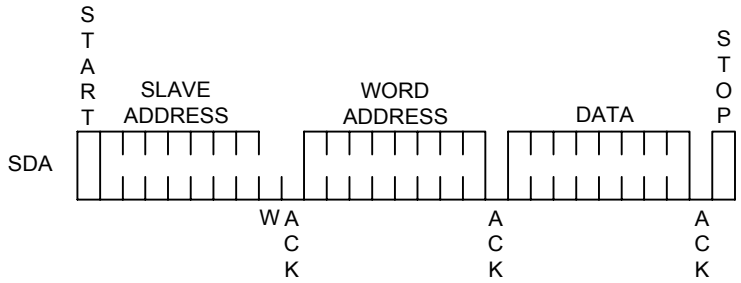


Figure-6 Random Write

□ Sequential Write

The initial step of Sequential Write is the same as Random Write, after the receipt of each word data, the MTL007 will respond with an Acknowledge and then internal address counter will increment by one for the next data write. If the master would stop writing data, it generates a stop condition as shown in Figure-7.

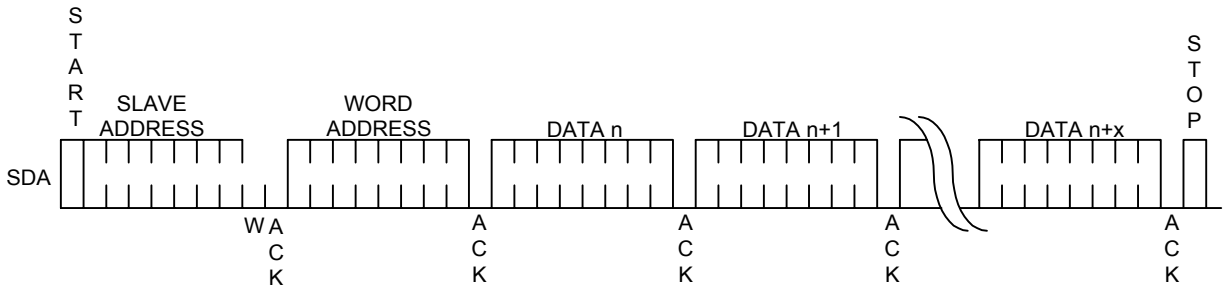


Figure-7 Sequential Write

□ Current Address Read

The MTL007 contains an address counter which maintains the last access address incremented by one. If the last access address is n, the read data should access from address n+1. Upon receipt of the slave address with R/W bit set to 1, the MTL007 generates an Acknowledge and transmits eight bits data. After receiving data the master will generate a stop condition instead of an Acknowledge as shown in Figure-8.

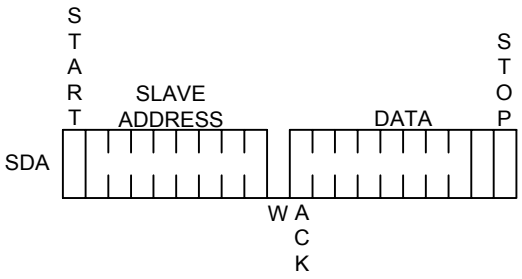


Figure-8 Current Address Read

□ Random Read

The operation of Random Read allows access to any address. Before reading data operation, it must issue a “dummy write” operation — a start condition, slave address and then the word address for read. After responding the word address acknowledge, the master generates a start condition again and slave address with R/W bit is set to 1. The MTL007 then transmits the 8 bits of data. Upon the completion of receiving data, the master will generate a stop condition instead of an Acknowledge as shown in Figure-9.

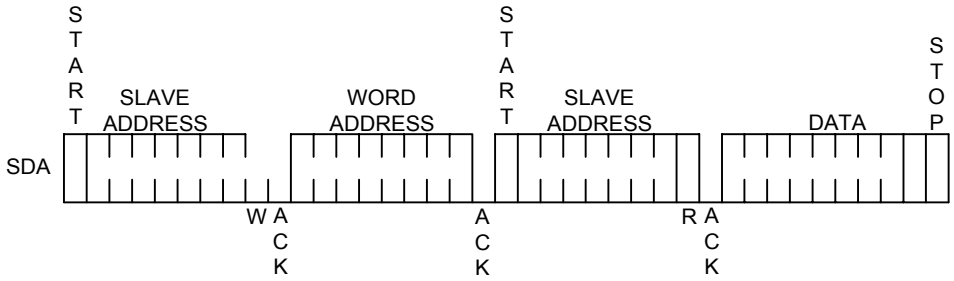


Figure-9 Random Read

□ Sequential Read

The initial step can be as either Current Address Read or Random Read. The first read data is transmitted the same manner as other read methods. However, the master generates an Acknowledge indicating that it requires more data to read. The MTL007 continues to output data for each Acknowledge received. The output data is sequential and the internal address counter increments by one for next read data as shown in Figure-10.

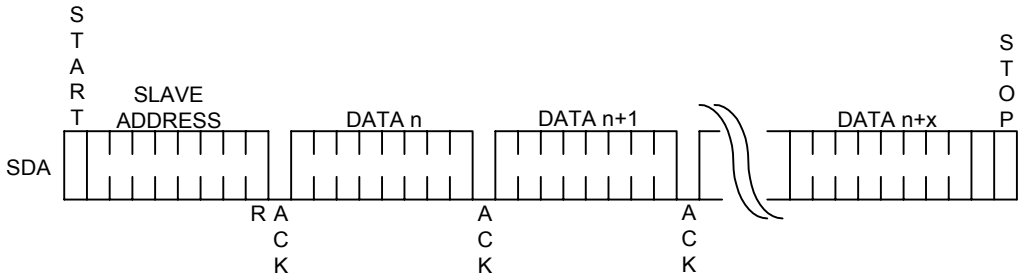


Figure-10 Sequential Read

ii) Interrupt

The MTL007 supports one interrupt output signal (IRQ) which can be programmed to provide SYNC related or function status related interrupts to the system. Upon receiving the interrupt request, Firmware needs to first check the interrupt event by reading the Interrupt Flag Control registers (Reg. E8h and E9h) to decide what events are happening. After the operation is finished, Firmware needs to clear interrupt status by writing the same registers Reg. E8h and E9h. Furthermore, by using the Interrupt Flag Enable registers (Reg. EAh and EBh), each interrupt event can be masked.

iii) Update Register Contents

I/O write operation to some consecutive register sets can have the “Double Buffer” effect by setting the Reg. C1h/D4. Written data is first stored in an intermediate bank of latches and then transferred to the active register set by setting Reg. C1h/D1-0.

ON-CHIP PLL

General Description

The MTL007 needs two clock sources to drive synchronous circuits on chip. These clocks are generated from the internal Phase Lock Loop (PLL) circuits with reference to the oscillator clock which is applied to pin XI and XO by an external quartz crystal at 14.31818 MHz. The first one is the same as to the oscillator clock at frequency (14.31818 MHz) to detect and measure graphic vertical and horizontal SYNC Frequency, Polarity as well as Presence. The second is the display clock for display controller on chip and output signals to LCD panel.

i) Reference Clock

It is the counting basis of counter values in SYNC Processor such as VS and HS period count registers; that is, the read back values from these registers must multiply the period of this clock to estimate VS and HS frequency. Incorporating with polarity and frequency information of VS and HS, it can show the input graphic image mode and pixel clock frequency.

ii) Display Clock

This clock is the synchronous clock for LCD panel. According to the LCD panel resolution of applications, the display clock range is from 50 MHz to 200 MHz by means of choosing a set of appropriate values for M, N as well as R. The formula to calculate the desired frequency of display clock is as follows:

$f_{mclk} = f_{osc} \times (M+1)/(N+1) \times 1/R$

Where f_{mclk} : the desired display clock

f_{osc} : oscillator clock with 14.31818 MHz

M : post-divider ratio

N : pre-divider ratio

R : optional divider ratio

REGISTER DESCRIPTION

Input Control Register

Address	Mode	Registers	Reset value
00h	R/W	Input Image Vertical Active Line Start - Low	00h
01h	R/W	Input Image Vertical Active Line Start - High	00h
02h	R/W	Input Image Vertical Active Lines - Low	00h
03h	R/W	Input Image Vertical Active Lines - High	00h
04h	R/W	Input Image Horizontal Active Pixel Start - Low	00h
05h	R/W	Input Image Horizontal Active Pixel Start - High	00h
06h	R/W	Input Image Horizontal Active Pixels - Low	00h
07h	R/W	Input Image Horizontal Active Pixels - High	00h
10h	R/W	Input Image Control Register 0	00h
11h	R/W	Input Image Control Register 1	00h
12h	R/W	Input Image Control Register 2	00h
13h	R/W	Input Image Control Register 3	00h
14h	R/W	Input Image Control Register 4	00h
15h	R/W	Input Image Control Register 5	00h
16h	R/W	Input Image Control Register 6	00h
* 17h	R/W	Input Invert Control	00h
* 18h	R/W	Input Delay Control 0	00h
* 19h	R/W	Input Delay Control 1	00h
1Ah	R/W	Input Delay Control 2	00h
1Ch	R/W	HS1 Sample Window Forward Extend	00h
1Dh	R/W	HS1 Sample Window Backward Extend	00h
* 1Eh	R/W	Input Miscellaneous Control	00h
1Fh	RO	Input Image Status Register	-
20h	R/W	Input Image Back Porch Guard Band	00h
21h	R/W	Input Image Front Porch Guard Band	00h

Frame Sync Registers

Address	Mode	Registers	Reset value
* 28h	R/W	Frame Sync Control	00h
* 29h	R/W	NFB Display VSYNC Control	00h
2Ch	R/W	Input Image Vertical Lock Position - Low	00h

2Dh	R/W	Input Image Vertical Lock Position - High	00h
2Eh	R/W	Input Image Horizontal Lock Position - Low	00h
2Fh	R/W	Input Image Horizontal Lock Position - High	00h

Auto Calibration Registers

Address	Mode	Registers	Reset value
30h	R/W	Auto Calibration Control 0	80h
31h	R/W	Auto Calibration Control 1	00h
34h	RO	Auto Calibration RED Value - Byte 0	-
35h	RO	Auto Calibration RED Value - Byte 1	-
36h	RO	Auto Calibration RED Value - Byte 2	-
37h	RO	Auto Calibration RED Value - Byte 3	-
38h	RO	Auto Calibration GREEN Value - Byte 0	-
39h	RO	Auto Calibration GREEN Value - Byte 1	-
3Ah	RO	Auto Calibration GREEN Value - Byte 2	-
3Bh	RO	Auto Calibration GREEN Value - Byte 3	-
3Ch	RO	Auto Calibration BLUE Value - Byte 0	-
3Dh	RO	Auto Calibration BLUE Value - Byte 1	-
3Eh	RO	Auto Calibration BLUE Value - Byte 2	-
3Fh	RO	Auto Calibration BLUE Value - Byte 3	-
40h	R/W	Pixel Grab V Reference Position – Low	00h
41h	R/W	Pixel Grab V Reference Position – High	00h
42h	R/W	Pixel Grab H Reference Position – Low	00h
43h	R/W	Pixel Grab H Reference Position – High	00h
44h	R/W	Histogram Reference Color - RED	00h
45h	R/W	Histogram Reference Color - GREEN	00h
46h	R/W	Histogram Reference Color - BLUE	00h

Sync Processor Registers

Address	Mode	Registers	Reset value
48h	R/W	SYNC Processor Control	00h
49h	R/W	Auto Position Control	00h
4Ah	R/W	Auto Position Reference Color - RED	00h
4Bh	R/W	Auto Position Reference Color - GREEN	00h
4Ch	R/W	Auto Position Reference Color - BLUE	00h

4Eh	R/W	Clamp Pulse Control 0	00h
4Fh	R/W	Clamp Pulse Control 1	00h
50h	RO	Input VS Period Count by REFCLK - Low	-
51h	RO	Input VS Period Count by REFCLK - High	-
52h	RO	Input V Back Porch Count by Input HS - Low	-
53h	RO	Input V Back Porch Count by Input HS - High	-
54h	RO	Input V Active Lines Count by Input HS - Low	-
55h	RO	Input V Active Lines Count by Input HS - High	-
56h	RO	Input V Total Lines Count by Input HS - Low	-
57h	RO	Input V Total Lines Count by Input HS - High	-
58h	RO	Input HS Period Count by REFCLK - Low	-
59h	RO	Input HS Period Count by REFCLK - High	-
5Ah	RO	Input H Back Porch Count by Input Pixel Clock - Low	-
5Bh	RO	Input H Back Porch Count by Input Pixel Clock - High	-
5Ch	RO	Input H Active Pixels Count by Input Pixel Clock - Low	-
5Dh	RO	Input H Active Pixels Count by Input Pixel Clock - High	-
5Eh	RO	Input H Total Pixels Count by Input Pixel Clock - Low	-
5Fh	RO	Input H Total Pixels Count by Input Pixel Clock - High	-

Display Control Registers

Address	Mode	Registers	Reset value
60h	R/W	Display Vertical Total - Low	00h
61h	R/W	Display Vertical Total - High	00h
62h	R/W	Display Vertical SYNC End- Low	00h
63h	R/W	Display Vertical SYNC End - High	00h
64h	R/W	Display Vertical Active Start - Low	00h
65h	R/W	Display Vertical Active Start - High	00h
66h	R/W	Display Vertical Active End - Low	00h
67h	R/W	Display Vertical Active End - High	00h
* 68h	R/W	Display Vertical Border Start - Low	00h
* 69h	R/W	Display Vertical Border Start - High	00h
* 6Ah	R/W	Display Vertical Border End - Low	00h
* 6Bh	R/W	Display Vertical Border End - High	00h
70h	R/W	Display Horizontal Total - Low	00h

71h	R/W	Display Horizontal Total - High	00h
72h	R/W	Display Horizontal SYNC End - Low	00h
73h	R/W	Display Horizontal SYNC End - High	00h
74h	R/W	Display Horizontal Active Start - Low	00h
75h	R/W	Display Horizontal Active Start - High	00h
76h	R/W	Display Horizontal Active End - Low	00h
77h	R/W	Display Horizontal Active End - High	00h
* 78h	R/W	Display Horizontal Border Start - Low	00h
* 79h	R/W	Display Horizontal Border Start - High	00h
* 7Ah	R/W	Display Horizontal Border End - Low	00h
* 7Bh	R/W	Display Horizontal Border End - High	00h
* 7Eh	R/W	NFB Timing Load Value	00h
7Fh	R/W	NFB Timing Control	60h
88h	R/W	Output Image Control Register 0	00h
89h	R/W	Output Image Control Register 1	00h
8Ah	R/W	Output Image Control Register 2	00h
90h	R/W	Color Gain Control - RED	80h
91h	R/W	Color Gain Control - GREEN	80h
92h	R/W	Color Gain Control - BLUE	80h
93h	R/W	Brightness Control - RED	00h
94h	R/W	Brightness Control - GREEN	00h
95h	R/W	Brightness Control - BLUE	00h
* 96h	R/W	Border Window Color - RED	00h
* 97h	R/W	Border Window Color - GREEN	00h
* 98h	R/W	Border Window Color - BLUE	00h
* 9Eh	R/W	Dithering Register	-
9Fh	R/W	Gamma Table Data Port	-
A0h	R/W	OSD Control Register 0	08h
A1h	R/W	OSD Control Register 1	00h
A2h	R/W	OSD Control Register 2	00h
A3h	R/W	OSD Control Register 3	00h
A4h	R/W	Output Invert Control	00h
A5h	R/W	Output Tri-State Control	00h

A6h	R/W	Output Clocks Delay Adjustment	00h
A7h	R/W	Output Clocks Duty Cycle Adjustment	00h
* A8h	R/W	Display Line Buffer Data Sample Adjustment	00h
A9h	R/W	Output Miscellaneous Control	00h
AAh	R/W	Output Vertical Active Line Number - Low	FFh
ABh	R/W	Output Vertical Active Line Number - High	02h
ACh	RO	Output Horizontal Total Pixel Number – Low	-
ADh	RO	Output Horizontal Total Pixel Number – High	-
AEh	RO	Output Horizontal Total Residue Number – Low	-
AFh	RO	Output Horizontal Total Residue Number - High	-

Zoom Control Register

Address	Mode	Registers	Reset value
B0h	R/W	Zoom Control Register 0	00h
B1h	R/W	Zoom Control Register 1	00h
B4h	R/W	Zoom Vertical Scale Ratio - Low	00h
B5h	R/W	Zoom Vertical Scale Ratio - High	00h
B6h	R/W	Zoom Horizontal Scale Ratio - Low	00h
B7h	R/W	Zoom Horizontal Scale Ratio – High	00h
BFh	R/W	Interpolation Table Data Port	-

Host Control Register

Address	Mode	Registers	Reset value
C1h	R/W	Host Control Register 1	00h
* C6h	R/W	Host Fill Color - RED	00h
* C7h	R/W	Host Fill Color - GREEN	00h
* C8h	R/W	Host Fill Color - BLUE	00h
CBh	RO	Host Access Mode Status	-

Clock Control Registers

Address	Mode	Registers	Reset value
E0h	R/W	Clock Control Register	00h
E1h	WO	Clock Synthesizer Value Load	-
E2h	R/W	Clock Synthesizer N Value	0Bh
E3h	R/W	Clock Synthesizer M Value	32h

E6h	R/W	Clock Synthesizer R Value	00h

Interrupt Control Registers

Address	Mode	Registers	Reset value
E8h	R/W	SYNC Interrupt Flag Control	00h
E9h	R/W	General Interrupt Flag Control	00h
EAh	R/W	SYNC Interrupt Enable Control	00h
EBh	R/W	General Interrupt Enable Control	00h
ECh	R/W	HS Frequency Change interrupt Compare	00h

Miscellaneous Registers

Address	Mode	Registers	Reset value
* F0h	RO	Device/Revision ID	10h
F1h	R/W	Power Management Control	00h
* F8h	R/W	Line Buffer Self Test Control	02h
* F9h	RO	Line Buffer Self Test Result Status	-
* FAh	R/W	Debug/Test Mode Control	00h

Input Image Vertical Active Line Start - Low (Address 00h) (R/W)

It defines the low byte of the start position of the Vertical Active Window.

D7-0 IV_ACT_START[7:0]

Input Image Vertical Active Line Start - High (Address 01h) (R/W)

It defines the high byte of the start position of the Vertical Active Window.

D7-3 Reserved

D2-0 IV_ACT_START[10:8]

Input Image Vertical Active Lines - Low (Address 02h) (R/W)

It defines the low byte of the number of active lines of the Vertical Active Window.

D7-0 IV_ACT_LEN[7:0]

Input Image Vertical Active Lines - High (Address 03h) (R/W)

It defines the high byte of the number of active lines of the Vertical Active Window.

D7-3 Reserved

D2-0 IV_ACT_LEN[10:8]

Input Image Horizontal Active Pixel Start - Low (Address 04h) (R/W)

It defines the low byte of the start position of the Horizontal Active Window.

D7-0 IH_ACT_START[7:0]

Input Image Horizontal Active Pixel Start - High (Address 05h) (R/W)

It defines the high byte of the start position of the Horizontal Active Window.

D7-3 Reserved

D2-0 IH_ACT_START[10:8]

Input Image Horizontal Active Pixels - Low (Address 06h) (R/W)

It defines the low byte of the number of active pixels of the Horizontal Active Window.

D7-0 IH_ACT_WIDTH[7:0]

Input Image Horizontal Active Pixels - High (Address 07h) (R/W)

It defines the high byte of the number of active pixels of the Horizontal Active Window.

D7-3 Reserved

D2-0 IH_ACT_WIDTH[10:8]

Input Image Control Register 0 (Address 10h) (R/W)

D7	Horizontal Sampling Point Reference 0: from Input HSYNC; 1: from Input HREF (only for Video Decoder)
D6	Input YCBCR Format 0: 4-2-2 1: 4-1-1
D5	Digital RGB 6 bit Mode 0: 8 bits; 1: 6 bits
D4	Digital RGB Mode Select 0: RGB Input from ADC; 1: RGB Input from Panel Link
D3	Input Image Format 0: RGB888; 1: YCBCR
D2	Reserved
D1	Input Image Source 0: from Graphic source through ADC; 1: from Video source through Video Decoder like SAA7111A
D0	Reserved

Input Image Control Register 1 (Address 11h) (R/W)

D7-4	Reserved
D3	CCIR656 mode Enable 0: Disable; 1: Enable
D2	CCIR656 VDE Select 0: from Internal Programming; 1: from Internal Self-Decode
D1-0	Reserved

Input Image Control Register 2 (Address 12h) (R/W)

D7	Input ODD Field Invert 0: Normal; 1: Invert
D6	External Input Interlace Select 0: Non-interlace; 1: Interlace
D5	External Input VSYNC Polarity 0: Active Low; 1: Active High
D4	External Input HSYNC Polarity 0: Active Low;

1: Active High

D3 Input ODD Field Source
0: from Internal Detection;
1: from External pin

D2 Input Interlace Source
0: from Internal detection;
1: from Register setting (D6)

D1 Input VSYNC Polarity Source
0: from Internal detection;
1: from Register setting (D5)

D0 Input HSYNC Polarity Source
0: from Internal detection;
1: from Register setting (D4)

Input Image Control Register 3 (Address 13h) (R/W)

D7 Active Position Area for Auto Position in TMDS
0: from Internal Detection;
1: from External Data Enable (TDIE)

*D6-4 Data Enable (TDIE) Delay in TMDS
000: No delay;
001: +3 clocks delay;
010: -3 clocks delay;
011: Reserved;
100: +1 clock delay;
101: +2 clocks delay;
110: -2 clocks delay;
111: -1 clock delay

D3-2 Reserved

D1 Input Vertical Timing based on VSYNC
0: Leading Edge;
1: Trailing Edge

D0 Input Horizontal Timing based on HSYNC
0: Leading Edge;
1: Trailing Edge

Input Image Control Register 4 (Address 14h) (R/W)

D7 Input ODD Field Detection Point
0: at the start of VSYNC pulse;
1: at the end of VSYNC pulse

D6-5 Reserved

D4 Input Image CBCR Order Swap
0: Normal;
1: Swap

D3 Reserved

*D2	Input HSYNC Pulse Cut 0: Normal; 1: Cut Short Input HSYNC Pulse
*D1-0	Input H/V SYNC Sample Mode 00: Filtered by a de_bounced filter; 01: Sampled by REFCLK to SYNC Processor, sampled by IDCLK to others; 1x: Pass Through

Input Image Control Register 5 (Address 15h) (R/W)

D7	Horizontal Pixel Valid Select 0: from Internal Programming; 1: from External HREF
D6	Reserved
D5	External Display Enable Select 0: Disable; 1: Enable
D4-3	Reserved
*D2	Input Clock IDCLK Mode 0: Internal IDCLK can only tune Invert; 1: Internal IDCLK can tune Invert, Delay and Duty cycles
*D1	Pixclk1 Adjustment Enable.
*D0	Input Sample Clock ADCCLK1 Mode 0: Internal ADCCLK1 can only tune Invert; 1: Internal ADCCLK1 can tune Invert, Delay and Duty cycles

Input Image Control Register 6 (Address 16h) (R/W)

D7	Input Rin-ports and Bin-ports Swap 0: Normal; 1: Swap
D6	Bit Order in Port A0: Normal; 1: Reverse
*D5	Flush Line Buffer Enable 0: Disable; 1: Enable
D4-3	Reserved
D2	ADC HS Polarity when D1=1 0: Active Low; 1: Active High
D1	Raw HS path Enable 0: Disable; 1: Enable
D0	Reserved

***Input Invert Control (Address 17h) (R/W)**

D7	Reserved
*D6	Internal ADCCLK1 Tuning 0: Disable; 1: Enable
D5	Input VSYNC Invert 0: Normal; 1: Invert
D4	Input HSYNC Invert 0: Normal; 1: Invert
D3	Reserved
D2	Input Clock IDCLK Invert 0: Normal; 1: Invert
D1	Reserved
*D0	Input Sample Clock ADCCLK1 from PC GRAPHIC Invert 0: Normal; 1: Invert

***Input Delay Control 0 (Address 18h) (R/W)**

D7-4	Reserved
*D3-0	Input Clock IDCLK Delay Adjustment 16 steps to change, each of them is 1ns delay/step.

***Input Delay Control 1 (Address 19h) (R/W)**

*D7-6	Input Pixel Delay Adjustment 4 steps to adjust, Typical 0.2ns/step
*D5-4	External Data Enable Delay Adjustment 4 steps to adjust, Typical 0.2ns/step
*D3-0	Input Sample Clock ADCCLK1 Delay Adjustment 16 steps to change, each of them is 1ns delay/step

***Input Delay Control 2 (Address 1Ah) (R/W)**

*D7-4	Input VSYNC Delay Adjustment 1111: 7 IDCLKs delay; 1110: 6 IDCLKs delay; 1101: 5 IDCLKs delay; 1100: 4 IDCLKs delay; 1011: 3 IDCLKs delay;

1010: 2 IDCLKs delay;
1001: 1 IDCLK delay;
1000: No delay;
0111: 7ns gate delay;
0110: 6ns gate delay;
0101: 5ns gate delay;
0100: 4ns gate delay;
0011: 3ns gate delay;
0010: 2ns gate delay;
0001: 1ns gate delay;
0000: No delay

D3-0 Input HSYNC Delay Adjustment
16 steps to change, each of them is 1ns delay/step

Input HS Pulse Width Forward Extend (Address 1Ch) (R/W)

D7-0 Input HS Pulse Width Forward Extend by IDCLK
HS1FWEXT[7:0]: Used when Interlace First/Second Field Detection.

Input HS Pulse Width Backward Extend (Address 1Dh) (R/W)

D7-0 Input HS Pulse Width Backward Extend by IDCLK
HS1BWEXT[7:0]: Used when Interlace First/Second Field Detection.

***Input Miscellaneous Control (Address 1Eh) (R/W)**

D7 Reserved

*D6-2 Internal VIU Debug Bus Select

*D1 VIU Counter Test Enable
0: Normal;
1: Enable

*D0 VIU Test Enable
0: Normal;
1: Enable

Input Image Status Register (Address 1Fh) (RO)

D7 Display VSYNC Monitor
Show Display VSYNC signal directly.

D6 Input VSYNC Monitor
Show Input VSYNC signal directly.

D5 External Input Interlace Status
0: Non-interlace;
1: Interlace

D4 Extracted CVSYNC Present Status
0: Not Present;
1: Present

D3	External Input VSYNC Present Status 0: Not Present; 1: Present
D2	External Input HSYNC Present Status 0: Not Present; 1: Present
D1	External Input VSYNC Polarity Status 0: Active Low; 1: Active High
D0	External Input HSYNC Polarity Status 0: Active Low; 1: Active High

Input Image Back Porch Guard Band (Address 20h) (R/W)

D7-0	Input Image Back Porch Guard Band by IDCLK HBPGB[7:0]: Used in Auto Position detection to mask out unwanted data.

Input Image Front Porch Guard Band (Address 21h) (R/W)

D7-0	Input Image Front Porch Guard Band by IDCLK HFPGB[7:0]: Used in Auto Position detection to mask out unwanted data.

***Frame Sync Control (Address 28h) (R/W)**

D7-6	Reserved
*D5	Lock Counter Select 0: from STACOUNT; 1: from VALCOUNT
*D4	Interlace Second Field Shift One line Enable 0: No Shift; 1: Shift One Line
*D3	Interlace Horizontal Lock Event Select 0: Normal; 1: Only Lock on the First Field
*D2	Horizontal Lock Event Function ON 0: OFF; 1: ON
D1-0	Reserved

***NFB Display VSYNC Control (Address 29h) (R/W)**

It defines Display VSYNC passed through from Input VSYNC tuning control in NFB mode.

D7-5	Reserved
*D4	Input VSYNC pass through to Output VSYNC Enable

0: Disable;
1: Enable

D3 Reserved

*D2-0 Output VSYNC delay
000: No delay;
001: 1 line delay;
010: 2 lines delay;
011: 3 lines delay;
100: 4 lines delay;
101: 5 lines delay;
110: 6 lines delay;
111: 7 lines delay

Input Image Vertical Lock Position - Low (Address 2Ch) (R/W)

It defines the low byte of the number of input lines where Display image timing synchronizes the input image source.

D7-0 IPV_LOCK_POS[7:0]

Input Image Vertical Lock Position - High (Address 2Dh) (R/W)

It defines the high byte of the number of input lines where Display image timing synchronizes the input image source.

D7-3 Reserved

D2-0 IPV_LOCK_POS[10:8]

Input Image Horizontal Lock Position - Low (Address 2Eh) (R/W)

It defines the low byte of the number of input pixel clocks where Display image timing synchronizes the input image source.

D7-0 IPH_LOCK_POS[7:0]

Input Image Horizontal Lock Position - High (Address 2Fh) (R/W)

It defines the high byte of the number of input pixel clocks where Display image timing synchronizes the input image source.

D7-3 Reserved

D2-0 IPH_LOCK_POS[10:8]

Auto Calibration Control 0 (Address 30h) (R/W)

D7 Pixel Grab Ready Flag (RO)
0: Ready;
1: Not Ready

D6	Pixel Grab Update Enable 0: Stop updating; 1: Continue updating
D5	Threshold Select Used in Histogram mode or MIN/MAX mode. 0: High bound / MAX; 1: Low bound / MIN
D4	Phase Calibration Method Select 0: MYSON proprietary method; 1: Difference Value method
D3-2	Auto Calibration Modes Select The measured value is available one item at a time, selected as shown: 00: Phase Calibration Mode; 01: Histogram Mode; 10: MIN/MAX Mode; 11: Pixel Grab Mode
D1	Auto Calibration Burst Mode Enable (except Pixel Grab Mode) 0: Single Mode; 1: Burst Mode
D0	Auto Calibration Enable (W) (except Pixel Grab Value) 0: Disable; 1: Enable Auto Calibration Ready Flag (R) 0: Ready; 1: Not Ready

Auto Calibration Control 1 (Address 31h) (R/W)

*D7	Pixel Grab Select 0: Single Pixel Grab; 1: Dual Pixel Grab
D6-3	Reserved
D2-0	Mask LSBs of Input Image Select 000: No Mask; 001: Mask bit0; 010: Mask bit0,1; 011: Mask bit0,1,2; 100: Mask bit0,1,2,3; 101: Mask bit0,1,2,3,4; 110: Mask bit0,1,2,3,4,5; 111: Mask bit0,1,2,3,4,5,6

Auto Calibration RED Value - Byte 0 (Address 34h) (RO)

It states the byte 0 of the number of Phase Calibration RED value in one frame or the byte 0 of the number of Histogram Red value in one frame or the Pixel Grab RED value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[7:0]

Auto Calibration RED Value - Byte 1 (Address 35h) (RO)

It states the byte 1 of the number of Phase Calibration RED value in one frame or the byte 1 of the number of Histogram Red value in one frame or the Pixel Grab GREEN value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[15:8]

Auto Calibration RED Value - Byte 2 (Address 36h) (RO)

It states the byte 2 of the number of Phase Calibration RED value in one frame or the byte 2 of the number of Histogram Red value in one frame or the Pixel Grab BLUE value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[23:16]

Auto Calibration RED Value - Byte 3 (Address 37h) (RO)

It states the byte 3 of the number of Phase Calibration RED value in one frame.

D7-6 Reserved

D5-0 CALVAL_R[29:24]

Auto Calibration GREEN Value - Byte 0 (Address 38h) (RO)

It states the byte 0 of the number of Phase Calibration GREEN value in one frame or the byte 0 of the number of Histogram GREEN value in one frame or the Pixel Grab RED value in one frame of Non_interlace mode or SECOND field of Interlace mode.

D7-0 CALVAL_G[7:0]

Auto Calibration GREEN Value - Byte 1 (Address 39h) (RO)

It states the byte 1 of the number of Phase Calibration GREEN value in one frame or the byte 1 of the number of Histogram GREEN value in one frame or the Pixel Grab GREEN value in one frame of Non_interlace mode or SECOND field of Interlace mode.

D7-0 CALVAL_G[15:8]

Auto Calibration GREEN Value - Byte 2 (Address 3Ah) (RO)

It states the byte 2 of the number of Phase Calibration GREEN value in one frame or the byte 2 of the number of Histogram GREEN value in one frame or the Pixel Grab BLUE value in one frame of Non_interlace mode or SECOND field of Interlace mode.

D7-0 CALVAL_G[23:16]

Auto Calibration GREEN Value - Byte 3 (Address 3Bh) (RO)

It states the byte 3 of the number of Phase Calibration GREEN value in one frame.

D7-6 Reserved

D5-0 CALVAL_G[29:24]

Auto Calibration BLUE Value - Byte 0 (Address 3Ch) (RO)

It states the byte 0 of the number of Phase Calibration BLUE value in one frame or the byte 0 of the number of Histogram BLUE value in one frame or the MIN/MAX RED value in one frame.

D7-0 CALVAL_B[7:0]

Auto Calibration BLUE Value - Byte 1 (Address 3Dh) (RO)

It states the byte 1 of the number of Phase Calibration BLUE value in one frame or the byte 1 of the number of Histogram BLUE value in one frame or the MIN/MAX GREEN value in one frame.

D7-0 CALVAL_B[15:8]

Auto Calibration BLUE Value - Byte 2 (Address 3Eh) (RO)

It states the byte 2 of the number of Phase Calibration BLUE value in one frame or the byte 2 of the number of Histogram BLUE value in one frame or the MIN/MAX BLUE value in one frame.

D7-0 CALVAL_B[23:16]

Auto Calibration BLUE Value - Byte 3 (Address 3Fh) (RO)

It states the byte 3 of the number of Phase Calibration BLUE value in one frame.

D7-6 Reserved

D5-0 CALVAL_B[29:24]

Pixel Grab V Reference Position - Low (Address 40h) (R/W)

It states the low byte of Vertical Reference Position in Pixel Grab Mode.

D7-0 VGRAB_POS[7:0]

Pixel Grab V Reference Position - High (Address 41h) (R/W)

It states the high byte of Vertical Reference Position in Pixel Grab Mode.

D7-3 Reserved

D2-0 VGRAB_POS[10:8]

Pixel Grab H Reference Position - Low (Address 42h) (R/W)

It states the low byte of Horizontal Reference Position in Pixel Grab Mode.

D7-0	HGRAB_POS[7:0]

Pixel Grab H Reference Position - High (Address 43h) (R/W)

It states the high byte of Horizontal Reference Position in Pixel Grab Mode.

D7-3	Reserved
D2-0	HGRAB_POS[10:8]

Histogram Reference Color - RED (Address 44h) (R/W)

It states the Histogram Reference RED Color in Histogram Mode.

D7-0	HIST_R[7:0]

Histogram Reference Color - GREEN (Address 45h) (R/W)

It states the Histogram Reference GREEN Color in Histogram Mode.

D7-0	HIST_G[7:0]

Histogram Reference Color - BLUE (Address 46h) (R/W)

It states the Histogram Reference BLUE Color in Histogram Mode.

D7-0	HIST_B[7:0]

SYNC Processor Control (Address 48h) (R/W)

D7-2	Reserved
D1-0	SYNC Source 00: from H/V SYNC; 01: from CVSYNC (Composite SYNC); 1x: Auto switch to CVSYNC when CVSYNC is present, but VSYNC not.

Auto Position Control (Address 49h) (R/W)

D7-2	Reserved
D1	Auto Position Burst Mode Enable 0: Single Mode; 1: Burst Mode
D0	Auto Position Enable (W) 0: Disable; 1: Enable

Auto Position Ready Flag (R)
0: Ready;
1: Not Ready

Auto Position Reference Color - RED (Address 4Ah) (R/W)

It defines the red component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_RED[7:0]

Auto Position Reference Color - GREEN (Address 4Bh) (R/W)

It defines the green component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_GREEN[7:0]

Auto Position Reference Color - BLUE (Address 4Ch) (R/W)

It defines the blue component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_BLUE[7:0]

Clamp Pulse Control 0 (Address 4Eh) (R/W)

D7 Clamp Pulse Mask
0: Normal;
1: Mask out Clamp Pulse

D6 Clamp Pulse Start Reference Edge
0: From Input HSYNC trailing edge;
1: From Input HSYNC leading edge

D5 Clamp Pulse output Polarity
0: Active High;
1: Active Low

D4-0 Clamp Pulse Start
Start of Clamp Pulse after the selected edge of Input HSYNC by Input DCLK.

Clamp Pulse Control 1 (Address 4Fh) (R/W)

D7 Clock Source for Clamp Pulse Generation;
0: from Input clock, IDCLK;
1: from OSC clock, REFCLK

D6-5 Reserved

D4-0 Clamp Pulse Width;
To Adjust Clamp Pulse Width by Input DCLK.

Input VS Period Count by REFCLK - Low (Address 50h) (RO)

It states the low byte of the number of REFCLK of the Vertical Sync period measurement.

D7-0 VSPRD[7:0]

Input VS Period Count by REFCLK - High (Address 51h) (RO)

It states the high byte of the number of REFCLK of the Vertical Sync period measurement.

D7-4 Reserved

D3-0 VSPRD[11:8]

Input V Back Porch Count by Input HS - Low (Address 52h) (RO)

It states the low byte of the number of lines between the end of VSYNC and the active image.

D7-0 VBPW[7:0]

Input V Back Porch Count by Input HS - High (Address 53h) (RO)

It states the high byte of the number of lines between the end of VSYNC and the active image

D7-3 Reserved

D2-0 VBPW[10:8]

Input V Active Image Count by Input HS - Low (Address 54h) (RO)

It states the low byte of the number of the active image lines.

D7-0 VACTW[7:0]

Input V Active Image Count by Input HS - High (Address 55h) (RO)

It states the high byte of the number of the active image lines

D7-3 Reserved

D2-0 VACTW[10:8]

Input V Total Image Count by Input HS - Low (Address 56h) (RO)

It states the low byte of the number of the total image lines.

D7-0 VTOTW[7:0]

Input V Total Image Count by Input HS - High (Address 57h) (RO)

It states the high byte of the number of the total image lines.

D7-3 Reserved

D2-0 VTOTW[10:8]

Input HS Period Count by REFCLK - Low (Address 58h) (RO)

It states the low byte of the number of REFCLKs of the Horizontal Sync period measurement.

D7-0 HSPRD[7:0]

Input HS Period Count by REFCLK - High (Address 59h) (RO)

It states the high byte of the number of REFCLKs of the Horizontal Sync period measurement.

D7-5 Reserved

D4-0 HSPRD[12:8]

Input H Back Porch Count by Input Pixel Clock -Low (Address 5Ah) (RO)

It states the low byte of the number of pixels between the end of HSYNC and the active image.

D7-0 HBPW[7:0]

Input H Back Porch Count by Input Pixel Clock -High (Address 5Bh) (RO)

It states the high byte of the number of pixels between the end of HSYNC and the active image.

D7-3 Reserved

D2-0 HBPW[10:8]

Input H Active Image Count by Input Pixel Clock-Low(Address 5Ch) (RO)

It states the low byte of the number of the Horizontal active image pixels.

D7-0 HACTW[7:0]

Input H Active Image Count by Input Pixel Clock-High(Address 5Dh)(RO)

It states the high byte of the number of the Horizontal active image pixels.

D7-3 Reserved

D2-0 HACTW[10:8]

Input H Total Image Count by Input Pixel Clock- Low (Address 5Eh) (RO)

It states the low byte of the number of the Horizontal total image pixels.

D7-0 HTOTW[7:0]

Input H Total Image Count by Input Pixel Clock- High (Address 5Fh) (RO)

It states the high byte of the number of the Horizontal total image pixels.

D7-3 Reserved

D2-0 HTOTW[10:8]

Display Vertical Total - Low (Address 60h) (R/W)

It defines the low byte of the number of lines per display frame.

D7-0 DV_TOTAL[7:0]

Display Vertical Total - High (Address 61h) (R/W)

It defines the high byte of the number of lines per display frame.

D7-3 Reserved

D2-0 DV_TOTAL[10:8]

Display Vertical SYNC End - Low (Address 62h) (R/W)

It defines the low byte of Vertical SYNC end position in lines.

D7-0 DV_SYNC_END[7:0]

Display Vertical SYNC End - High (Address 63h) (R/W)

It defines the high byte of Vertical SYNC end position in lines.

D7-3 Reserved

D2-0 DV_SYNC_END[10:8]

Note: Display Vertical SYNC Start is always equal 0.

Display Vertical Active Start - Low (Address 64h) (R/W)

It defines the low byte of Vertical Active region start position in lines.

D7-0 DV_ACT_START[7:0]

Display Vertical Active Start - High (Address 65h) (R/W)

It defines the high byte of Vertical Active region start position in lines.

D7-3 Reserved

D2-0 DV_ACT_START[10:8]

Display Vertical Active End - Low (Address 66h) (R/W)

It defines the low byte of Vertical Active region end position in lines.

D7-0 DV_ACT_END[7:0]

Display Vertical Active End - High (Address 67h) (R/W)

It defines the high byte of Vertical Active region end position in lines.

D7-3 Reserved

D2-0 DV_ACT_END[10:8]

***Display Vertical Border Start - Low (Address 68h) (R/W)**

It defines the low byte of Vertical Border start position in lines.

D7-0 DV_BOR_START[7:0]

***Display Vertical Border Start - High (Address 69h) (R/W)**

It defines the high byte of Vertical Border start position in lines.

D7-3 Reserved

D2-0 DV_BOR_START[10:8]

***Display Vertical Border End - Low (Address 6Ah) (R/W)**

It defines the low byte of Vertical Border end position in lines.

D7-0 DV_BOR_END[7:0]

***Display Vertical Border End - High (Address 6Bh) (R/W)**

It defines the high byte of Vertical Border end position in lines.

D7-3 Reserved

D2-0 DV_BOR_END[10:8]

Display Horizontal Total - Low (Address 70h) (R/W)

It defines the low byte of the number of display clock cycles per display line.

D7-0 DH_TOTAL[7:0]

Display Horizontal Total - High (Address 71h) (R/W)

It defines the high byte of the number of display clock cycles per display line.

D7-3 Reserved

D2-0 DH_TOTAL[10:8]

Display Horizontal SYNC End - Low (Address 72h) (R/W)

It defines the low byte of Horizontal SYNC end position in display clock cycles.

D7-0 DH_SYNC_END[7:0]

Display Horizontal SYNC End - High (Address 73h) (R/W)

It defines the high byte of Horizontal SYNC end position in display clock cycles.

D7-3 Reserved

D2-0 DH_SYNC_END[10:8]

Note: Display Horizontal SYNC Start is always equal 0.

Display Horizontal Active Start - Low (Address 74h) (R/W)

It defines the low byte of Horizontal Active region start position in display clock cycles.

D7-0 DH_ACT_START[7:0]

Display Horizontal Active Start - High (Address 75h) (R/W)

It defines the high byte of Horizontal Active region start position in display clock cycles.

D7-3 Reserved

D2-0 DH_ACT_START[10:8]

Display Horizontal Active End - Low (Address 76h) (R/W)

It defines the low byte of Horizontal Active region end position in display clock cycles.

D7-0 DH_ACT_END[7:0]

Display Horizontal Active End - High (Address 77h) (R/W)

It defines the high byte of Horizontal Active region end position in display clock cycles.

D7-3 Reserved

D2-0 DH_ACT_END[10:8]

***Display Horizontal Border Start - Low (Address 78h) (R/W)**

It defines the low byte of Horizontal Border start position in display clock cycles.

D7-0 DH_BOR_START[7:0]

***Display Horizontal Border Start - High (Address 79h) (R/W)**

It defines the high byte of Horizontal Border start position in display clock cycles.

D7-3 Reserved

D2-0 DH_BOR_START[10:8]

***Display Horizontal Border End - Low (Address 7Ah) (R/W)**

It defines the low byte of Horizontal Border end position in display clock cycles.

D7-0 DH_BOR_END[7:0]

***Display Horizontal Border End - High (Address 7Bh) (R/W)**

It defines the high byte of Horizontal Border end position in display clock cycles.

*D7 Auto-period Enable
0: Disable;
1: Enable

D6-3 Reserved

*D2-0 DH_BOR_END[10:8]

***NFB Timing Load Value (Address 7Eh)**

It defines the low byte of NFB Horizontal Counter load value.

The total additive(positive number)/subtractive(negative number) pixels in one frame.

It is 2's complement value.

*D7-0 DH_NFB_LD_VAL[7:0]

NFB Timing Control (Address 7Fh)

It defines the NFB timing setting and high byte of NFB Horizontal Counter load value.

D7 Free Running mode Select
0: Normal;
1: Free Running

D6-4 NFB Synchronization mode
000: Delay mode. Output HSYNC trimmed in output VSYNC and VDE issued on next HSYNC when Lock event occurs;
010: Immediate mode. Output HSYNC trimmed immediately and VDE issued on next HSYNC when Lock event occurs;
110: Early mode. Output HSYNC trimmed immediately and VDE issued immediately when Lock event occurs.

*D3-0	DH_NFB_LD_VAL[11:8]

Output Image Control Register 0 (Address 88h) (R/W)

D7-5	RGB Sharpness Factor Select 000: Disable; 001: 1/16; 010: 2/16; 011: 3/16; 100: 4/16; 101: 5/16; 110: 6/16; 111: 8/16
D4	OUTPUT port MSB / LSB change 0: No Exchange; 1: Exchange
D3	Auto Black Enable 0: Disable; 1: Enable
D2	Output Pixel 18 bit RGB Mode Select 0: 24 bit RGB; 1: 18 bit RGB
D1	Output Dual Pixel Data Exchange 0: Normal; 1: Exchange
D0	Reserved // Output Dual Pixel Select; //0: Dual Pixel; //1: Single Pixel

Output Image Control Register 1 (Address 89h) (R/W)

D7	RGB Smooth Control Enable 0: Disable; 1: Enable
D6	Reserved
D5	RGB Brightness Control Enable 0: Disable; 1: Enable
D4	RGB Gain Control Enable 0: Disable; 1: Enable
D3-2	Pattern Generation Type Select 00: Single Color; 01: Vertical Line Moire; 10: Horizontal Line Moire; 11: Dot Moire

*D1	Border Window Function (Only valid in Free Running mode Reg. 7Fh/D7=1) 0: OFF; 1: ON
D0	Output Blank Screen 0: Normal; 1: Output Pixel masked as BLACK color

Output Image Control Register 2 (Address 8Ah) (R/W)

D7	Reserved
D6	Temporal Dithering Enable 0: Static Dithering; 1: Temporal Dithering
D5	Reserved
D4	Dithering Enable; 0: Disable; 1: Enable
D3	Color Gain Control Resolution Select 0: 8-bit Resolution; 1: 9-bit Resolution
D2	8-bit or 10-bit Gamma Table 0: 8-bit; 1: 10-bit
D1	Gamma Table R/W Access Enable 0: Disable; 1: Enable
D0	Gamma Correction Function 0: OFF; 1: ON

Color Gain Control - RED (Address 90h) (R/W)

It can be used to adjust the gain of RED component of the Display Image.

D7-0	RGAIN[7:0] 0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Gain Control - GREEN (Address 91h) (R/W)

It can be used to adjust the gain of GREEN component of the Display Image.

D7-0 GGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Gain Control - BLUE (Address 92h) (R/W)

It can be used to adjust the gain of BLUE component of the Display Image.

D7-0 BGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Brightness Control - RED (Address 93h) (R/W)

It can be used to adjust the brightness of RED component of the Display Image.

D7-0 RBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

Color Brightness Control - GREEN (Address 94h) (R/W)

It can be used to adjust the brightness of GREEN component of the Display Image.

D7-0 GBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

Color Brightness Control - BLUE (Address 95h) (R/W)

It can be used to adjust the brightness of BLUE component of the Display Image.

D7-0 BBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

***Border Window Color - RED (Address 96h) (R/W)**

When the Display Image is not expanded to full screen, it can be specified as the RED component of the border color.

D7-0 BCR[7:0]

***Border Window Color - GREEN (Address 97h) (R/W)**

When the Display Image is not expanded to full screen, it can be specified as the GREEN component of the border color.

D7-0 BCG[7:0]

***Border Window Color - BLUE (Address 98h) (R/W)**

When the Display Image is not expanded to full screen, it can be specified as the BLUE component of the border color.

D7-0 BCB[7:0]

***Dithering Table Data Port (Address 9Eh) (R/W)**

Since the Dithering Table is downloadable, this data port is the entry address.

D7-0 DITHER_REG[7:0]

Gamma Table Data Port (Address 9Fh) (R/W)

Since the Gamma Table is downloadable, this data port is the entry address.

D7-0 GAMMA_PORT[7:0]

OSD Control Registers 0 (Address A0h) (R/W)

D7 OSD Output Clock Select
0: from Internal Display Dot Clock;
1: from Internal Display Dot Clock x 2

D6 OSD Output VS Invert
0: Normal;
1: Invert

*D5-4 OSD Output VS Select
00: Display VDE, when Reg. 89h/D1=0;
Display VBDE, when Reg. 89h/D1=1;
01: Display VS;
1x: Input VS

D3 OSD Function
0: OFF;
1: ON

D2 Reserved

D1-0 OSD TYPE Select
00: OSDRGB = {R0000000, G0000000, B0000000};
01: OSDRGB = {RR000000, GG000000, BB000000};
10: OSDRGB = {RRRR0000, GGGG0000, BBBB0000};
11: OSDRGB = {RRRRRRRR, GGGGGGGG, BBBBBBBB};
R = OSDR, G = OSDG, B = OSDB

OSD Control Register 1 (Address A1h) (R/W)

D7 OSD Output HS Invert;
0: Normal;
1: Invert.

D6 OSD Output DCLK Invert;
0: Normal;
1: Invert.

D5-4 OSD Output HS Delay
4 steps to change, each of them is 1ns delay/step.

D3 OSD Input Data Sample Clock Invert
0: Normal;
1: Invert.

D2-0	OSD Input Data Sample Clock Delay 8 steps to change, each of them is 1ns delay/step.

OSD Control Register 2 (Address A2h) (R/W)

D7-4	Reserved
D3-0	OSD Output Clock Delay 16 steps to change, each of them is 1ns delay/step.

OSD Control Register 3 (Address A3h) (R/W)

D7	OSD Intensity Pulse Polarity Invert 0: Disable; 1: Enable
D6	Reserved
D5	OSD Transparent Control Enable 0: Disable; 1: Enable
D4	OSD Weighting Control Enable 0: Disable; 1: Enable
D3-0	OSD Weighting Factor (N) Select N = 0 ~ 15 (D [3:0] = 0000 ~ 1111) RGB Weighting Factor = (N+1)/16; D4=0: OSD Weighting Factor = 1; D4=1: OSD Weighting Factor = (15-N)/16

Output Invert Control (Address A4h) (R/W)

D7	Reserved
D6	RGB Data Invert Enable 0: Disable; 1: Enable
D5	Display DCLKH Invert 0: Normal; 1: Invert
D4	Display DCLK Invert 0: Normal; 1: Invert
D3	Reserved
D2	Display Data Enable (DDEN) Invert 0: Normal; 1: Invert
D1	Display VSYNC Invert 0: Normal;

1: Invert

D0 Display HSYNC Invert
0: Normal;
1: Invert

Output Tri_state Control (Address A5h) (R/W)

D7 Display Data R2OUT, G2OUT, B2OUT Output Disable
0: Normal;
1: Tri_stated

D6 Display Data R1OUT, G1OUT, B1OUT Output Disable
0: Normal;
1: Tri_stated

D5 Display DCLKH Output Disable
0: Normal;
1: Tri_stated

D4 Display DCLK / Display VSYNC / Display HSYNC / Display data enable Output Disable
0: Normal;
1: Tri_stated

D3 OSD OCLK / OVSYNC / OHSYNC Output Disable
0: Normal;
1: Tri_stated

D2-D0 Reserved

Output Clocks Delay Adjustment (Address A6h) (R/W)

D7-4 Display DCLKH delay adjustment
16 steps to adjust, Typical 1ns delay/step

D3-0 Display DCLK delay adjustment
16 steps to adjust, Typical 1ns delay/step

Output Clocks Duty Cycle Adjustment (Address A7h) (R/W)

D7 Display DCLKH duty cycle Increase/Decrease
0: Decrease;
1: Increase

D6-4 Display DCLKH duty cycle adjustment
8 steps to adjust, Typical 0.5ns delay/step

D3 Display DCLK duty cycle Increase/Decrease
0: Decrease;
1: Increase

D2-0 Display DCLK duty cycle adjustment
8 steps to adjust, Typical 0.5ns delay/step

***Display Line Buffer Data Sample Adjustment (Address A8h) (R/W)**

*D7	Reg. AEh, AFh Selection 0: Report Output Horizontal Total Residue Number; 1: Report Output Vertical Total Counter Value
D6	Reserved
*D5	Display Vsync Mode 0: Normal; 1: Delay 1 clock
D4-0	Reserved

Output Miscellaneous Control (Address A9h) (R/W)

D7	Second field Line Buffer Overflow status for Interlace input (RO) 0: Not Overflow; 1: Overflow
D6	Second field Line Buffer Underflow status for Interlace input (RO) 0: Not Underflow; 1: Underflow
D5	First field Line Buffer Overflow status for Interlace input or Line buffer Overflow status for Non-interlace input (RO) 0: Not Overflow; 1: Overflow
D4	First field Line Buffer Underflow status for Interlace input or Line Buffer Overflow status for Non-interlace input (RO) 0: Not Underflow; 1: Underflow
D3	Auto Output Horizontal Total Calculation Start (W) 0: Disable; 1: Enable Auto Output Horizontal Total Calculation Ready Flag (R) 0: Ready; 1: Not Ready
*D2-0	Internal VOU Debug Bus Select

Output Vertical Active Line Number - Low (Address AAh) (R/W)

It defines the low byte of Output Vertical Active Line Number -1, only used for getting the values of Reg. ACh and ADh.

D7-0	OVDE[7:0]

Output Vertical Active Line Number - High (Address ABh) (R/W)

It defines the high byte of Output Vertical Active Line Number -1, only used for getting the values of Reg. ACh and ADh.

D2-0 OVDE[10:8]

Output Horizontal Total Pixel Number - Low (Address ACh) (RO)

It states the low byte of Output Horizontal Total Pixel Number.

D7-0 OHTOT[7:0]

Output Horizontal Total Pixel Number - High (Address ADh) (RO)

It states the high byte of Output Horizontal Total Pixel Number, or output vertical total counter value, setting by RegA8[7].

D2-0 OHTOT[10:8]

Output Horizontal Total Residue Number - Low (Address AEh) (RO)

It states the low byte of Output Horizontal Total Pixel Residue Number, or output vertical total counter value, setting by RegA8[7].

D7-0 OHTOT_RES[7:0]

Output Horizontal Total Residue Number - High (Address AFh) (RO)

It states the high byte of Output Horizontal Total Pixel Residue Number.

D7-2 Reserved

D2-0 OHTOT_RES[10:8]

Zoom Control Register 0 (Address B0h) (R/W)

D7 Reserved

D6-4 Vertical Scale Select
0xx: PASS mode;
10x: DUPLICATE mode;
110: BILINEAR mode;
111: INTERPOLATION TABLE mode
(Down Scaling Mode: Enable Average the neighbor lines)

D3 Reserved

D2-0 Horizontal Scale Select
0xx: PASS mode;
10x: DUPLICATE mode;
110: BILINEAR mode;
111: INTERPOLATION TABLE mode

Zoom Control Register 1 (Address B1h) (R/W)

D7-1 Reserved

D0 Interpolation Table R/W Access Enable
0: Disable;
1: Enable

Zoom Vertical Scale Ratio – Low (Address B4h) (R/W)

It defines the low byte of vertical scale ratio value for scale up.

D7-0 ZVSF[7:0]

Zoom Vertical Scale Ratio - High (Address B5h) (R/W)

It defines the high byte of vertical scale ratio value for scale up.

D7-0 ZVSF[15:8]

ZVSF = CEIL[(input_height – 1)/ (output_height – 1)* 2^{16}]

Zoom Horizontal Scale Ratio - Low (Address B6h) (R/W)

It defines the low byte of horizontal scale ratio value for scale up.

D7-0 ZHSF[7:0]

Zoom Horizontal Scale Ratio - High (Address B7h) (R/W)

It defines the high byte of horizontal scale ratio value for scale up.

D7-0 ZHSF[15:8]

ZHSF = CEIL[(input_width – 1)/ (output_width – 1)* 2^{16}]

Interpolation Table Data Port (Address BFh) (R/W)

It defines the entry address of the Interpolation table data port.

D7-0 TFPORT[7:0]

Host Control Register 1 (Address C1h) (R/W)

D7 Reserved

D6 I2C Bus Address No Increment
0: Normal;
1: No Increment

D5 Double Buffer load Select
0: Immediately;
1: Delay to Display VSYNC

D4 Registers Double Buffer function Enable
0: Disable;

1: Enable

D3-2 Reserved

D1 Display Registers Double Buffer Load (WO)

D0 Input Registers Double Buffer Load (WO)

***Host Fill RED Color (Address C6h) (R/W)**

It defines Fill Red color for Line Buffer Flush defined in Reg. 16h/D5.

D7-0 HFR[7:0]

***Host Fill GREEN Color (Address C7h) (R/W)**

It defines Fill Green color for Line Buffer Flush defined in Reg. 16h/D5.

D7-0 HFG[7:0]

***Host Fill BLUE Color (Address C8h) (R/W)**

It defines Fill Blue color for Line Buffer Flush defined in Reg. 16h/D5.

D7-0 HFB[7:0]

Host Access Mode Status (Address CBh) (RO)

D7-1 Reserved

D0 Host Access Mode
0: 2-wire Serial mode (IIC);
1: 8-bit Parallel mode

Clock Synthesizer Control Register (Address E0h) (R/W)

D7 External Display Clock Selection
0: External Display Clock 1;
1: External Display Clock 2

D6-5 Reserved

*D4 Internal Display Clock Select
It is used for two purposes: one for better clock duty cycle, the other for lower frequency testing in Tester.
0: VCG DCLK;
1: VCG DCLK / 2

D3 Reserved

D2 Display Clock Source
0: Internal Display Clock;
1: External Reference Clock

D1	Reserved
D0	Display Clock Synthesizer Enable 0: Enable; 1: Disable

Clock Synthesizer Value Load (Address E1h) (WO)

D7-1	Reserved
D0	Display Clock Synthesizer Value Load (WO)

Display Clock Synthesizer N Value (Address E2h) (R/W)

D7-0	Display Clock Synthesizer N value

Display Clock Synthesizer M Value (Address E3h) (R/W)

D7-0	Display Clock Synthesizer M value

Clock Synthesizer R Value (Address E6h) (R/W)

*D7-4	PLL Test mode Control
D3-2	Reserved
D1-0	Display Clock Synthesizer R value 00: Not divided; 01: Divided by 2; 10: Divided by 4; 11: Divided by 8

SYNC Interrupt Flag Control (Address E8h) (R)

It contains the status of SYNC Interrupts.

D7	Display VSYNC Pulse Interrupt Status 0: No Display VSYNC pulse detected; 1: Any Display VSYNC pulse detected
D6	Input VSYNC Pulse Interrupt Status 0: No Input VSYNC pulse detected; 1: Any Input VSYNC pulse detected
D5	VSYNC Presence Change Status 0: No Change; 1: Change
D4	HSYNC Presence Change Status 0: No Change; 1: Change

D3 VSYNC Polarity Change Status
0: No Change;
1: Change

D2 HSYNC Polarity Change Status
0: No Change;
1: Change

D1 VSYNC Frequency Change Status
0: No Change;
1: Change

D0 HSYNC Frequency Change Status
0: No Change;
1: Change

SYNC Interrupt Flag Control (Address E8h) (W)

It is used to clear the corresponding SYNC interrupt signal when Software finishes serving the interrupt service routine.

D7 Clear Display VSYNC Pulse Interrupt Enable
0: Disable;
1: Enable

D6 Clear Input VSYNC Pulse Interrupt Enable
0: Disable;
1: Enable

D5 Clear VSYNC Presence Change Interrupt Enable
0: Disable;
1: Enable

D4 Clear HSYNC Presence Change Interrupt Enable
0: Disable;
1: Enable

D3 Clear VSYNC Polarity Change Interrupt Enable
0: Disable;
1: Enable

D2 Clear HSYNC Polarity Change Interrupt Enable
0: Disable;
1: Enable

D1 Clear VSYNC Frequency Change Interrupt Enable
0: Disable;
1: Enable

D0 Clear HSYNC Frequency Change Interrupt Enable
0: Disable;
1: Enable

General Interrupt Flag Control (Address E9h) (R)

It contains the status of General Interrupts.

D7-2	Reserved
D1	Auto Position Finish Status (valid for Single mode only) 0: Not Finished; 1: Finished
D0	Auto Calibration Finish Status (valid for Single mode only) 0: Not Finished; 1: Finished

General Interrupt Flag Control (Address E9h) (W)

It is used to clear the corresponding general interrupt signal when Software finishes serving the interrupt service routine.

D7-2	Reserved
D1	Clear Auto Position Finish Interrupt Enable 0: Disable; 1: Enable
D0	Clear Auto Calibration Finish Interrupt Enable 0: Disable; 1: Enable

SYNC Interrupt Enable Control (Address EAh) (R/W)

It is used to enable SYNC Interrupt function.

D7	Display VSYNC Pulse Interrupt Enable 0: Disable; 1: Enable
D6	Input VSYNC Pulse Interrupt Enable 0: Disable; 1: Enable
D5	VSYNC Presence Change Interrupt Enable 0: Disable; 1: Enable
D4	HSYNC Presence Change Interrupt Enable 0: Disable; 1: Enable
D3	VSYNC Polarity Change Interrupt Enable 0: Disable; 1: Enable
D2	HSYNC Polarity Change Interrupt Enable 0: Disable; 1: Enable
D1	VSYNC Frequency Change Interrupt Enable 0: Disable; 1: Enable
D0	HSYNC Frequency Change Interrupt Enable

0: Disable;
1: Enable

General Interrupt Enable Control (Address EBh) (R/W)

It is used to enable General Interrupt functions.

D7 Interrupt Output Polarity
0: Active High;
1: Active Low

D6-2 Reserved

D1 Auto Position Finish Interrupt Enable
0: Disable;
1: Enable

D0 Auto Calibration Finish Interrupt Enable
0: Disable;
1: Enable

HS Frequency Change Interrupt Compare (Address ECh) (R/W)

It is used to control Interrupt generation by comparing the frequency change value when Input HS Frequency changes.

D7-0 HSCMPREG[7:0]

***Device/Revision ID (Address F0h) (RO)**

D7-4 Device ID

D3-0 Revision ID

Power Management Control (Address F1h) (R/W)

D7 Reserved

D6 Power Down Gamma & Interpolation Table
0: Normal;
1: Power Down

D5 Reserved

D4 Power Down Line Buffers
0: Normal;
1: Power Down

D3 Regulator Power Down
0: Normal;
1: Power Down

D2 Mask REFCLK
0: Disable;
1: Enable

D1	Power Down all the clocks except REFCLK 0: Normal; 1: Power Down
D0	Software Reset Enable 0: Disable; 1: Enable

***Line Buffer Self Test Control (Address F8h) (R/W)**

It controls the operation of Line Buffer Self Test Mode.

D7-2	Reserved
D1	Line Buffer Self Test mode Finish Status (RO) 0: Finish; 1: Not Finish
D0	Line Buffer Self Test mode Enable 0: Disable; 1: Enable

***Line Buffer Self Test Result Status (Address F9h) (RO)**

It contains the status of Line Buffer Self Test Mode result.

D7-5	Reserved
D4	Line Buffer 4 Self Test mode Result Status (RO) 0: Success; 1: Fail
D3	Line Buffer 3 Self Test mode Result Status (RO) 0: Success; 1: Fail
D2	Line Buffer 2 Self Test mode Result Status (RO) 0: Success; 1: Fail
D1	Line Buffer 1 Self Test mode Result Status (RO) 0: Success; 1: Fail
D0	Line Buffer 0 Self Test mode Result Status (RO) 0: Success; 1: Fail

***Debug/Test Mode Control (Address FAh) (R/W)**

D7	Reserved
*D6-4	Internal Top Debug Bus Select
D3-2	Reserved

*D1	VCG Test mode Enable 0: Disable; 1: Enable
*D0	Debug mode Enable 0: Disable; 1: Enable

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Operation Voltage	3.0	3.3	3.6	V
Tamb	Operating Ambient Temperature	0		70	°C
Tstg	Storage Temperature	-55		150	°C

DC Electrical Characteristics for 3.3 V Operation

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		2.0			V
Vt-	Input Schmitt Trigger Low Voltage at pins SDA and SCK			1.0		
Vt+	Input Schmitt Trigger High Voltage at pins SDA and SCK			1.7		
VOL	Output Low Voltage				0.4	V
VOH	Output High Voltage		2.4			V
RI	Input Pull-up/Down Resistance	VIL = 0v or VIH = VCC		75		Kohm
ILI	Input Leakage Current		-10		10	uA
ILO	Output Leakage Current		-20		20	uA

AC CHARACTERISTICS

□ **Input Interface Timing**

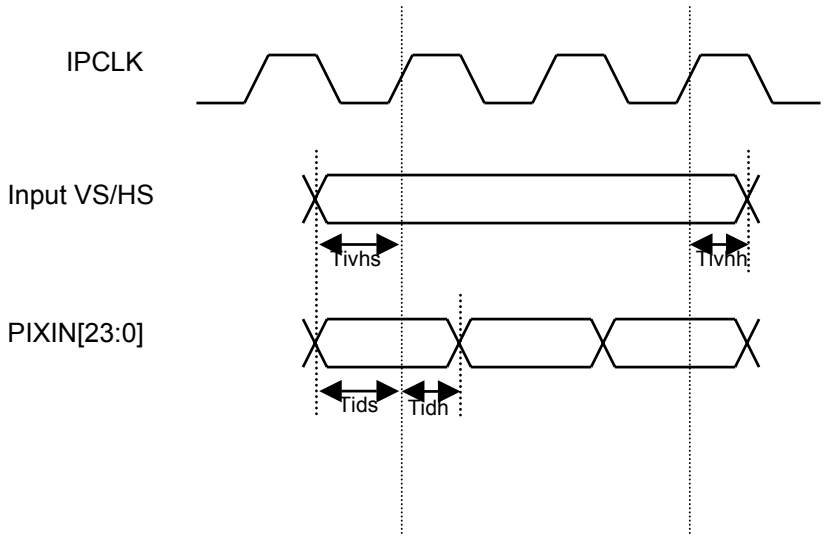


Figure-11 Input Interface Timing

Table-1 Input Interface Timing

Symbol	Parameter	Min	Max	Unit
Tids	Input Image Signal Setup Time for IPCLK	2		ns
Tidh	Input Image Signal Hold Time for IPCLK	3		ns
Tivhs	Input VSYNC/HSYNC Setup Time for IPCLK	2		ns
Tivhh	Input VSYNC/HSYNC Hold Time for IPCLK	3		ns

□

□ **Output Interface Timing**

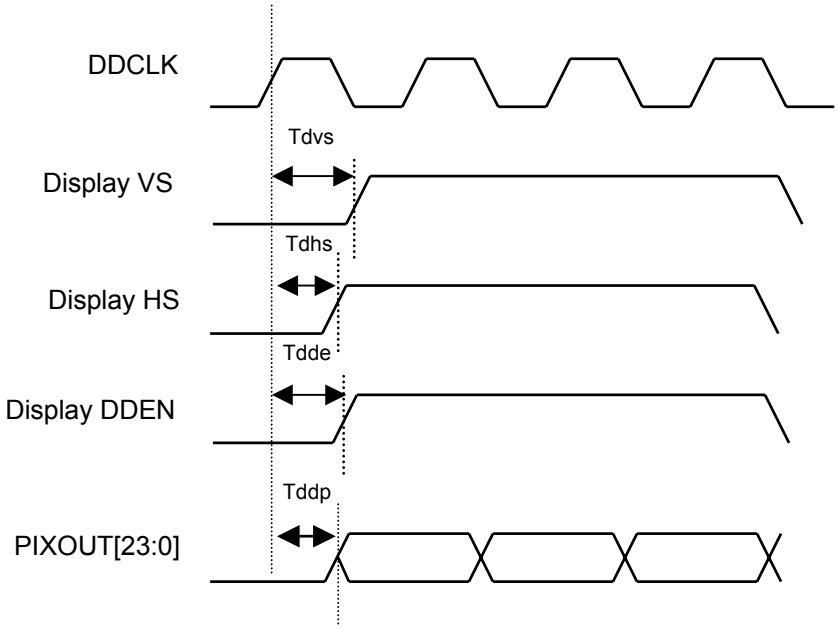


Figure-12 Output Interface Timing

Table-2 Output Interface Timing

Symbol	Parameter	Min	Max	Unit
Tdvs	Display VSYNC Output Delay to DDCLK	2		ns
Tdhs	Display HSYNC Output Delay to DDCLK	0.5		ns
Tdde	Display DDEN Output Delay to DDCLK	1		ns
Tddp	Display Data Output Delay to DDCLK	1.5		ns

Note: DDCLK phase can be adjusted relative to data and control outputs using the DDCLK_INV (Reg. A4h/D5-4) and DDCLK_DELAY[2:0] (Reg. A6h/D7-0) programming controls.

□ **OSD Interface Timing**

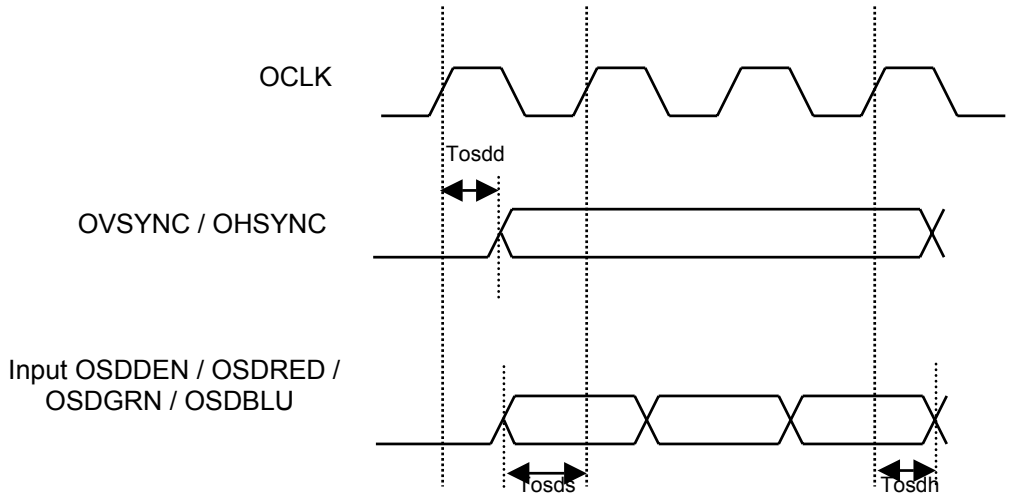


Figure-13 OSD Interface Timing

Table-3 OSD Interface Timing

Symbol	Parameter	Min	Max	Unit
Tosdd	OSD VS / HS Output Delay to OCLK	2		ns
Tosds	OSD Signal Input Setup Time for OCLK	5.5		ns
Tosdh	OSD Signal Input Hold Time for OCLK	0		ns

Note: OCLK phase can be adjusted using OCLK_INV (Reg. A1h/D3) programming control and OHSYNC phase can be adjusted using OHSYNC_DELAY[1:0] (Reg. A1h/D5-4) programming control.

I2C Host Interface Timing

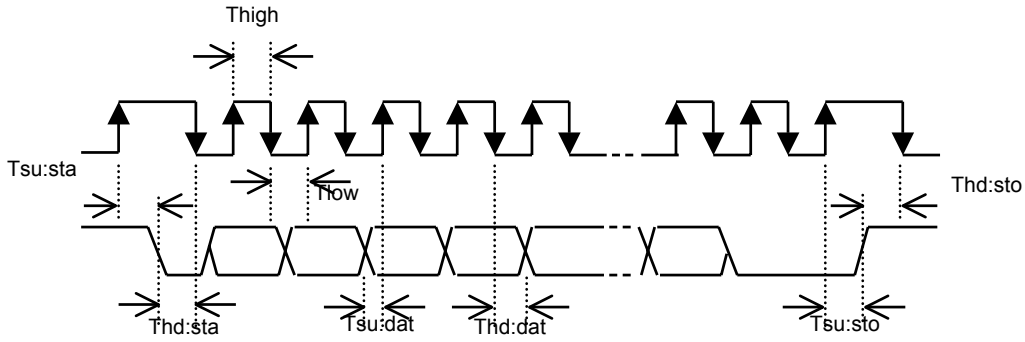
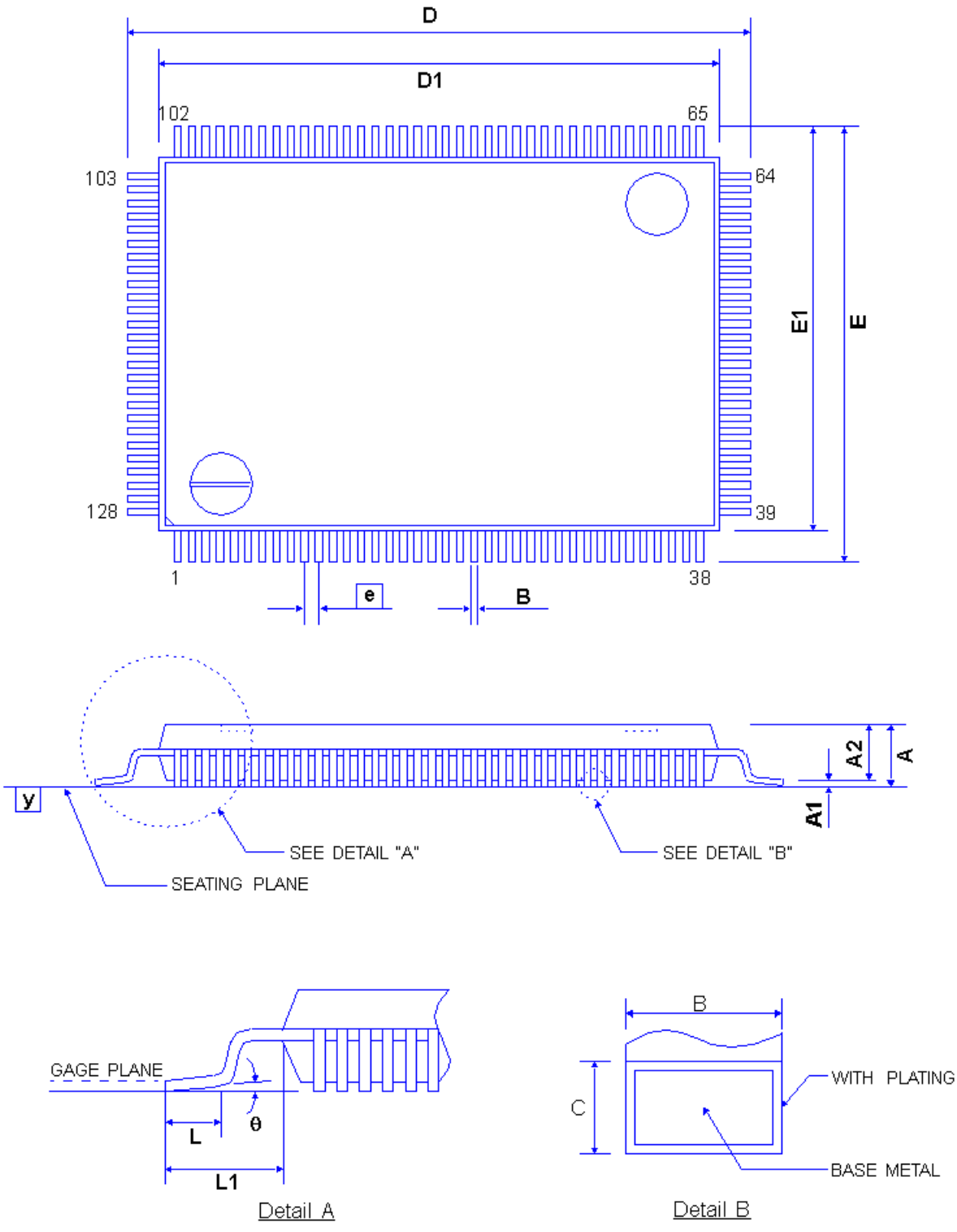


Figure-14 Host Interface Timing

Table-4 Host Interface Timing

Symbol	Parameter	Min	Max	Unit
Thigh	Clock High Period	500		ns
Tlow	Clock Low Period	500		ns
Tsu:dat	Data in Setup Time	200		ns
Thd:dat	Data in Hold Time	100		ns
Tsu:sta	Start condition Setup Time	500		ns
Thd:sta	Start condition Hold Time	500		ns
Tsu:sto	Stop condition Setup Time	500		ns
Thd:sto	Stop condition Hold Time	500		ns

PACKAGE OUTLINE



Symbol	Dimension in Millimeters	Dimension in Inches

	Min	Nom	Max	Min	Nom	Max
A	-	-	3.40	-	-	0.134
A1	0.25	-	-	0.010	-	-
A2	2.73	2.85	2.97	0.107	0.112	0.117
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09	-	0.20	0.004	-	0.008
D	23.70	23.90	24.10	0.933	0.941	0.949
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	17.70	17.90	18.10	0.697	0.705	0.713
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.95 BSC			0.077 BSC		
y	-	-	0.10	-	-	0.004
θ	0°	-	7°	0°	-	7°

ORDERING INFORMATION

Standard Configuration:

Prefix	Part Type	Package Type
MTL	007	F: PQFP