



# SYNCHRONOUS DRAM MODULE

## MT9LSDT872, MT9LSDT1672

For the latest data sheet, please refer to the Micron Web site: [www.micronsemi.com/datasheets/datasheet.html](http://www.micronsemi.com/datasheets/datasheet.html)

### FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC133- and PC100-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 133 MHz and 125 MHz SDRAM components
- ECC-optimized pinout
- 64MB (8 Meg x 72) and 128MB (16 Meg x 72)
- Single +3.3V  $\pm 0.3V$  power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

### OPTIONS

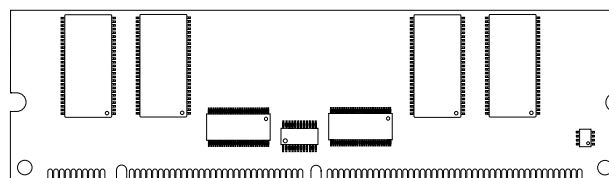
- Package  
168-pin DIMM (gold) G
- Frequency/CAS Latency\*  
133 MHz/CL = 2 -13E  
(7.5ns, 133 MHz SDRAMs)  
133 MHz/CL = 3 -133  
(7.5ns, 133 MHz SDRAMs)  
100 MHz/CL = 2 -10E  
(8ns, 125 MHz SDRAM)

\*Device latency only; extra clock cycle required due to input register.

### KEY SDRAM COMPONENT TIMING PARAMETERS

| MODULE MARKING | SPEED GRADE | CAS LATENCY | ACCESS TIME | SETUP TIME | HOLD TIME |
|----------------|-------------|-------------|-------------|------------|-----------|
| -13E           | -7E         | 2           | 5.4ns       | 1.5ns      | 0.8ns     |
| -133           | -75         | 3           | 5.4ns       | 1.5ns      | 0.8ns     |
| -10E           | -8E         | 2           | 6ns         | 2ns        | 1ns       |

### PIN ASSIGNMENT (FRONT VIEW) 168-PIN DIMM



| PIN | SYMBOL          | PIN | SYMBOL          | PIN | SYMBOL          | PIN | SYMBOL          |
|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|
| 1   | V <sub>SS</sub> | 43  | V <sub>SS</sub> | 85  | V <sub>SS</sub> | 127 | V <sub>SS</sub> |
| 2   | DQ0             | 44  | DNU             | 86  | DQ32            | 128 | CKE0            |
| 3   | DQ1             | 45  | S2#             | 87  | DQ33            | 129 | RFU (S3#)       |
| 4   | DQ2             | 46  | DQMB2           | 88  | DQ34            | 130 | DQMB6           |
| 5   | DQ3             | 47  | DQMB3           | 89  | DQ35            | 131 | DQMB7           |
| 6   | V <sub>DD</sub> | 48  | DNU             | 90  | V <sub>DD</sub> | 132 | RFU (A13)       |
| 7   | DQ4             | 49  | V <sub>DD</sub> | 91  | DQ36            | 133 | V <sub>DD</sub> |
| 8   | DQ5             | 50  | NC              | 92  | DQ37            | 134 | NC              |
| 9   | DQ6             | 51  | NC              | 93  | DQ38            | 135 | NC              |
| 10  | DQ7             | 52  | CB2             | 94  | DQ39            | 136 | CB6             |
| 11  | DQ8             | 53  | CB3             | 95  | DQ40            | 137 | CB7             |
| 12  | V <sub>SS</sub> | 54  | V <sub>SS</sub> | 96  | V <sub>SS</sub> | 138 | V <sub>SS</sub> |
| 13  | DQ9             | 55  | DQ16            | 97  | DQ41            | 139 | DQ48            |
| 14  | DQ10            | 56  | DQ17            | 98  | DQ42            | 140 | DQ49            |
| 15  | DQ11            | 57  | DQ18            | 99  | DQ43            | 141 | DQ50            |
| 16  | DQ12            | 58  | DQ19            | 100 | DQ44            | 142 | DQ51            |
| 17  | DQ13            | 59  | V <sub>DD</sub> | 101 | DQ45            | 143 | V <sub>DD</sub> |
| 18  | V <sub>DD</sub> | 60  | DQ20            | 102 | V <sub>DD</sub> | 144 | DQ52            |
| 19  | DQ14            | 61  | NC              | 103 | DQ46            | 145 | NC              |
| 20  | DQ15            | 62  | NC              | 104 | DQ47            | 146 | NC              |
| 21  | CB0             | 63  | RFU (CKE1)      | 105 | CB4             | 147 | REGE            |
| 22  | CB1             | 64  | V <sub>SS</sub> | 106 | CB5             | 148 | V <sub>SS</sub> |
| 23  | V <sub>SS</sub> | 65  | DQ21            | 107 | V <sub>SS</sub> | 149 | DQ53            |
| 24  | NC              | 66  | DQ22            | 108 | NC              | 150 | DQ54            |
| 25  | NC              | 67  | DQ23            | 109 | NC              | 151 | DQ55            |
| 26  | V <sub>DD</sub> | 68  | V <sub>SS</sub> | 110 | V <sub>DD</sub> | 152 | V <sub>SS</sub> |
| 27  | WE#             | 69  | DQ24            | 111 | CAS#            | 153 | DQ56            |
| 28  | DQMB0           | 70  | DQ25            | 112 | DQMB4           | 154 | DQ57            |
| 29  | DQMB1           | 71  | DQ26            | 113 | DQMB5           | 155 | DQ58            |
| 30  | S0#             | 72  | DQ27            | 114 | RFU (S1#)       | 156 | DQ59            |
| 31  | DNU             | 73  | V <sub>DD</sub> | 115 | RAS#            | 157 | V <sub>DD</sub> |
| 32  | V <sub>SS</sub> | 74  | DQ28            | 116 | V <sub>SS</sub> | 158 | DQ60            |
| 33  | A0              | 75  | DQ29            | 117 | A1              | 159 | DQ61            |
| 34  | A2              | 76  | DQ30            | 118 | A3              | 160 | DQ62            |
| 35  | A4              | 77  | DQ31            | 119 | A5              | 161 | DQ63            |
| 36  | A6              | 78  | V <sub>SS</sub> | 120 | A7              | 162 | V <sub>SS</sub> |
| 37  | A8              | 79  | CK2             | 121 | A9              | 163 | CK3             |
| 38  | A10             | 80  | NC              | 122 | BA0             | 164 | NC              |
| 39  | BA1             | 81  | WP              | 123 | A11             | 165 | SA0             |
| 40  | V <sub>DD</sub> | 82  | SDA             | 124 | V <sub>DD</sub> | 166 | SA1             |
| 41  | V <sub>DD</sub> | 83  | SCL             | 125 | CK1             | 167 | SA2             |
| 42  | CK0             | 84  | V <sub>DD</sub> | 126 | RFU (A12)       | 168 | V <sub>DD</sub> |

**NOTE:** Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.



## PART NUMBERS

| PART NUMBER        | CONFIGURATION | SYSTEM BUS SPEED |
|--------------------|---------------|------------------|
| MT9LSDT872G-13E__  | 8 Meg x 72    | 133MHz           |
| MT9LSDT872G-133__  | 8 Meg x 72    | 133MHz           |
| MT9LSDT872G-10E__  | 8 Meg x 72    | 100MHz           |
| MT9LSDT1672G-13E__ | 16 Meg x 72   | 133MHz           |
| MT9LSDT1672G-133__ | 16 Meg x 72   | 133 MHz          |
| MT9LSDT1672G-10E__ | 16 Meg x 72   | 100 MHz          |

**NOTE:** All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9LSDT1672G-133B1

## GENERAL DESCRIPTION

The MT9LSDT872 and MT9LSDT1672 are high-speed CMOS, dynamic random-access, 64MB and 128MB memories organized in a x72 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signals CK0).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every

clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb and 128Mb SDRAM data sheets.

## PLL AND REGISTER OPERATION

These modules can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the modules is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

## SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

## SPD CLOCK AND DATA CONVENTIONS

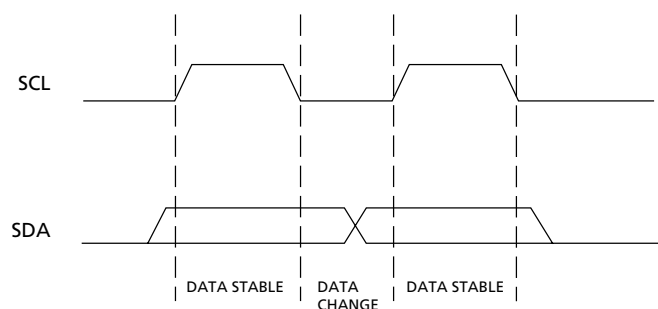
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

### SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

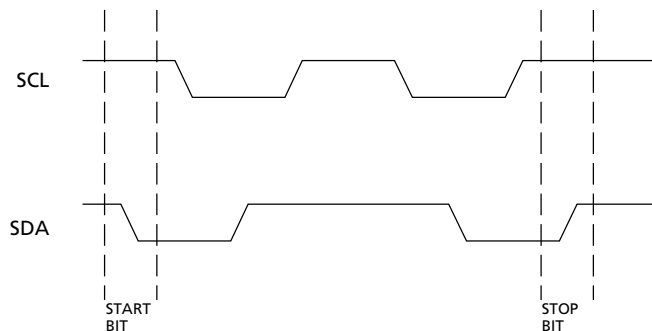


**Figure 1**  
**Data Validity**

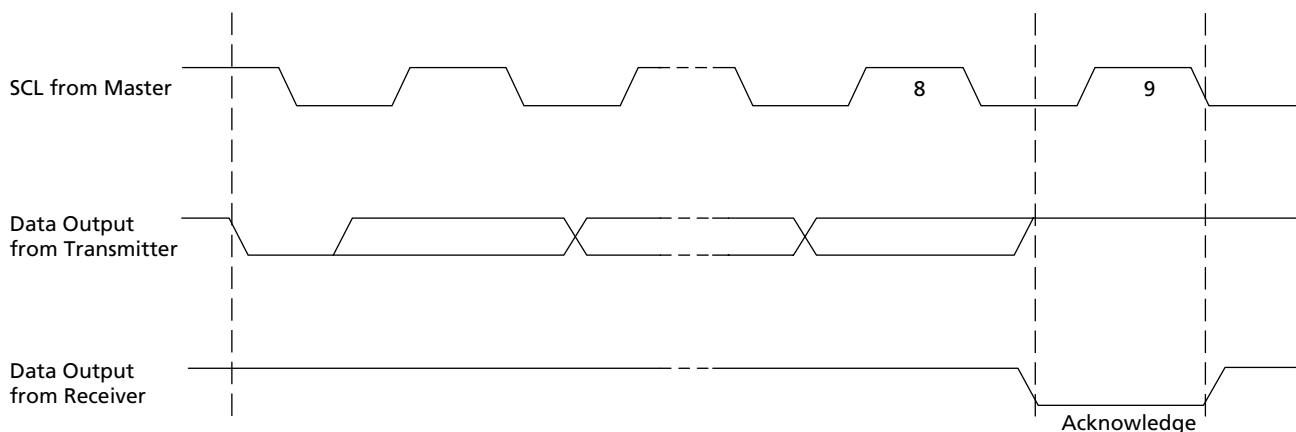
## SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

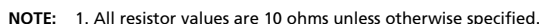
The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.



**Figure 2**  
**Definition of Start and Stop**



**Figure 3**  
**Acknowledge Response from Receiver**





## PIN DESCRIPTIONS

| PIN NUMBERS                                                                                                                     | SYMBOL          | TYPE         | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27, 111, 115                                                                                                                    | WE#, CAS#, RAS# | Input        | Command Inputs: WE#, RAS#, and CAS# (along with S0#, S2#) define the command being entered.                                                                                                                                                                                                                                                                                                                                                                                                            |
| 42, 79, 125, 163                                                                                                                | CK0-CK3         | Input        | Clock: CK0 is distributed through an on-board PLL to all devices. CK1-CK3 are terminated.                                                                                                                                                                                                                                                                                                                                                                                                              |
| 128                                                                                                                             | CKE0            | Input        | Clock Enable: CKE0 activates (HIGH) and deactivates (LOW) the CK0 signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 is synchronous except after the device enters power-down and self refresh modes, where CKE0 becomes asynchronous until after exiting the same mode. The input buffers, including CK0, are disabled during power-down and self refresh modes, providing low standby power. |
| 30, 45                                                                                                                          | S0#, S2#        | Input        | Chip Select: S0#, S2# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#, S2# are registered HIGH. S0#, S2# are considered part of the command code.                                                                                                                                                                                                                                                                                          |
| 28-29, 46-47, 112-113, 130-131                                                                                                  | DQMB0-DQMB7     | Input        | Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.                                                                                                                                                                                              |
| 122, 39                                                                                                                         | BA0, BA1        | Input        | Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.                                                                                                                                                                                                                                                                                                                                                                                          |
| 33, 117, 34, 118, 35, 119, 36, 120, 37, 121, 38, 123                                                                            | A0-A11          | Input        | Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A8/A9, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.                                                                     |
| 81                                                                                                                              | WP              | Input        | Write Protect: Serial presence-detect hardware write protect.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 83                                                                                                                              | SCL             | Input        | Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.                                                                                                                                                                                                                                                                                                                                                                                 |
| 165-167                                                                                                                         | SA0-SA2         | Input        | Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.                                                                                                                                                                                                                                                                                                                                                                                                           |
| 147                                                                                                                             | REGE            | Input        | Register Enable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161 | DQ0-DQ63        | Input/Output | Data I/Os: Data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 21-22, 0 52-53, 105-106, 136-137                                                                                                | CB0-CB7         | Input/Output | Check Bits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |


**PIN DESCRIPTIONS (continued)**

| PIN NUMBERS                                                                        | SYMBOL          | TYPE             | DESCRIPTION                                                                                                                                                 |
|------------------------------------------------------------------------------------|-----------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 82                                                                                 | SDA             | Input/<br>Output | Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module. |
| 6, 18, 26, 40-41, 49, 59,<br>73, 84, 90, 102, 110, 124,<br>133, 143, 157, 168      | V <sub>DD</sub> | Supply           | Power Supply: +3.3V ±0.3V.                                                                                                                                  |
| 1, 12, 23, 32, 43, 54, 64,<br>68, 78, 85, 96, 107, 116,<br>127, 138, 148, 152, 162 | V <sub>SS</sub> | Supply           | Ground.                                                                                                                                                     |
| 63, 114, 126, 129, 132                                                             | RFU             | –                | Reserved for Future Use: These pins are not connected on this module but are assigned pins on other SDRAM versions.                                         |
| 31, 44, 48                                                                         | DNU             | –                | Do Not Use: These pins are not connected on this module but are assigned pins on the compatible DRAM version.                                               |


**SERIAL PRESENCE-DETECT MATRIX**

| BYTE | DESCRIPTION                                                              | ENTRY (VERSION)   | MT9LSDT872 | MT9LSDT1672 |
|------|--------------------------------------------------------------------------|-------------------|------------|-------------|
| 0    | NUMBER OF BYTES USED BY MICRON                                           | 128               | 80         | 80          |
| 1    | TOTAL NUMBER OF SPD MEMORY BYTES                                         | 256               | 08         | 08          |
| 2    | MEMORY TYPE                                                              | SDRAM             | 04         | 04          |
| 3    | NUMBER OF ROW ADDRESSES                                                  | 12                | 0C         | 0C          |
| 4    | NUMBER OF COLUMN ADDRESSES                                               | 9 or 10           | 09         | 0A          |
| 5    | NUMBER OF BANKS                                                          | 1                 | 01         | 01          |
| 6    | MODULE DATA WIDTH                                                        | 72                | 48         | 48          |
| 7    | MODULE DATA WIDTH (continued)                                            | 0                 | 00         | 00          |
| 8    | MODULE VOLTAGE INTERFACE LEVELS                                          | LVTTL             | 01         | 01          |
| 9    | SDRAM CYCLE TIME, $t_{CK}$<br>(CAS LATENCY = 3)                          | 7 (-13E)          | 70         | 70          |
|      |                                                                          | 7.5 (-133)        | 75         | 75          |
|      |                                                                          | 8 (-10E)          | 80         | 80          |
| 10   | SDRAM ACCESS FROM CLOCK, $t_{AC}$<br>(CAS LATENCY = 3)                   | 5.4 (-13E/-133)   | 54         | 54          |
|      |                                                                          | 6 (-10E)          | 60         | 60          |
| 11   | MODULE CONFIGURATION TYPE                                                | ECC               | 02         | 02          |
| 12   | REFRESH RATE/TYPE                                                        | 15.6 $\mu$ s/SELF | 80         | 80          |
| 13   | SDRAM WIDTH (PRIMARY SDRAM)                                              | 8                 | 08         | 08          |
| 14   | ERROR-CHECKING SDRAM DATA WIDTH                                          | 8                 | 08         | 08          |
| 15   | MIN. CLOCK DELAY FROM BACK-TO-BACK<br>RANDOM COLUMN ADDRESSES, $t_{CCD}$ | 1                 | 01         | 01          |
| 16   | BURST LENGTHS SUPPORTED                                                  | 1, 2, 4, 8, PAGE  | 8F         | 8F          |
| 17   | NUMBER OF BANKS ON SDRAM DEVICE                                          | 4                 | 04         | 04          |
| 18   | CAS LATENCIES SUPPORTED                                                  | 2, 3              | 06         | 06          |
| 19   | CS LATENCY                                                               | 0                 | 01         | 01          |
| 20   | WE LATENCY                                                               | 0                 | 01         | 01          |
| 21   | SDRAM MODULE ATTRIBUTES                                                  | -13E/-133         | 1F         | 1F          |
|      |                                                                          | -10E              | 16         | 16          |
| 22   | SDRAM DEVICE ATTRIBUTES: GENERAL                                         | 0E                | 0E         | 0E          |
| 23   | SDRAM CYCLE TIME, $t_{CK}$<br>(CAS LATENCY = 2)                          | 7.5 (-13E)        | 75         | 75          |
|      |                                                                          | 10 (-133/-10E)    | A0         | A0          |
| 24   | SDRAM ACCESS FROM CLK, $t_{AC}$<br>(CAS LATENCY = 2)                     | 5.4(-13E)         | 54         | 54          |
|      |                                                                          | 6 (-10E)          | 60         | 60          |
| 25   | SDRAM CYCLE TIME, $t_{CK}$<br>(CAS LATENCY = 1)                          | –                 | 00         | 00          |
| 26   | SDRAM ACCESS FROM CLK, $t_{AC}$<br>(CAS LATENCY = 1)                     | –                 | 00         | 00          |
| 27   | MINIMUM ROW PRECHARGE TIME, $t_{RP}$                                     | 15 (-13E)         | 0F         | 0F          |
|      |                                                                          | 20 (-133/-10E)    | 14         | 14          |
|      |                                                                          | 14 (-13E)         | 0E         | 0E          |
| 28   | MINIMUM ROW ACTIVE TO ROW ACTIVE,<br>$t_{RRD}$                           | 14 (-13E)         | 0E         | 0E          |
|      |                                                                          | 15(-133)          | 0F         | 0F          |
|      |                                                                          | 20(-10E)          | 14         | 14          |
| 29   | MINIMUM RAS# TO CAS# DELAY, $t_{RCD}$                                    | 15(-13E)          | 0F         | 0F          |
|      |                                                                          | 20(-133/-10E)     | 14         | 14          |
|      |                                                                          | 37(-13E)          | 25         | 25          |

**NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."


**SERIAL PRESENCE-DETECT MATRIX (continued)**

| BYTE   | DESCRIPTION                                                           | ENTRY (VERSION)                           | MT9LSDT872                                         | MT9LSDT1672                                        |
|--------|-----------------------------------------------------------------------|-------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| 30     | MINIMUM RAS# PULSE WIDTH,<br>( $t_{RAS}^{MODULE} = t_{RC} - t_{RP}$ ) | 45(-13E)<br>44(-133)<br>50(-10E)          | 2D<br>2C<br>32                                     | 2D<br>2C<br>32                                     |
| 31     | MODULE BANK DENSITY                                                   | 64MB/128MB                                | 10                                                 | 20                                                 |
| 32     | COMMAND AND ADDRESS SETUP TIME,<br>$t_{AS}$ , $t_{CMS}$               | 1.5(-13E/-133)<br>2(-10E)                 | 15<br>20                                           | 15<br>20                                           |
| 33     | COMMAND AND ADDRESS HOLD TIME,<br>$t_{AH}$ , $t_{CMH}$                | 0.8(-13E/133)<br>1(-10E)                  | 08<br>10                                           | 08<br>10                                           |
| 34     | DATA SIGNAL INPUT SETUP TIME, $t_{DS}$                                | 1.5(-13E/-133)<br>2(-10E)                 | 15<br>20                                           | 15<br>20                                           |
| 35     | DATA SIGNAL INPUT HOLD TIME, $t_{DH}$                                 | 0.8(-13E/-133)<br>1(-10E)                 | 08<br>10                                           | 08<br>10                                           |
| 36-61  | RESERVED                                                              |                                           | 00                                                 | 00                                                 |
| 62     | SPD REVISION                                                          | REV. 1.2                                  | 12                                                 | 12                                                 |
| 63     | CHECKSUM FOR BYTES 0-62                                               | -13E<br>-133<br>-10E                      | 88<br>C5<br>0D                                     | 99<br>CE<br>16                                     |
| 64     | MANUFACTURER'S JEDEC ID CODE                                          | MICRON                                    | 2C                                                 | 2C                                                 |
| 65-71  | MANUFACTURER'S JEDEC ID CODE (CONT.)                                  |                                           | FF                                                 | FF                                                 |
| 72     | MANUFACTURING LOCATION                                                |                                           | 01<br>02<br>03<br>04<br>05<br>06<br>07<br>08<br>09 | 01<br>02<br>03<br>04<br>05<br>06<br>07<br>08<br>09 |
| 73-90  | MODULE PART NUMBER (ASCII)                                            |                                           | xx                                                 | xx                                                 |
| 91     | PCB IDENTIFICATION CODE                                               | 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9 | 01<br>02<br>03<br>04<br>05<br>06<br>07<br>08<br>09 | 01<br>02<br>03<br>04<br>05<br>06<br>07<br>08<br>09 |
| 92     | IDENTIFICATION CODE (CONT.)                                           | 0                                         | 00                                                 | 00                                                 |
| 93     | YEAR OF MANUFACTURE IN BCD                                            |                                           | xx                                                 | xx                                                 |
| 94     | WEEK OF MANUFACTURE IN BCD                                            |                                           | xx                                                 | xx                                                 |
| 95-98  | MODULE SERIAL NUMBER                                                  |                                           | xx                                                 | xx                                                 |
| 99-125 | MANUFACTURER-SPECIFIC DATA (RSVD)                                     |                                           | —                                                  | —                                                  |
| 126    | SYSTEM FREQUENCY                                                      | 100/133 MHz                               | 64                                                 | 64                                                 |
| 127    | SDRAM COMPONENT AND CLOCK DETAIL                                      |                                           | 8F                                                 | 8F                                                 |

**NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."  
2. x = Variable Data.



## Commands

Truth Table 1 provides a quick reference of available commands. This is followed by a written description of each command. For a more detailed description of

commands and operations refer to the 64Mb, 128Mb x4, x8, x16 SDRAM datasheets.

## TRUTH TABLE 1 – COMMANDS AND DQMB OPERATION

(Note: 1)

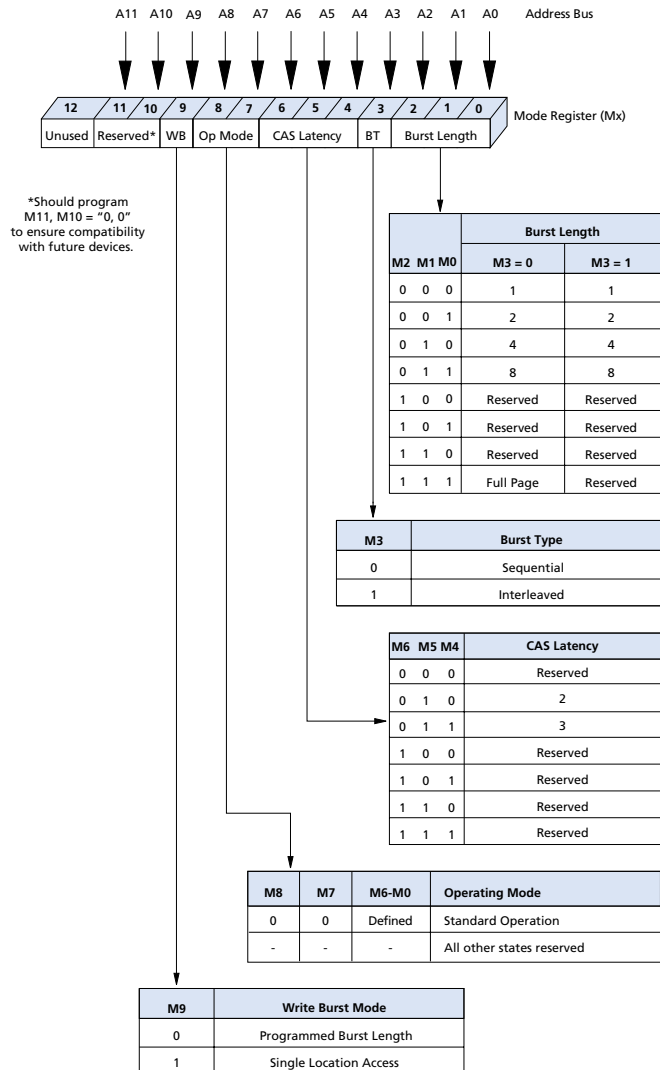
| NAME (FUNCTION)                                           | CS# | RAS# | CAS# | WE# | DQMB             | ADDR     | DQs    | NOTES |
|-----------------------------------------------------------|-----|------|------|-----|------------------|----------|--------|-------|
| COMMAND INHIBIT (NOP)                                     | H   | X    | X    | X   | X                | X        | X      |       |
| NO OPERATION (NOP)                                        | L   | H    | H    | H   | X                | X        | X      |       |
| ACTIVE (Select bank and activate row)                     | L   | L    | H    | H   | X                | Bank/Row | X      | 3     |
| READ (Select bank and column, and start READ burst)       | L   | H    | L    | H   | L/H <sup>8</sup> | Bank/Col | X      | 4     |
| WRITE (Select bank and column, and start WRITE burst)     | L   | H    | L    | L   | L/H <sup>8</sup> | Bank/Col | Valid  | 4     |
| BURST TERMINATE                                           | L   | H    | H    | L   | X                | X        | Active |       |
| PRECHARGE (Deactivate row in bank or banks)               | L   | L    | H    | L   | X                | Code     | X      | 5     |
| AUTO REFRESH or<br>SELF REFRESH (Enter self refresh mode) | L   | L    | L    | H   | X                | X        | X      | 6, 7  |
| LOAD MODE REGISTER                                        | L   | L    | L    | L   | X                | Op-Code  | X      | 2     |
| Write Enable/Output Enable                                | –   | –    | –    | –   | L                | –        | Active | 8     |
| Write Inhibit/Output High-Z                               | –   | –    | –    | –   | H                | –        | High-Z | 8     |

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
  2. A0-A11 define the op-code written to the Mode Register.
  3. A0-A11 provide row address, and BA0, BA1 determine which bank is made active.
  4. A0-A8/A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
  5. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0, BA1 are "Don't Care."
  6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
  8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).


**Table 1  
Burst Definition**

| Burst Length  | Starting Column Address   | Order of Accesses Within a Burst                     |                  |
|---------------|---------------------------|------------------------------------------------------|------------------|
|               |                           | Type=Sequential                                      | Type=Interleaved |
| 2             | A0                        |                                                      |                  |
|               | 0                         | 0-1                                                  | 0-1              |
|               | 1                         | 1-0                                                  | 1-0              |
| 4             | A1 A0                     |                                                      |                  |
|               | 0 0                       | 0-1-2-3                                              | 0-1-2-3          |
|               | 0 1                       | 1-2-3-0                                              | 1-0-3-2          |
|               | 1 0                       | 2-3-0-1                                              | 2-3-0-1          |
|               | 1 1                       | 3-0-1-2                                              | 3-2-1-0          |
| 8             | A2 A1 A0                  |                                                      |                  |
|               | 0 0 0                     | 0-1-2-3-4-5-6-7                                      | 0-1-2-3-4-5-6-7  |
|               | 0 0 1                     | 1-2-3-4-5-6-7-0                                      | 1-0-3-2-5-4-7-6  |
|               | 0 1 0                     | 2-3-4-5-6-7-0-1                                      | 2-3-0-1-6-7-4-5  |
|               | 0 1 1                     | 3-4-5-6-7-0-1-2                                      | 3-2-1-0-7-6-5-4  |
|               | 1 0 0                     | 4-5-6-7-0-1-2-3                                      | 4-5-6-7-0-1-2-3  |
|               | 1 0 1                     | 5-6-7-0-1-2-3-4                                      | 5-4-7-6-1-0-3-2  |
|               | 1 1 0                     | 6-7-0-1-2-3-4-5                                      | 6-7-4-5-2-3-0-1  |
|               | 1 1 1                     | 7-0-1-2-3-4-5-6                                      | 7-6-5-4-3-2-1-0  |
| Full Page (y) | n = A0-9/8 (location 0-y) | Cn, Cn+1, Cn+2<br>Cn+3, Cn+4...<br>...Cn-1,<br>Cn... | Not supported    |

- NOTE:**
- For full-page accesses: y = 1,024 (128MB), y = 512 (64MB)
  - For a burst length of two, A1-A9/A8 select the block of two burst; A0 selects the starting column within the block.
  - For a burst length of four, A2-A9/A8 select the block of four burst; A0-A1 select the starting column within the block.
  - For a burst length of eight, A3-A9/A8 select the block of eight burst; A0-A2 select the starting column within the block.
  - For a full-page burst, the full row is selected and A0-A9/A8 select the starting column.
  - Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  - For a burst length of one, A0-A9/A8 select the unique column to be accessed, and Mode Register bit M3 is ignored.


**Figure 4  
Mode Register Definition**



### ABSOLUTE MAXIMUM RATINGS\*

Voltage on V<sub>DD</sub> Supply Relative to V<sub>SS</sub> : -1V to +4.6V  
Voltage on Inputs, NC or I/O Pins

Relative to V<sub>SS</sub> ..... -1V to +4.6V  
Operating Temperature, T<sub>A</sub> (ambient) ... 0°C to +70°C  
Storage Temperature (plastic) ..... -55°C to +125°C  
Power Dissipation ..... 18W

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 2) (V<sub>DD</sub> = +3.3V ±0.3V)

| PARAMETER/CONDITION                                                                                                | SYMBOL          | MIN  | MAX                   | UNITS | NOTES |
|--------------------------------------------------------------------------------------------------------------------|-----------------|------|-----------------------|-------|-------|
| SUPPLY VOLTAGE                                                                                                     | V <sub>DD</sub> | 3    | 3.6                   | V     |       |
| INPUT HIGH VOLTAGE: Logic 1; All inputs                                                                            | V <sub>IH</sub> | 2    | V <sub>DD</sub> + 0.3 | V     | 3     |
| INPUT LOW VOLTAGE: Logic 0; All inputs                                                                             | V <sub>IL</sub> | -0.5 | 0.8                   | V     | 3     |
| INPUT LEAKAGE CURRENT:<br>Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub><br>(All other pins not under test = 0V) | I <sub>I1</sub> | -5   | 5                     | μA    | 4     |
| OUTPUT LEAKAGE CURRENT:<br>DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>                               | I <sub>OZ</sub> | -5   | 5                     | μA    |       |
| OUTPUT LEVELS:<br>Output High Voltage (I <sub>OUT</sub> = -4mA)<br>Output Low Voltage (I <sub>OUT</sub> = 4mA)     | V <sub>OH</sub> | 2.4  | –                     | V     |       |
|                                                                                                                    | V <sub>OL</sub> | –    | 0.4                   | V     |       |

- NOTE:**
1. All voltages referenced to V<sub>SS</sub>.
  2. An initial pause of 100μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
  3. V<sub>IH</sub> overshoot: V<sub>IH</sub> (MAX) = V<sub>DD</sub> + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V<sub>IL</sub> undershoot: V<sub>IL</sub> (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.
  4. Input leakage values based on register electrical characteristics, V<sub>DD</sub> = 3.6V.


**I<sub>DD</sub> SPECIFICATIONS AND CONDITIONS**

 (Notes: 1-4) ( $V_{DD} = +3.3V \pm 0.3V$ )

(Notes: 1-4) (V<sub>DD</sub> = +3.3V ±0.3V)

|                                                                                                                                      |                                                    |       | MAX   |       |       |       |               |                  |
|--------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|-------|-------|-------|-------|-------|---------------|------------------|
| PARAMETER/CONDITION                                                                                                                  | SYMBOL                                             | SIZE  | -13E  | -133  | -10E  | UNITS | NOTES         |                  |
| OPERATING CURRENT: Active Mode;<br>Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CAS latency = 3                | IDD1                                               | 64MB  | 1,125 | 1,035 | 855   | mA    | 5, 6,<br>7, 8 |                  |
|                                                                                                                                      |                                                    | 128MB | 1,440 | 1,350 | 1,260 |       |               |                  |
| STANDBY CURRENT: Power-Down Mode;<br>CKE = LOW; All banks idle                                                                       | IDD2                                               | 64MB  | 18    | 18    | 18    | mA    | 8             |                  |
|                                                                                                                                      |                                                    | 128MB | 18    | 18    | 18    |       |               |                  |
| STANDBY CURRENT: Active Mode; S0#, S2# = HIGH;<br>CKE = HIGH;All banks active after t <sub>RCD</sub> met;<br>No accesses in progress | IDD3                                               | 64MB  | 405   | 405   | 315   | mA    | 5, 7,<br>8, 9 |                  |
|                                                                                                                                      |                                                    | 128MB | 450   | 450   | 360   |       |               |                  |
| OPERATING CURRENT: Burst Mode; Continuous burst;<br>READ or WRITE; All banks active; CAS latency = 3                                 | IDD4                                               | 64MB  | 1,350 | 1,260 | 1,080 | mA    | 5, 6,<br>7, 8 |                  |
|                                                                                                                                      |                                                    | 128MB | 1,485 | 1,350 | 1,260 |       |               |                  |
| AUTO REFRESH CURRENT: CKE = HIGH;<br>S0#, S2# = HIGH                                                                                 | t <sub>RC</sub> = t <sub>RC</sub> (MIN);<br>CL = 3 | IDD5  | 64MB  | 2,070 | 1,890 | 1,710 | mA            | 5, 6, 7,<br>8, 9 |
|                                                                                                                                      |                                                    | 128MB | 2,970 | 2,790 | 2,430 |       |               |                  |
|                                                                                                                                      | t <sub>RC</sub> = 15.625µs;<br>CL = 3              | IDD6  | 64MB  | 27    | 27    | 27    | mA            |                  |
|                                                                                                                                      |                                                    |       | 128MB | 27    | 27    | 27    |               |                  |
| SELF REFRESH CURRENT: CKE ≤ 0.2V                                                                                                     | IDD7                                               | 64MB  | 9     | 9     | 9     | mA    | 10            |                  |
|                                                                                                                                      |                                                    | 128MB | 18    | 18    | 18    |       |               |                  |

- NOTE:**
1. All voltages referenced to  $V_{SS}$ .
  2. An initial pause of 100 $\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
  3. AC timing and I<sub>DD</sub> test have  $V_{IL} = 0V$  and  $V_{IH} = 3V$ , with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at  $V_{IL}(\text{MAX})$  and  $V_{IL}(\text{MIN})$  and no longer at the 1.5V crossover point.
  4. I<sub>DD</sub> specifications are tested after the device is properly initialized.
  5. I<sub>DD</sub> is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
  6. The I<sub>DD</sub> current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
  7. Address transitions average one transition every two clocks.
  8.  $t_{CK} = 7\text{ns}$  for -13E;  $t_{CK} = 7.5\text{ns}$  for -133;  $t_{CK} = 10\text{ns}$  for -10E.
  9. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid  $V_{IH}$  or  $V_{IL}$  levels.
  10. Enables on-chip refresh and address counters.



## CAPACITANCE

| PARAMETER                                            | SYMBOL          | MAX | UNITS |
|------------------------------------------------------|-----------------|-----|-------|
| Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE# | C <sub>I1</sub> | 8   | pF    |
| Input Capacitance: S0#, S2#, CKE0, DQMB0#-DQMB7#     | C <sub>I2</sub> | 8   | pF    |
| Input Capacitance: CK0                               | C <sub>I3</sub> | 6   | pF    |
| Input Capacitance: REGE                              | C <sub>I4</sub> | 5   | pF    |
| Input Capacitance: SCL, SA0-SA2, WP                  | C <sub>I5</sub> | 12  | pF    |
| Input/Output Capacitance: DQ0-DQ63, CB0-CB7, SDA     | C <sub>IO</sub> | 8   | pF    |

**NOTE:** This parameter is sampled. V<sub>DD</sub> = +3.3V; f = 1 MHz.

## SDRAM COMPONENT\* AC ELECTRICAL CHARACTERISTICS

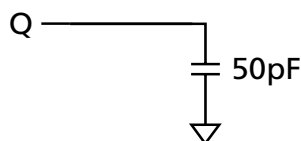
(Notes: 2, 3, 4, 5, 6, 7)

| AC CHARACTERISTICS                     |        |                             | -13E        |         | -133          |         | -10E        |         |       |       |
|----------------------------------------|--------|-----------------------------|-------------|---------|---------------|---------|-------------|---------|-------|-------|
| PARAMETER                              |        | SYMBOL                      | MIN         | MAX     | MIN           | MAX     | MIN         | MAX     | UNITS | NOTES |
| Access time from CLK (positive edge)   | CL = 3 | t <sub>AC</sub>             |             | 5.4     |               | 5.4     |             | 6       | ns    | 8     |
|                                        | CL = 2 | t <sub>AC</sub>             |             | 5.4     |               | 6       |             | 6       | ns    |       |
| Address hold time                      |        | t <sub>AH</sub>             | 0.8         |         | 0.8           |         | 1           |         | ns    |       |
| Address setup time                     |        | t <sub>AS</sub>             | 1.5         |         | 1.5           |         | 2           |         | ns    |       |
| CLK high level width                   |        | t <sub>CH</sub>             | 2.5         |         | 2.5           |         | 3           |         | ns    |       |
| CLK low level width                    |        | t <sub>CL</sub>             | 2.5         |         | 2.5           |         | 3           |         | ns    |       |
| Clock cycle time                       | CL = 3 | t <sub>CK</sub>             | 7           |         | 7.5           |         | 8           |         | ns    | 9     |
|                                        | CL = 2 | t <sub>CK</sub>             | 7.5         |         | 10            |         | 10          |         | ns    | 9     |
| CKE hold time                          |        | t <sub>CKH</sub>            | 0.8         |         | 0.8           |         | 1           |         | ns    |       |
| CKE setup time                         |        | t <sub>CKS</sub>            | 1.5         |         | 1.5           |         | 2           |         | ns    |       |
| CS#, RAS#, CAS#, WE#, DQM hold time    |        | t <sub>CMH</sub>            | 0.8         |         | 0.8           |         | 1           |         | ns    |       |
| CS#, RAS#, CAS#, WE#, DQM setup time   |        | t <sub>CMS</sub>            | 1.5         |         | 1.5           |         | 2           |         | ns    |       |
| Data-in hold time                      |        | t <sub>DH</sub>             | 0.8         |         | 0.8           |         | 1           |         | ns    |       |
| Data-in setup time                     |        | t <sub>DS</sub>             | 1.5         |         | 1.5           |         | 2           |         | ns    |       |
| Data-out high-impedance time           | CL = 3 | t <sub>HZ</sub>             |             | 5.4     |               | 5.4     |             | 6       | ns    | 10    |
|                                        | CL = 2 | t <sub>HZ</sub>             |             | 5.4     |               | 6       |             | 7       | ns    | 10    |
| Data-out low-impedance time            |        | t <sub>LZ</sub>             | 1           |         | 1             |         | 1           |         | ns    |       |
| Data-out hold time (load)              |        | t <sub>OH</sub>             | 2.7         |         | 2.7           |         | 3           |         | ns    |       |
| Data-out hold time (no load)           |        | t <sub>OH<sub>N</sub></sub> | 1.8         |         | 1.8           |         | 1.8         |         | ns    | 11    |
| ACTIVE to PRECHARGE command            |        | t <sub>RAS</sub>            | 37          | 120,000 | 44            | 120,000 | 50          | 120,000 | ns    |       |
| ACTIVE to ACTIVE command period        |        | t <sub>RC</sub>             | 60          |         | 66            |         | 70          |         | ns    |       |
| ACTIVE to READ or WRITE delay          |        | t <sub>RCD</sub>            | 15          |         | 20            |         | 20          |         | ns    |       |
| Refresh period (4,096 cycles)          |        | t <sub>REF</sub>            |             | 64      |               | 64      |             | 64      | ms    |       |
| AUTO REFRESH PERIOD                    |        | t <sub>RFC</sub>            | 66          |         | 66            |         | 70          |         | ns    |       |
| PRECHARGE command period               |        | t <sub>RP</sub>             | 15          |         | 20            |         | 20          |         | ns    |       |
| ACTIVE bank A to ACTIVE bank B command |        | t <sub>RRD</sub>            | 14          |         | 15            |         | 20          |         | ns    |       |
| Transition time                        |        | t <sub>T</sub>              | 0.3         | 1.2     | 0.3           | 1.2     | 0.3         | 1.2     | ns    | 12    |
| WRITE recovery time                    |        | t <sub>WR</sub>             | 1 CLK + 7ns |         | 1 CLK + 7.5ns |         | 1 CLK + 7ns |         | –     | 13    |
|                                        |        |                             | 14          |         | 15            |         | 15          |         | ns    | 14    |
| Exit SELF REFRESH to ACTIVE command    |        | t <sub>XSR</sub>            | 67          |         | 75            |         | 80          |         | ns    |       |

\*Specifications for the SDRAM components used on the module.



- NOTE:**
1. This parameter is sampled.  $V_{DD} = +3.3V$ ;  $f = 1 \text{ MHz}$ .
  5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ) is ensured.
  6. An initial pause of  $100\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{\text{REF}}$  refresh requirement is exceeded.
  7. AC characteristics assume  $t_T = 1\text{ns}$ .
  8. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
  9. Outputs measured at  $1.5V$  with equivalent load:



10.  $t_{\text{HZ}}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ . The last valid data element will meet  $t_{\text{OH}}$  before going High-Z.
11. AC timing and  $I_{DD}$  test have  $V_{IL} = 0V$  and  $V_{IH} = 3V$ , with timing referenced to  $1.5V$  crossover point. If the input transition time is longer than  $1\text{ns}$ , then the timing is referenced at  $V_{IL}(\text{MAX})$  and  $V_{IL}(\text{MIN})$  and no longer at the  $1.5V$  crossover point.
24. There will be an added one-clock latency at the system level due to the register requiring an added clock cycle.
26. Auto precharge mode only. The precharge timing budget ( $t_{\text{RP}}$ ) begins  $7.5\text{ns}/7\text{ns}$  after the first clock delay, after the last WRITE is executed.
27. Precharge mode only.
28. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including  $t_{\text{WR}}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
30.  $t_{\text{AC}}$  for -133 at  $CL = 3$  with no load is  $4.6\text{ns}$  and is guaranteed by design.
32. Parameter guaranteed by design.

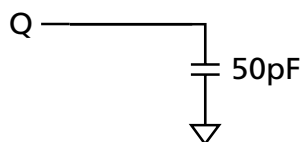


## AC FUNCTIONAL CHARACTERISTICS

(Notes: 1-7)

| PARAMETER                                               | SYMBOL           | -133 | -13E/-10E | UNITS    | NOTES  |
|---------------------------------------------------------|------------------|------|-----------|----------|--------|
| READ/WRITE command to READ/WRITE command                | $t_{CCD}$        | 1    | 1         | $t_{CK}$ | 8      |
| CKE to clock disable or power-down entry mode           | $t_{CKED}$       | 1    | 1         | $t_{CK}$ | 9      |
| CKE to clock enable or power-down exit setup mode       | $t_{PED}$        | 1    | 1         | $t_{CK}$ | 9      |
| DQM to input data delay                                 | $t_{DQD}$        | 0    | 0         | $t_{CK}$ | 8      |
| DQM to data mask during WRITES                          | $t_{DQM}$        | 0    | 0         | $t_{CK}$ | 8      |
| DQM to data high-impedance during READs                 | $t_{DQZ}$        | 2    | 2         | $t_{CK}$ | 8      |
| WRITE command to input data delay                       | $t_{DWD}$        | 0    | 0         | $t_{CK}$ | 8      |
| Data-in to ACTIVE command                               | $t_{DAL}$        | 5    | 4         | $t_{CK}$ | 10, 11 |
| Data-in to PRECHARGE command                            | $t_{DPL}$        | 2    | 2         | $t_{CK}$ | 11, 12 |
| Last data-in to burst STOP command                      | $t_{BDL}$        | 1    | 1         | $t_{CK}$ | 8      |
| Last data-in to new READ/WRITE command                  | $t_{CDL}$        | 1    | 1         | $t_{CK}$ | 8      |
| Last data-in to PRECHARGE command                       | $t_{RDL}$        | 2    | 2         | $t_{CK}$ | 11, 12 |
| LOAD MODE REGISTER command to ACTIVE or REFRESH command | $t_{MRD}$        | 2    | 2         | $t_{CK}$ | 13     |
| Data-out to high-impedance from PRECHARGE command       | CL = 3 $t_{ROH}$ | 3    | 3         | $t_{CK}$ | 8      |
|                                                         | CL = 2 $t_{ROH}$ | 2    | 2         | $t_{CK}$ | 8      |

- NOTE:**
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ) is ensured.
  2. An initial pause of 100 $\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
  3. AC characteristics assume  $t_T = 1\text{ns}$ .
  4. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
  5. Outputs measured at 1.5V with equivalent load:



6. AC timing and  $I_{DD}$  test have  $V_{IL} = 0\text{V}$  and  $V_{IH} = 3\text{V}$ , with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at  $V_{IL}(\text{MAX})$  and  $V_{IL}(\text{MIN})$  and no longer at the 1.5V crossover point.
7. There will be an added one-clock latency at the system level due to the register requiring an added clock cycle.
8. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
9. Timing actually specified by  $t_{CKS}$ ; clock(s) specified as a reference only at minimum cycle rate.
10. Timing actually specified by  $t_{WR}$  plus  $t_{RP}$ ; clock(s) specified as a reference only at minimum cycle rate.
11. Based on  $t_{CK} = 143\text{MHz}$  for -13E,  $t_{CK} = 133\text{MHz}$  for -133, 100MHz for -10E.
12. Timing actually specified by  $t_{WR}$ .
13. JEDEC and PC100 specify three clocks.


**SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS**

 (Note: 1) ( $V_{DD} = +3.3V \pm 0.3V$ )

| PARAMETER/CONDITION                                                                       | SYMBOL   | MIN                 | MAX                 | UNITS   |
|-------------------------------------------------------------------------------------------|----------|---------------------|---------------------|---------|
| SUPPLY VOLTAGE                                                                            | $V_{DD}$ | 3                   | 3.6                 | V       |
| INPUT HIGH VOLTAGE: Logic 1; All inputs                                                   | $V_{IH}$ | $V_{DD} \times 0.7$ | $V_{DD} + 0.5$      | V       |
| INPUT LOW VOLTAGE: Logic 0; All inputs                                                    | $V_{IL}$ | -1                  | $V_{DD} \times 0.3$ | V       |
| OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$                                                       | $V_{OL}$ | –                   | 0.4                 | V       |
| INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to $V_{DD}$                                         | $I_{LI}$ | –                   | 10                  | $\mu A$ |
| OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to $V_{DD}$                                       | $I_{LO}$ | –                   | 10                  | $\mu A$ |
| STANDBY CURRENT:<br>SCL = SDA = $V_{DD} - 0.3V$ ; All other inputs = GND or $3.3V + 10\%$ | $I_{SB}$ | –                   | 30                  | $\mu A$ |
| POWER SUPPLY CURRENT:<br>SCL clock frequency = 100 KHz                                    | $I_{DD}$ | –                   | 2                   | mA      |

**SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS**

 (Note: 1) ( $V_{DD} = +3.3V \pm 0.3V$ )

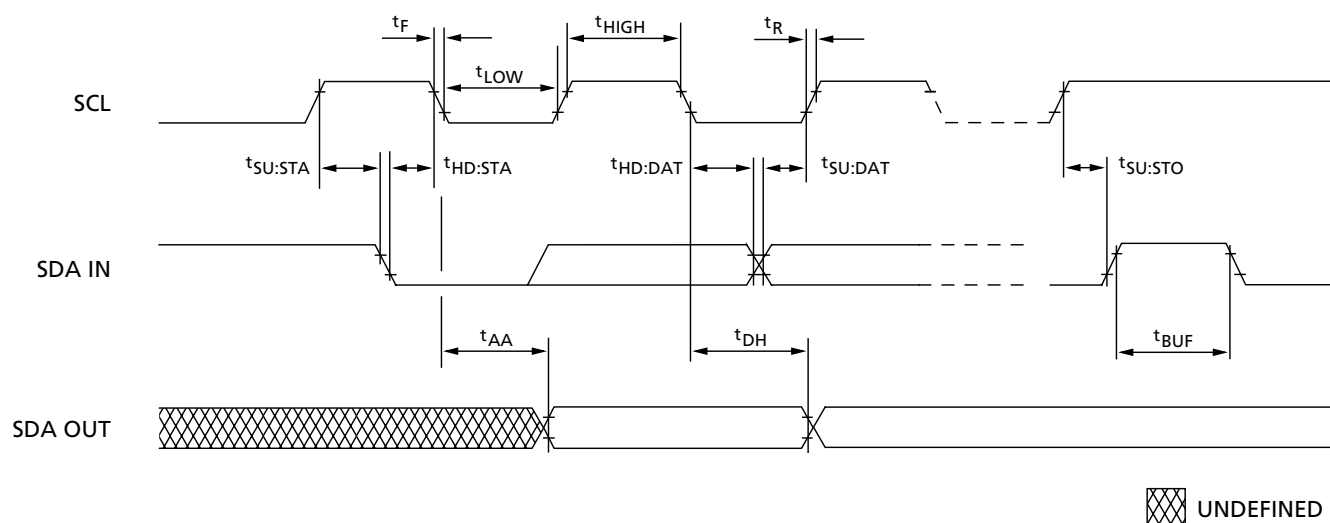
| PARAMETER/CONDITION                                         | SYMBOL       | MIN | MAX | UNITS   | NOTES |
|-------------------------------------------------------------|--------------|-----|-----|---------|-------|
| SCL LOW to SDA data-out valid                               | $t_{AA}$     | 0.3 | 3.5 | $\mu s$ |       |
| Time the bus must be free before a new transition can start | $t_{BUF}$    | 4.7 |     | $\mu s$ |       |
| Data-out hold time                                          | $t_{DH}$     | 300 |     | ns      |       |
| SDA and SCL fall time                                       | $t_F$        |     | 300 | ns      |       |
| Data-in hold time                                           | $t_{HD:DAT}$ | 0   |     | $\mu s$ |       |
| Start condition hold time                                   | $t_{HD:STA}$ | 4   |     | $\mu s$ |       |
| Clock HIGH period                                           | $t_{HIGH}$   | 4   |     | $\mu s$ |       |
| Noise suppression time constant at SCL, SDA inputs          | $t_I$        |     | 100 | ns      |       |
| Clock LOW period                                            | $t_{LOW}$    | 4.7 |     | $\mu s$ |       |
| SDA and SCL rise time                                       | $t_R$        |     | 1   | $\mu s$ |       |
| SCL clock frequency                                         | $t_{SCL}$    |     | 100 | KHz     |       |
| Data-in setup time                                          | $t_{SU:DAT}$ | 250 |     | ns      |       |
| Start condition setup time                                  | $t_{SU:STA}$ | 4.7 |     | $\mu s$ |       |
| Stop condition setup time                                   | $t_{SU:STO}$ | 4.7 |     | $\mu s$ |       |
| WRITE cycle time                                            | $t_{WRC}$    |     | 10  | ms      | 2     |

**NOTE:** 1. All voltages referenced to  $V_{SS}$ .

 2. The SPD EEPROM WRITE cycle time ( $t_{WRC}$ ) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.



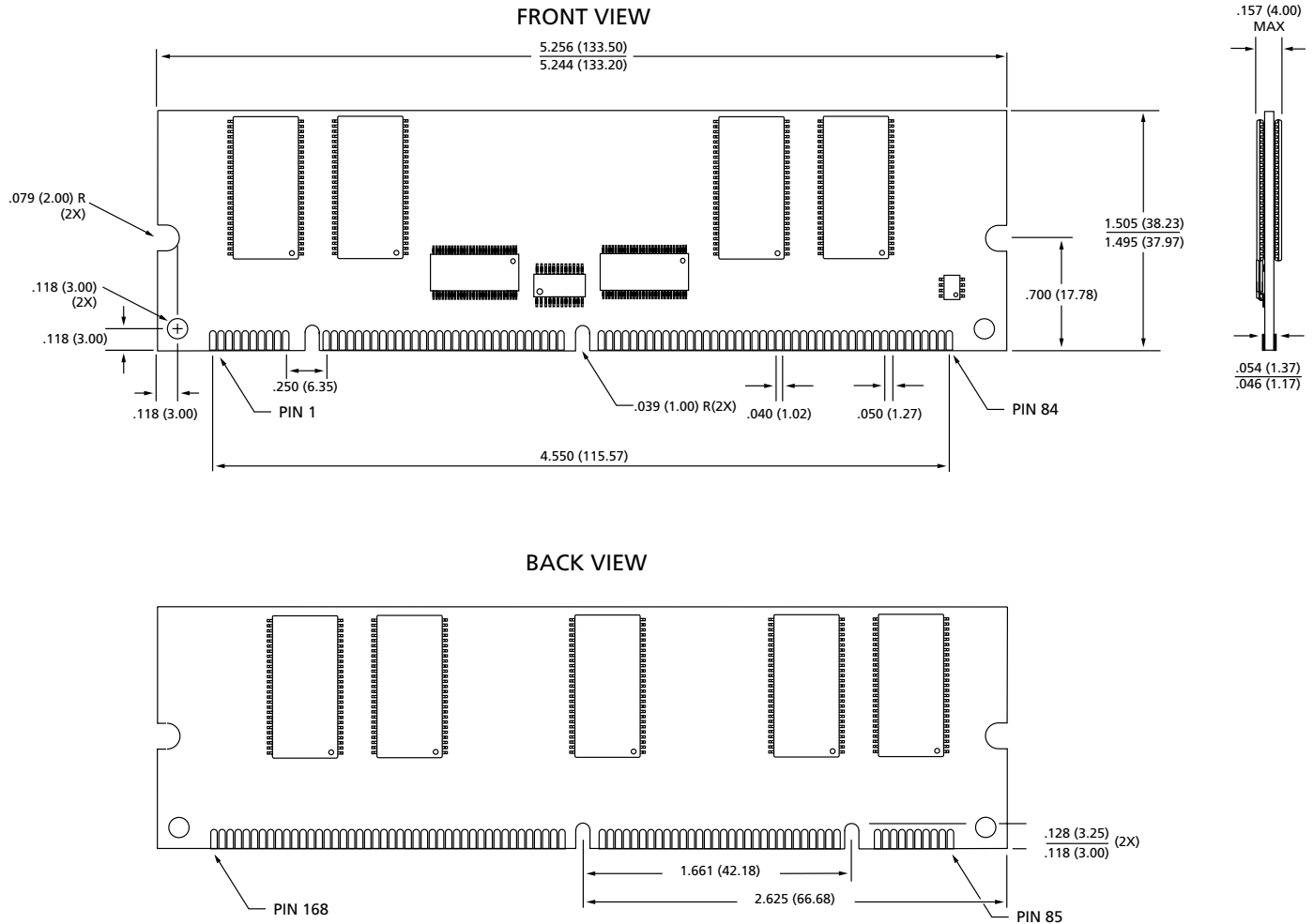
### SPD EEPROM



### SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

| SYMBOL       | MIN | MAX | UNITS   |
|--------------|-----|-----|---------|
| $t_{AA}$     | 0.3 | 3.5 | $\mu s$ |
| $t_{BUF}$    | 4.7 |     | $\mu s$ |
| $t_{DH}$     | 300 |     | ns      |
| $t_F$        |     | 300 | ns      |
| $t_{HD:DAT}$ | 0   |     | $\mu s$ |
| $t_{HD:STA}$ | 4   |     | $\mu s$ |

| SYMBOL       | MIN | MAX | UNITS   |
|--------------|-----|-----|---------|
| $t_{HIGH}$   | 4   |     | $\mu s$ |
| $t_{LOW}$    | 4.7 |     | $\mu s$ |
| $t_R$        |     | 1   | $\mu s$ |
| $t_{SU:DAT}$ | 250 |     | ns      |
| $t_{SU:STA}$ | 4.7 |     | $\mu s$ |
| $t_{SU:STO}$ | 4.7 |     | $\mu s$ |

**168-PIN DIMM  
(64MB/128MB)**


**NOTE:** 1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.



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