CMOS MT88E43B

Extended Voltage Calling Number Identification Circuit 2

Data Sheet

April 2006

Features

- Compatible with:
  - British Telecom (BT) SIN227 & SIN242
  - U.K.'s Cable Communications Association (CCA) specification TW/P&E/312
  - Bellcore GR-30-CORE (formerly known as TR-NWT-000030) & SR-TSV-002476
- Bellcore "CPE Alerting Signal (CAS)" and BT "Idle State Tone Alert Signal" detection
- Ring and line reversal detection
- 1200 baud Bell 202 and CCITT V.23 Frequency Shift Keying (FSK) demodulation
- 3 or 5 V ±10% supply voltage
- High input sensitivity (-40 dBV Tone and FSK Detection)
- Selectable 3-wire data interface (microcontroller or MT88E43 controlled)
- Low power CMOS with powerdown mode
- Input gain adjustable amplifier
- Carrier detect status output
- Uses 3.58 MHz crystal

Applications

- BT Calling Line Identity Presentation (CLIP), CCA CLIP, and Bellcore Calling Identity Delivery (CID) systems

Ordering Information

MT88E43BE	24 Pin PDIP	Tubes
MT88E43BS	24 Pin SOIC	Tubes
MT88E43BSR	24 Pin SOIC	Tape & Reel
MT88E43BS1	24 Pin SOIC*	Tubes
MT88E43BSR1	24 Pin SOIC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

- Feature phones, including Analog Display Services Interface (ADSI) phones
- Phone set adjunct boxes
- FAX and answering machines
- Database query and Computer Telephony Integration (CTI) systems

Description

The MT88E43 Calling Number Identification Circuit 2 (ECNIC2) is a low power CMOS integrated circuit intended for receiving physical layer signals transmitted according to BT (British Telecom) SIN227 & SIN242, the U.K.'s CCA (Cable Communications Association) TW/P&E/312 and Bellcore GR-30-CORE & SR-TSV-002476 specifications. The MT88E43 is suitable for applications using a fixed voltage power source between 3 and 5 V ±10%.

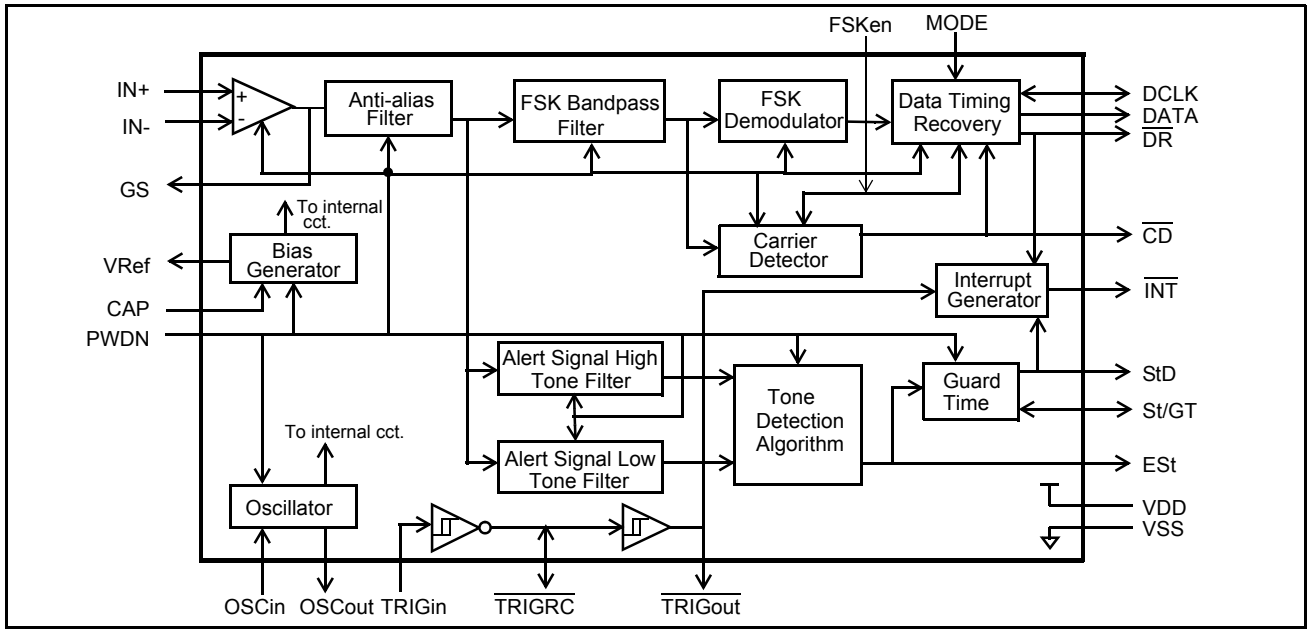

Figure 1 - Functional Block Diagram

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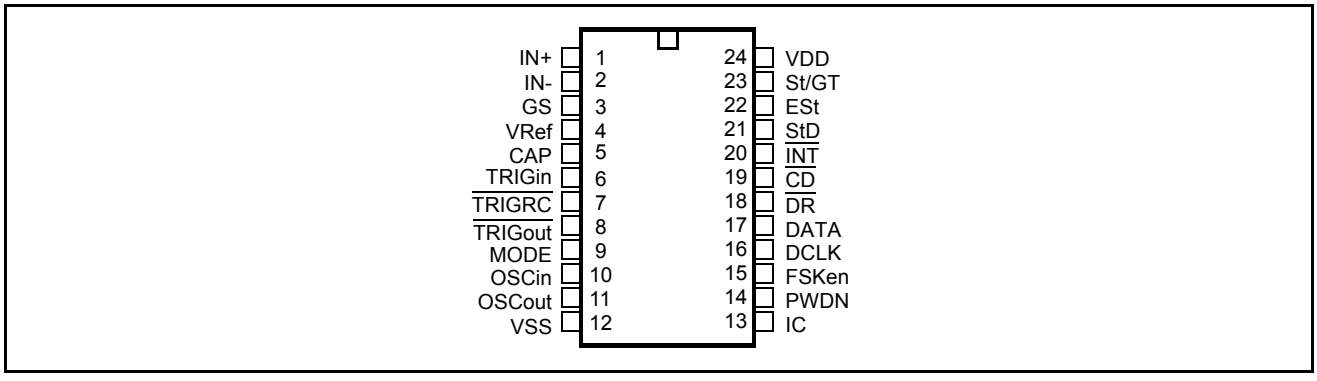


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	IN+	**Non-inverting Input** of the internal opamp.
2	IN-	**Inverting Input** of the internal opamp.
3	GS	**Gain Select (Output)** of internal opamp. The opamp's gain should be set according to the nominal Vdd of the application using the information in Figure 10.
4	V_{Ref}	**Reference Voltage (Output)**. Nominally $V_{DD}/2$. It is used to bias the input opamp.
5	CAP	**Capacitor**. A 0.1 μF decoupling capacitor should be connected across this pin and V_{SS}.
6	TRIGin	**Trigger Input**. Schmitt trigger buffer input. Used for line reversal and ring detection.
7	$\overline{\text{TRIGRC}}$	**Trigger RC (Open Drain Output/Schmitt Input)**. Used to set the (RC) time interval from TRIGin going low to $\overline{\text{TRIGout}}$ going high. An external resistor connected to V_{DD} and capacitor connected to V_{SS} determine the duration of the (RC) time interval.
8	$\overline{\text{TRIGout}}$	**Trigger Out (CMOS Output).** Schmitt trigger buffer output. Used to indicate detection of line reversal and/or ringing.
9	MODE	**3-wire interface: Mode Select (CMOS Input)**. When low, selects interface mode 0. When high, selects interface mode 1. See pin 16 (DCLK) description to understand how MODE affects the DCLK pin.
10	OSCin	**Oscillator Input**. A 3.579545 MHz crystal should be connected between this pin and OSCout. It may also be driven directly from an external clock source.
11	OSCout	**Oscillator Output**. A 3.579545 MHz crystal should be connected between this pin and OSCin. When OSCin is driven by an external clock, this pin should be left open.
12	V_{SS}	**Power Supply Ground**.
13	IC	**Internal Connection**. Must be connected to V_{SS} for normal operation.
14	PWDN	**Power Down (Schmitt Input)**. Active high. When high, the device consumes minimal power by disabling all functionality except TRIGin, $\overline{\text{TRIGRC}}$ and $\overline{\text{TRIGout}}$. Must be pulled low for device operation.
15	FSKen	**FSK Enable (CMOS Input)**. Must be high for FSK demodulation. This pin should be set low to prevent the FSK demodulator from reacting to extraneous signals (such as speech, alert signal and DTMF which are all in the same frequency band as FSK).
16	DCLK	**3-wire Interface: Data Clock (CMOS Input/Output)**. In mode 0 (MODE pin low), this pin is an output. In mode 1 (MODE pin high), this pin is an input.

Pin Description

Pin #	Name	Description
17	DATA	**3-wire Interface: Data (CMOS Output)**. In mode 0 data appears at the pin once demodulated. In mode 1 data is shifted out on the rising edge of the microcontroller supplied DCLK.
18	$\overline{DR}$	**3-wire Interface: Data Ready (CMOS Output)**. Active low. In mode 0 this output goes low after the last DCLK pulse of each data word. This identifies the 8-bit word boundary on the serial output stream. Typically, $\overline{DR}$ is used to latch 8-bit words from a serial-to-parallel converter into a microcontroller. In mode 1 this pin will signal the availability of data.
19	$\overline{CD}$	**Carrier Detect (CMOS Output)**. Active low. A logic low indicates the presence of in-band signal at the output of the FSK bandpass filter.
20	$\overline{INT}$	**Interrupt (Open Drain Output)**. Active low. It is active when $\overline{TRIGout}$ or $\overline{DR}$ is low, or StD is high. This output stays low until all three signals have become inactive.
21	StD	**Dual Tone Alert Signal Delayed Steering Output (CMOS Output)**. When high, it indicates that a guard time qualified alert signal has been detected.
22	ESt	**Dual Tone Alert Signal Early Steering Output (CMOS Output)**. Alert signal detection output. Used in conjunction with St/GT and external circuitry to implement the detect and non-detect guard times.
23	St/GT	**Dual Tone Alert Signal Steering Input/Guard Time (Analog Input/CMOS Output)**. A voltage greater than V_{TGt} (see Figure 4) at the St/GT pin causes the device to indicate that a dual tone has been detected by asserting StD high. A voltage less than V_{TGt} frees the device to accept a new dual tone.
24	V_{DD}	**Positive Power Supply**.

The MT88E43 provides all the features and functions offered by Zarlink's MT8841 (CNIC), including 1200 baud Bell 202 and CCITT V.23 FSK demodulation. The 3-wire serial data interface provided by CNIC has been enhanced to operate in two modes. In the CNIC compatible mode data transfer is initiated by the device. A second mode allows a microcontroller to extract 8-bit data words from the device. Furthermore, the MT88E43 offers Idle State Tone Alert Signal and line reversal detection capability for BT's CLIP, ring burst detection for the U.K.'s CCA's CLIP, and ring and CAS detection for Bellcore's CID.

Functional Overview

The MT88E43, Extended Voltage Calling Number Identification Circuit 2 (ECNIC2) is a device compatible with BT, the U.K.'s CCA and Bellcore specifications. As shown in Figure 1, the MT88E43 provides an FSK demodulator as well as a 3-wire serial interface similar to that of it's predecessor, the MT8841 (CNIC). The 3-wire interface has been enhanced to provide two modes of operation - a mode whereby data transfer is initiated by the device and a mode whereby data transfer is initiated by an external microcontroller.

In addition to supporting all the features and functions of the MT8841, the MT88E43 also provides line reversal detection, ring detection and dual tone alert signal/CAS detection. These new functions eliminate some external circuitry previously required with the MT8841.

The MT88E43 is compatible with the caller identity specifications of BT, the U.K.'s CCA, and Bellcore.

BT specifications SIN227 and SIN242 describe the signalling mechanism between the network and the Terminal Equipment (TE) for the Caller Display Service (CDS). CDS provides Calling Line Identity Presentation (CLIP), which delivers to an on hook (idle state) TE the identity of an incoming caller before the first ring.

An incoming CDS call is indicated by a polarity reversal on the A and B wires (see Figure 3), followed by an Idle State Tone Alert Signal. Caller ID FSK information is then transmitted in CCITT V.23 format. MT88E43 can detect the line reversal, tone alert signal, and demodulate the incoming CCITT V.23 FSK signals.

The U.K.'s CCA specification TW/P&E/312 proposes an alternate CDS TE interface. According to TW/P&E/312, data is transmitted after a single burst of ringing rather than before the first ringing cycle (as specified in the BT standards). The Idle State Tone Alert Signal is not required as it is replaced by a single ring burst. MT88E43 has the capability to detect the ring burst. It can also demodulate either Bell-202 or CCITT V.23 FSK data following the ring burst. The U.K.'s CCA specifies that data can be transmitted in either format.

Bellcore specification GR-30-CORE is the generic requirement for transmitting asynchronous voiceband data to Customer Premises Equipment (CPE). Another Bellcore specification SR-TSV-002476 describes the same requirements from the CPE's perspective. The data transmission technique specified in both documents is applicable in a variety of services like Calling Number Delivery (CND), Calling Name Delivery (CNAM) and Calling Identity Delivery on Call Waiting (CIDCW) - services promoted by Bellcore.

In CND/CNAM service, information about a calling party is embedded in the silent interval between the first and second ring burst. The MT88E43 detects the first ring burst and can then be setup to receive and demodulate the incoming Bell-202 FSK data. The device will output the demodulated data onto a 3-wire serial interface.

In CIDCW service, information about an incoming caller is sent to the subscriber, while he/she is engaged in another call. A CPE Alerting Signal (CAS) indicates the arrival of CIDCW information. The MT88E43 can detect the alert signal and then be setup to demodulate incoming FSK data containing CIDCW information.

Functional Description

Detection of CLIP/CID Call Arrival Indicators

The circuit in Figure 3 illustrates the relationship between the TRIGin, $\overline{\text{TRIGRC}}$ and $\overline{\text{TRIGout}}$ signals. Typically, the three pin combination is used to detect an event indicated by an increase of the TRIGin voltage from V_{SS} to above the Schmitt trigger high going threshold V_{T+} (see DC electrical characteristics).

Figure 3 shows a circuit to detect any one of three CLIP/CID call arrival indicators: line reversal, ring burst and ringing.

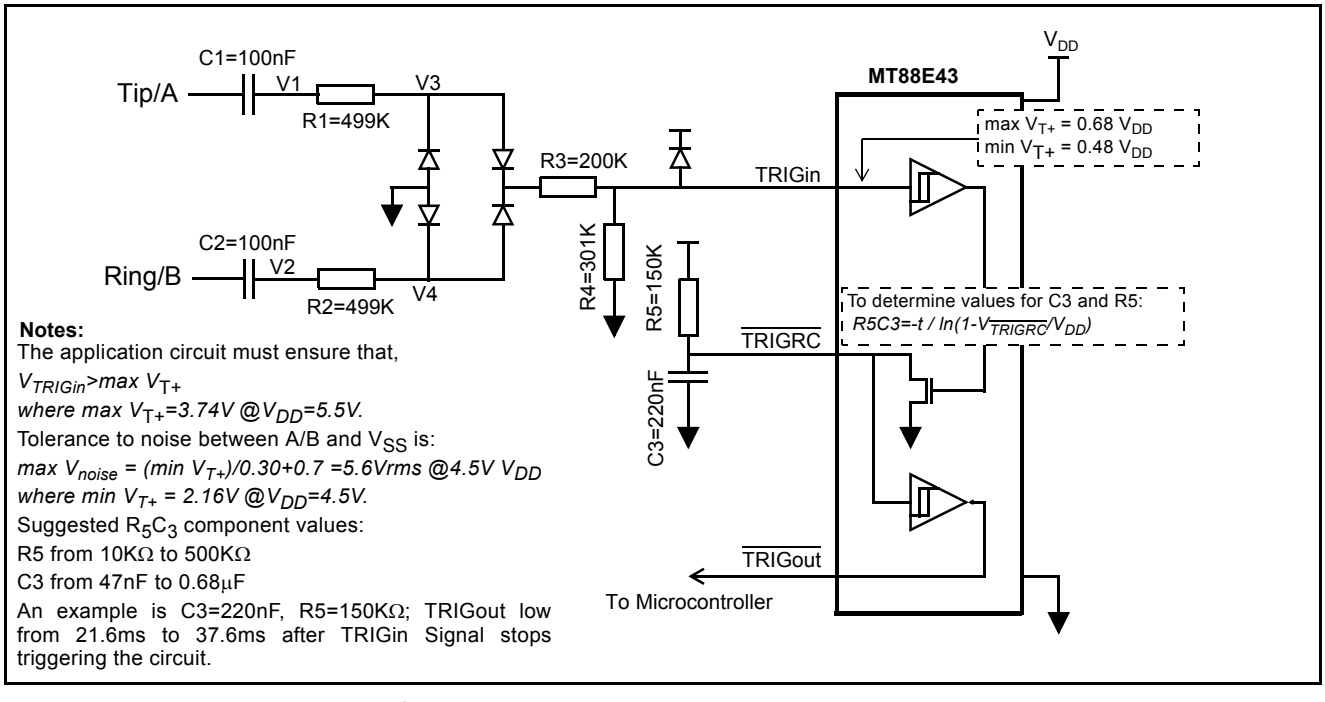


Figure 3 - Circuit to Detect Line Reversal, Ring Burst and Ringing

1. Line Reversal Detection

Line reversal, or polarity reversal on the A and B wires indicates the arrival of an incoming CDS call, as specified in SIN227. When the event (line reversal) occurs, TRIGin rises past the high going Schmitt threshold V_{T+} and $\overline{\text{TRIGout}}$, which is normally high, is pulled low. When the event is over, TRIGin falls back to below the low going Schmitt threshold V_{T-} and $\overline{\text{TRIGout}}$ returns high. The components R5 and C3 (see Figure 3) at $\overline{\text{TRIGRC}}$ ensure a minimum $\overline{\text{TRIGout}}$ low interval.

In a TE designed for CLIP, the $\overline{\text{TRIGout}}$ high to low transition may be used to interrupt or wake-up the microcontroller. The controller can thus be put into power-down mode to conserve power in a battery operated TE.

2. Ring Burst Detection

CCA does not support the dual tone alert signal (refer to Dual Tone Alert Signal Detection section). Instead, CCA requires that the TE be able to detect a single burst of ringing (duration 200-450 ms) that precedes CLIP FSK data. The ring burst may vary from 30 to 75 Vrms and is approximately 25 Hz.

Again in a TE designed for CCA CLIP, the $\overline{\text{TRIGout}}$ high to low transition may be used to interrupt or wake-up the microcontroller. The controller can thus be put into power-down mode to conserve power in a battery operated TE.

3. Ring Detection

In Bellcore's CND/CNAM scheme, the CID FSK data is transmitted between the first and second ringing cycles. The circuit in Figure 3 will generate a ring envelope signal (active low) at $\overline{\text{TRIGout}}$ for a ring voltage of at least 40 Vrms. R5 and C3 filter the ring signal to provide an envelope output.

The diode bridge shown in Figure 3 works for both single ended and balanced ringing. A fraction of the ring voltage is applied to the TRIGin input. When the voltage at TRIGin is above the Schmitt trigger high going threshold V_{T+}, $\overline{\text{TRIGRC}}$ is pulled low as C3 discharges. $\overline{\text{TRIGout}}$ stays low as long as the C3 voltage stays below the minimum V_{T+}.

In a CPE designed for CND/CNAM, the $\overline{\text{TRIGout}}$ high to low transition may be used to interrupt or wake-up the microcontroller. The controller can thus be put into power-down mode to conserve power.

If precise ring duration determination is critical, capacitor C3 in Figure 3 may be removed. The microcontroller will now be able to time the ring duration directly. The result will be that $\overline{\text{TRIGout}}$ will be low only as long as the ringing signal is present. Previously the RC time constant would cause only one interrupt.

Dual Tone Alert Signal Detection

The BT on hook (idle state) caller ID scheme uses a dual tone alert signal whose characteristics are shown in Table 1.

Bellcore specifies a similar dual tone alert signal called CPE Alerting Signal (CAS) for use in off-hook data transmission (see Table 1). Bellcore states that the CPE should be able to detect the CAS in the presence of near end speech. The CAS detector should also be immune to imitation from near and far end speech.

In the MT88E43 the dual tone alert signal is separated into a high and a low tone by two bandpass filters. A detection algorithm examines the two filter outputs to determine the presence of a dual tone alert signal. The ESt pin goes high when both tones are present. Note that ESt is only a preliminary indication. The indication must be sustained over the tone present guard time to be considered valid. Tone present and tone absent guard times can be implemented with external RC components. The tone present guard time rejects signals of insufficient duration. The tone absent guard time masks momentary detection dropout once the present guard time has been satisfied. StD is the guard time qualified detector output.

Item	BT	Bellcore
Low tone frequency	2130Hz ±1.1%	2130Hz ±0.5%
High tone frequency	2750Hz ± 1.1%	2750Hz ± 0.5%
Received signal level	-2dBV to -40dBV per tone on-hook[1] (0.22dBm[2] to -37.78dBm)	-14dBm[b] to - 32dBm per tone off-hook
Signal reject level	-46dBV (-43.78dBm)	-45dBm
Signal level differential (twist)	up to 7dB	up to 6dB
Unwanted signals	<= -20dB (300-3400Hz)	<= -7dBm ASL[3] near end speech
Duration	88ms to 110ms[4]	75ms to 85ms
Speech present	No	Yes

Table 1 - Dual Tone Alert Signal Characteristics

1. In the future BT may specify the off-hook signal level as -15 dBm to -34 dBm per tone for BT CIDCW.
2. The signal power is expressed in dBm referenced to 600 ohm at the CPE A/B (tip/ring) interface.
3. ASL = active speech level expressed in dBm referenced to 600 ohm at the CPE tip/ring interface. The level is measured according to method B of Recommendation P.56 "Objective Measurement of Active Speech Level" published in the CCITT Blue Book, volume V "Telephone Transmission Quality" 1989. EPL (Equivalent Peak Level) = ASL+11.7 dB
4. SIN227 suggests that the recognition time should be not less than 20 ms if both tones are detected.

Dual Tone Detection Guard Time

When the dual tone alert signal is detected by the MT88E43, ESt goes high. When the alerting signal ceases to be detected, ESt goes low.

The ESt pin signals raw detection of CAS/Alerting Tones. Since both Bellcore and BT applications require a minimum duration for valid signals, ESt detection must be guard time qualified. The StD pin provides guard time qualified CAS/Alerting Tone detection. When the MT88E43 is used in a caller identity system, StD indicates correct CAS/Alerting Tone detection.

Figure 4 shows the relationship between the St/GT, ESt and StD pins. It also shows the operation of a guard time circuit.

The total recognition time is $t_{REC} = t_{GP} + t_{DP}$, where t_{GP} is the tone present guard time and t_{DP} is the tone present detect time (refer to timing between ESt, St/GT and StD in Figures 17 and 20).

The total tone absent time is $t_{ABS} = t_{GA} + t_{DA}$, where t_{GA} is the tone absent guard time and t_{DA} is the tone absent detect time (refer to timing between ESt, St/GT and StD in Figures 17 and 20).

Bellcore states that it is desirable to be able to turn off CAS detection for an off-hook capable CPE. The disable switch allows the subscriber who disconnects a service that relies on CAS detection (e.g., CIDCW) but retains the CPE, to turn off the detector and not be bothered by false detection.

When SW1 in Figure 4 is in the B position the guard time circuit is disabled. The detector will still process CAS/Alerting tones but the MT88E43 will not signal their presence by ensuring StD is low.

BT specifies that the idle state tone alert signal recognition time should not be less than 20 ms when both tones are used for detection. That is, both tones must be detected together for at least 20 ms before the signal can be declared valid. This requirement can be met by setting the t_{GP} (refer to Figure 5) to at least 20 ms.

BT also specifies that the TE is required to apply a D.C. wetting pulse and an AC load 15-25 ms after the end of the alerting signal. If $t_{ABS}=t_{DA}+t_{GA}$ is 15 to 25 ms, the D.C. current wetting pulse and the A.C. load can both be applied at the falling edge of StD. The maximum t_{DA} is 8ms so t_{GA} should be 15-17 ms. Therefore, t_{GP} must be greater than t_{GA}. Figure 5(a) shows a possible implementation. The values in Figures 9 and 11 (R2=R3=422K, C=0.1μF) will meet the BT timing requirements.

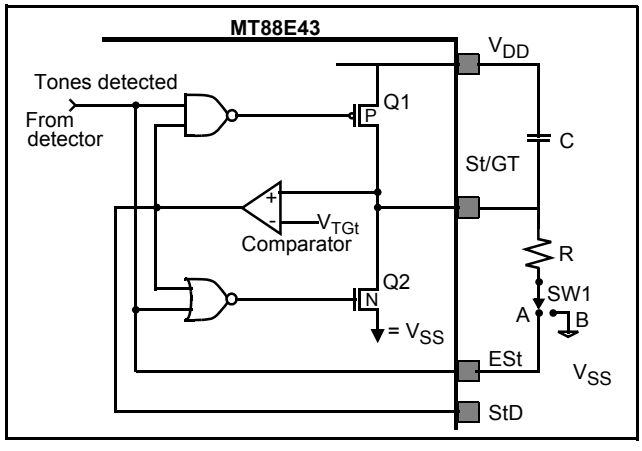


Figure 4 - Guard Time Circuit Operation

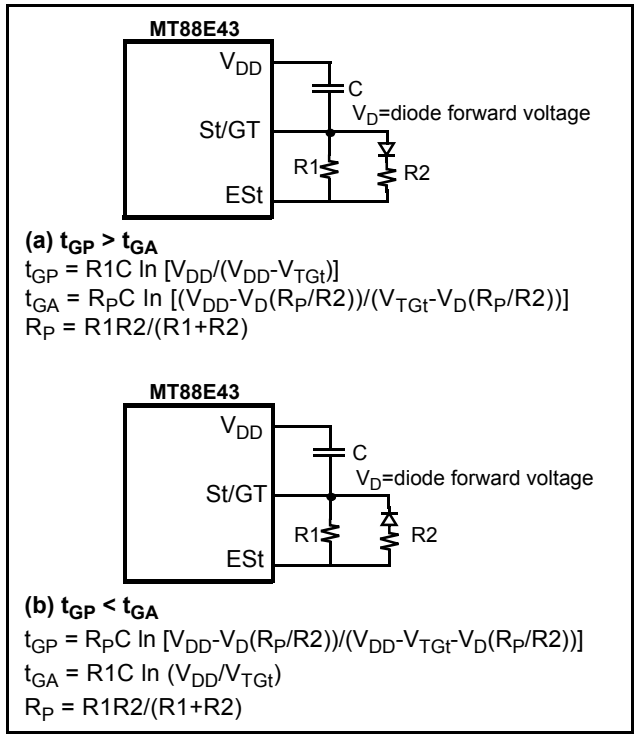


Figure 5 - Guard Time Circuits with Unequal Times

Input Configuration

The MT88E43 provides an input arrangement comprised of an operational amplifier and a bias source (V_{Ref}); which is used to bias the opamp inputs at V_{DD}/2. The feedback resistor at the opamp output (GS) can be used to adjust the gain. In a single-ended configuration, the opamp is connected as shown in Figure 6. For a differential input configuration, Figure 7 shows the necessary connections.

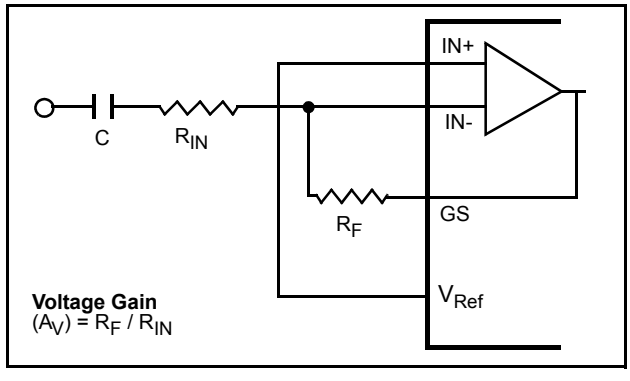


Figure 6 - Single-Ended Input Configuration

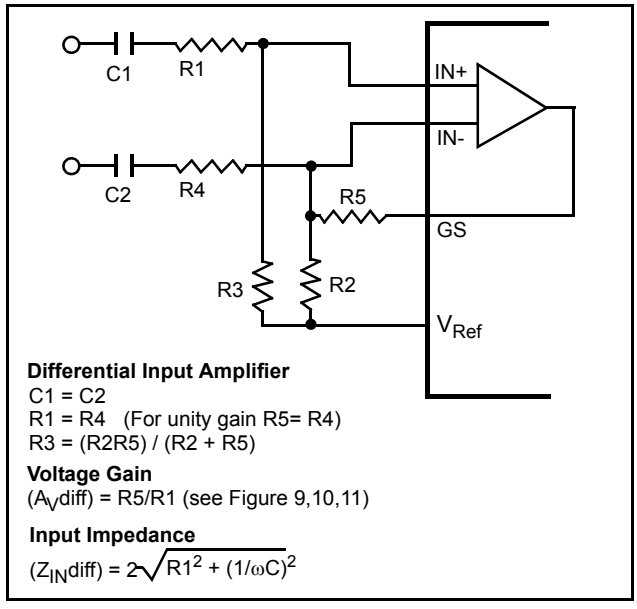


Figure 7 - Differential Input Configuration

FSK Demodulation

The MT88E43 first bandpass filters and then demodulates the incoming FSK signal. The carrier detector provides an indication of the presence of signal at the bandpass filter output. The MT88E43's dual mode 3-wire interface allows convenient extraction of the 8-bit data words in the demodulated FSK bit stream.

Note that signals such as dual tone alert signal, speech and DTMF tones lie in the same frequency band as FSK. They will, therefore, be demodulated and as a result, false data will be generated. To avoid demodulation of false data, an FSKen pin is provided so that the FSK demodulator may be disabled when FSK signal is not expected. There are two events that if either is true, should be used to disable FSKen. The events are $\overline{CD}$ returning high or receiving all the data indicated by the message length word.

Item	BT	Bellcore
Mark frequency (logic 1)	1300Hz ±1.5%	1200Hz ±1%
Space frequency (logic 0)	2100Hz ±1.5%	2200Hz ±1%
Received signal level - mark	-8dBV to -40dBV (-5.78dBm to -37.78dBm)	-12dBm[1] to -32dBm
Received signal level - space	-8dBV to -40dBV	-12dBm to -36dBm

Table 2 - FSK Characteristics

Item	BT	Bellcore
Signal level differential (twist)	up to 6dB	up to 10dB[2]
Unwanted signals	<= -20dB (300-3400Hz)	<= -25dB (0-4kHz)[3]
Transmission rate	1200 baud ±± 1%	1200 baud ±± 1%
Word format	1 start bit (logic 0), 8 bit word (LSB first), 1 to 10 stop bits (logic 1)	1 start bit (logic 0), 8 bit word (LSB first), 1 stop bit (logic 1)[4]

Table 2 - FSK Characteristics

1. The signal power is expressed in dBm referenced to 600 ohm at the CPE tip/ring (A/B) interface.
2. SR-3004,Issue 2, January 1995.
3. The frequency range is specified in GR-30-CORE.
4. Up to 20 marks may be inserted in specific places in a single or multiple data message.

The FSK characteristics described in Table 2 are listed in BT and Bellcore specifications. The BT signal frequencies correspond to CCITT V.23. The Bellcore frequencies correspond to Bell 202. The U.K.'s CCA requires that the TE be able to receive both CCITT V.23 and Bell 202, as specified in the BT and Bellcore specifications. The MT88E43 is compatible with both formats without any adjustment.

- **3-wire User Interface**

The MT88E43 provides a powerful dual mode 3-wire interface so that the 8-bit data words in the demodulated FSK bit stream can be extracted without the need either for an external UART or for the TE/CPE's microcontroller to perform the UART function in software. The interface is specifically designed for the 1200 baud rate and is comprised of the DATA, DCLK (data clock) and $\overline{DR}$ (data ready) pins. Two modes (modes 0 and 1) are selectable via control of the device's MODE pin: in mode 0, data transfer is initiated by the MT88E43; in mode 1, data transfer is initiated by the external microcontroller.

Mode 0

This mode is selected when the MODE pin is low. It is the MT8841 compatible mode where data transfer is initiated by the device.

In this mode, the MT88E43 receives the FSK signal, demodulates it, and outputs the data directly to the DATA pin (refer to Figure 14). For each received stop and start bit sequence, the MT88E43 outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each clock rising edge occurs in the centre of each DATA bit cell. DCLK is not generated for the stop and start bits. Consequently, DCLK will clock only valid data into a peripheral device such as a serial to parallel shift register or a micro-controller. The MT88E43 also outputs an end of word pulse (data ready) on the $\overline{DR}$ pin. The data ready signal indicates the reception of every 10-bit word (including start and stop bits) sent from the network to the TE/CPE. This $\overline{DR}$ signal can be used to interrupt a micro-controller. $\overline{DR}$ can also cause a serial to parallel converter to parallel load its data into a microcontroller. The mode 0 data pin can also be connected to a personal computer's serial communication port after converting from CMOS to RS-232 voltage levels.

Mode 1

This mode is selected when the MODE pin is high. In this mode, the microcontroller supplies read pulses (DCLK) to shift the 8-bit data words out of the MT88E43, onto the DATA pin. The MT88E43 asserts $\overline{DR}$ to denote the word boundary and indicate to the microprocessor that a new word has become available (refer to Figure 16).

Internal to the MT88E43, the demodulated data bits are sampled and stored. After the 8th bit, the word is parallel loaded into an 8 bit shift register and $\overline{DR}$ goes low. The shift register's contents are shifted out to the DATA pin on the supplied DCLK's rising edge in the order they were received.

If DCLK begins while $\overline{DR}$ is low, $\overline{DR}$ will return to high upon the first DCLK. This feature allows the associated interrupt (see section on "Interrupt") to be cleared by the first read pulse. Otherwise $\overline{DR}$ is low for half a nominal bit time (1/2400 sec).

After the last bit has been read, additional DCLKs are ignored.

- **Carrier Detect**

The carrier detector provides an indication of the presence of a signal in the FSK frequency band. It detects the presence of a signal of sufficient amplitude at the output of the FSK bandpass filter. The signal is qualified by a digital algorithm before the $\overline{CD}$ output is set low to indicate carrier detection. An 8ms hysteresis is provided to allow for momentary signal drop out once $\overline{CD}$ has been activated. $\overline{CD}$ is released when there is no activity at the FSK bandpass filter output for 8 ms.

When $\overline{CD}$ is inactive (high), the raw output of the demodulator is ignored by the data timing recovery circuit (refer to Figure 1). In mode 0, the DATA pin is forced high. No DCLK or $\overline{DR}$ signal is generated. In mode 1, the internal shift register is not updated. No $\overline{DR}$ is generated. If DCLK is clocked (in mode 1), DATA is undefined.

Note that signals such as dual tone alert signal, speech and DTMF tones also lie in the FSK frequency band and the carrier detector may be activated by these signals. The signals will be demodulated and presented as data. To avoid false data detection, the FSKen pin should be used to disable the FSK demodulator when no FSK signal is expected.

Ringing, on the other hand, does not pose a problem as it is ignored by the carrier detector.

Interrupt

To facilitate interfacing with microcontrollers running interrupt driven firmwear, an open drain interrupt output $\overline{INT}$ is provided. $\overline{INT}$ is asserted when $\overline{TRIGout}$ is low, StD is high, or $\overline{DR}$ is low. When $\overline{INT}$ is asserted, these signals should be read (through an input port of the microcontroller) to determine the cause of the interrupt ($\overline{TRIGout}$, StD or $\overline{DR}$) so that the appropriate response can be made.

When system power is first applied, $\overline{TRIGout}$ will be low because capacitor C3 at $\overline{TRIGRC}$ (see Figure 3) has no initial charge. This will result in an interrupt upon power up. Also when system power is first applied and the PWDN pin is low, an interrupt will occur due to StD. Since there is no charge across the capacitor at the St/GT pin in Figure 4, StD will be high triggering an interrupt. The interrupts will not clear until both capacitors are charged. The microcontroller should ignore interrupt from these sources on initial power up until there is sufficient time to charge the capacitors.

It is possible to clear StD and its interrupt by asserting PWDN immediately after system power up. When PWDN is high, StD is low. PWDN will also force both ESt and the comparator output low, Q2 will turn on so that the capacitor at the St/GT pin charges up quickly (refer to Figure 4).

Power Down Mode

For applications requiring reduced power consumption, the MT88E43 can be powered up only when it is required, that is, upon detection of one of three CLIP/CID call arrival indicators: line reversal, ring burst and ringing.

The MT88E43 is powered down by asserting the PWDN pin. In powerdown mode, the crystal oscillator, opamp and all internal circuitry, except for TRIGin, $\overline{TRIGRC}$ and $\overline{TRIGout}$ pins, are disabled. The three TRIG pins are not affected by power down, such that, the MT88E43 can still react to call arrival indicators. The MT88E43 can be powered up by grounding the PWDN pin.

Crystal Oscillator

The MT88E43 requires a 3.579545MHz crystal oscillator as the master timing source.

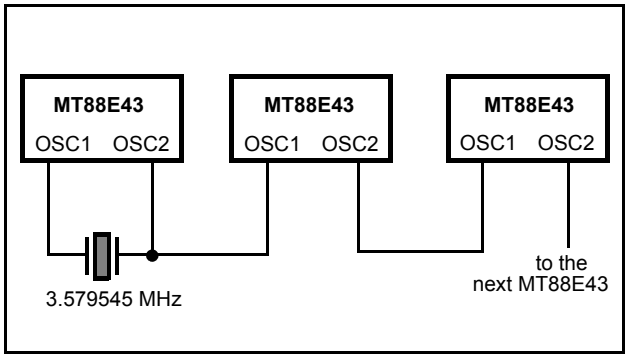


Figure 8 - Common Crystal Connection

The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency tolerance:	±0.1%(-40°C+85°C)
Resonance mode:	Parallel
Load capacitance:	18 pF
Maximum series resistance:	150 ohms
Maximum drive level (mW):	2 mW

e.g., CTS MP036S

Any number of MT88E43 devices can be connected as shown in Figure 8 such that only one crystal is required. The connection between OSC2 and OSC1

can be D.C. coupled as shown, or the OSC1 input on all devices can be driven from a CMOS buffer (dc coupled) with the OSC2 outputs left unconnected.

To meet BT and Bellcore requirements for proper tone detection the crystal must have a frequency tolerance of 0.1%.

VRef and CAP Inputs

V_{Ref} is the output of a low impedance voltage source equal to $V_{DD/2}$ and is used to bias the input opamp. A 0.1μF capacitor is required between CAP and V_{SS} to eliminate noise on $V_{Ref.}$

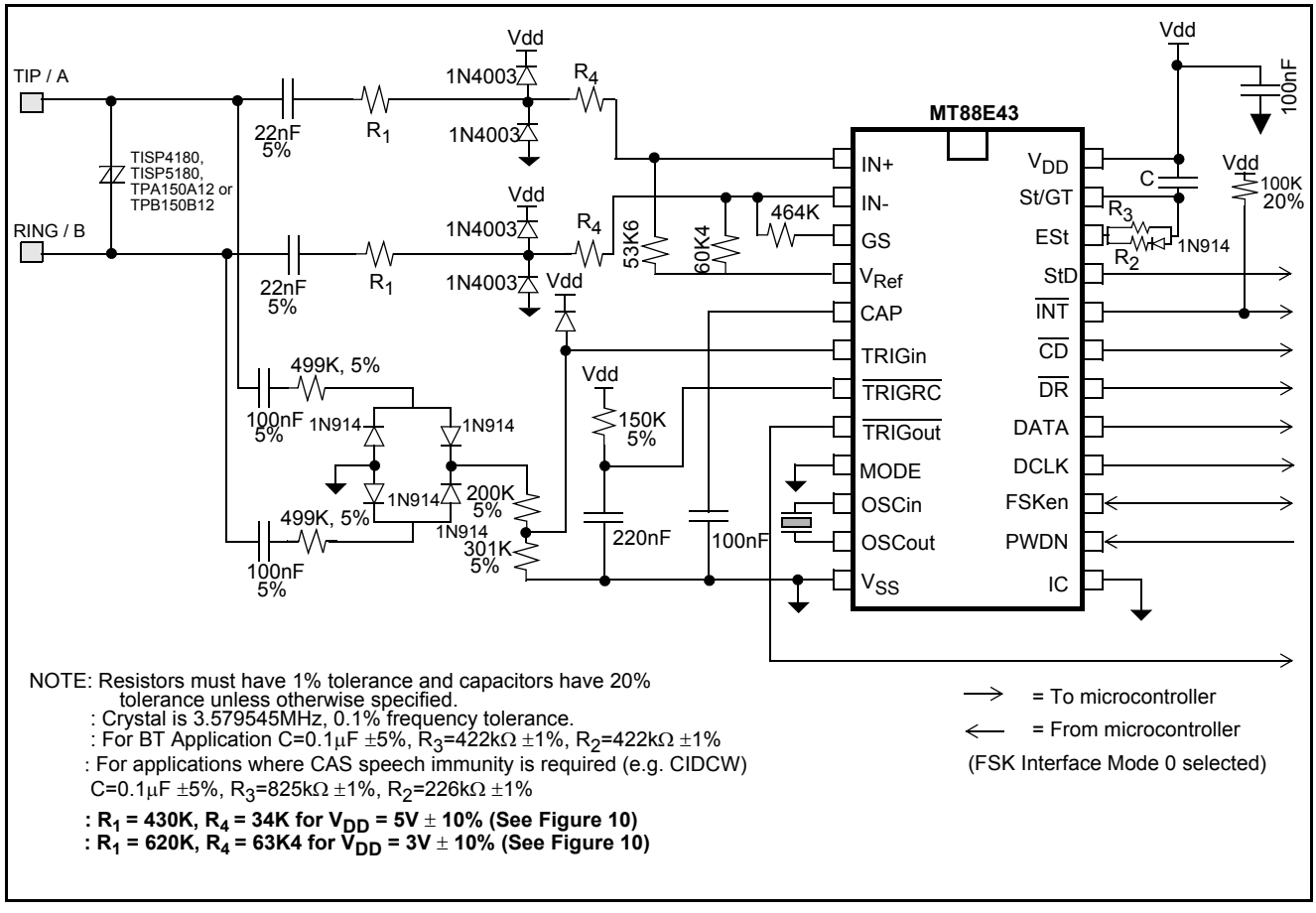


Figure 9 - Application Circuit

Application Circuits

The circuits shown in Figures 9 and 11 are application circuits for the MT88E43. As supply voltage (V_{DD}) is decreased, the threshold of the device's tone and FSK detectors will be reduced. Therefore, to meet the BT or Bellcore tone reject level requirements the gain of the internal opamp should be reduced according to the graph in Figure 10. For example when V_{DD}=5V (+/- 10%), R_1 should equal 430 kΩ and R_4 should equal 34 kΩ; and if V_{DD}=3V (+/- 10%) R_1 should equal 620 kΩ and R_4 should equal 63.4 kΩ. Resistors R_1 and R_4 are shown in Figures 9 and 11.

The circuit shown in Figure 9 illustrates the use of the MT88E43 in a proprietary system that doesn't need to meet FCC, DOC, and UL approvals. It should be noted that if glitches on the tip/ring interface are of sufficient amplitude, the circuit will falsely detect these signals as ringing or line reversal.

The circuit shown in Figure 11 will provide common mode rejection of signals received by the ringing circuit. This circuit should pass safety related tests specified by FCC Part 68, DOC CS-03, UL 1459, and CSA C22.2. These safety tests will simulate high voltage faults that may occur on the line. The circuit provides isolation from these high voltage faults via R1 and the 12 k1Ω resistors as well as the 22 nF & 330 nF capacitors. IRC manufactures a resistor (part number GS3) that should be used for R1. This resistor is a 3 W, 5%, 1 kV power resistor. The 12 k1 resistor is manufactured by IRC (part number FA8425F). This resistor is a 1.5 W, 5%, fuseable type resistor. The 22 nF and 330 nF capacitors have a 400 V rating.

See the application note "MSAN-164: Applications of the MT8843 Calling Number Identification Circuit 2" for information on designing the MT88E43 into CID and CIDCW systems.

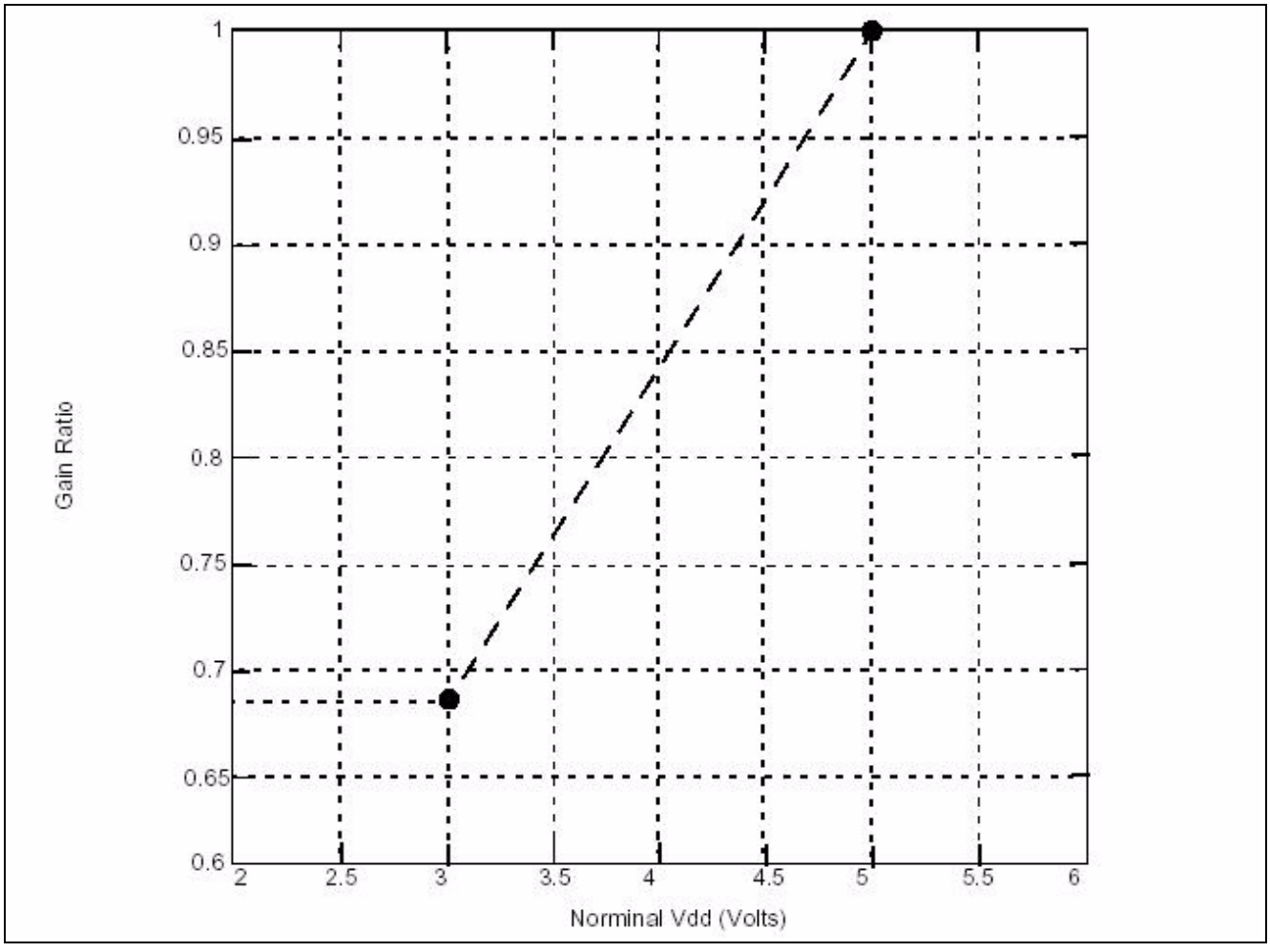


Figure 10 - Gain Ratio as a function of Nominal Vdd

Note: In the application circuits shown in Figures 9 and 11, the Gain Ratio of MT88E43 opamp is

$$\text{GainRatio} = \frac{464\text{k}\Omega}{R_1 + R_4}$$

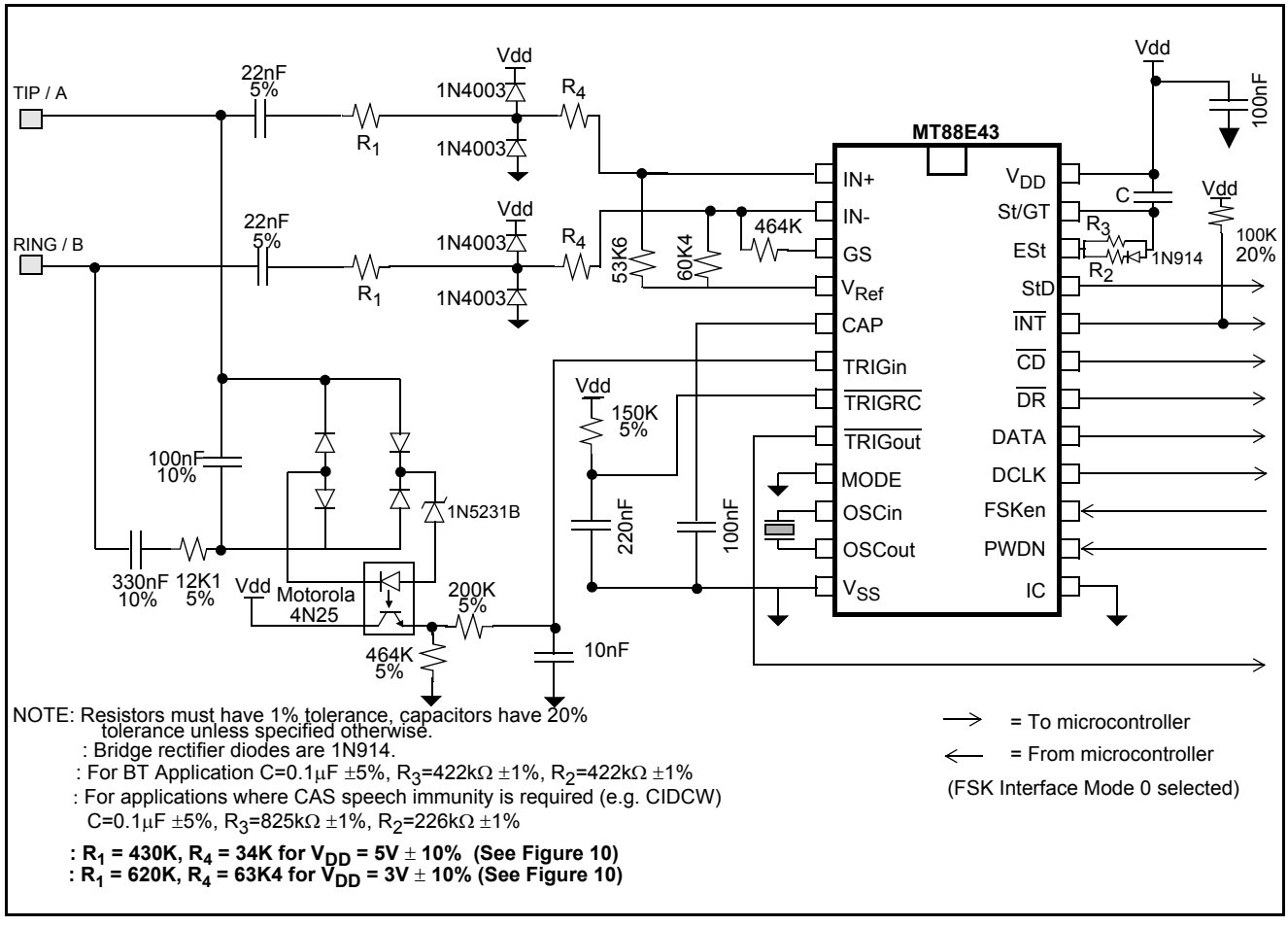


Figure 11 - Application Circuit with Improved Common Mode Noise Immunity and Isolation in Line Interface

Approvals

FCC Part 68, DOC CS-03, UL 1459, and CAN/CSA-22.2 No. 225-M90 are all system (i.e. connectors, power supply, cabinet, etc.) requirements. Since the MT88E43 is a component and not a system, the application circuit (Figure 11) has been designed to meet the CO Trunk interface requirements of FCC, DOC, UL, and CSA; thus enabling the complete system to be approved by these standards bodies.

Products are designed in accordance with meeting the above requirements; however, full conformance to these standards is dependent upon the application in which the MT88E43 is being used, and therefore, approvals are the responsibility of the customer and Zarlink will not have tested the product to meet the above standards.

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage with respect to V_{ss}	V_{DD}	-0.3	6	V
2	Voltage on any pin other than supplies **	V_{PIN}	V_{ss}-0.3	V_{DD}+0.3	V
3	Current at any pin other than supplies	I_{PIN}		10	mA
4	Storage Temperature	T_{ST}	-65	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
** Under normal operating conditions voltage on any pin except supplies can be minimum V_{SS}-1V to maximum V_{DD}+1V for an input current limited to less than 200 μA

.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Power Supplies	V_{DD}	2.7	-	5.5	V
2	Clock Frequency	f_{OSC}		3.579545		MHz
3	Tolerance on Clock Frequency	Δfc	-0.1		+0.1	%
4	Operating Temperature	T_{OP}	-40		85	°C

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUPPLY	Standby Supply Current	I_{DDQ}		0.5	15	μA	All inputs are V_{DD}/V_{SS} except for oscillator pins. No analog input. outputs unloaded. PWDN=V_{DD}
2		Operating Supply Current V_{DD} = 5V ±10% V_{DD} = 3V ±10%	I_{DD}		 4.7 2.5	 8 4.5	 mA mA	All inputs are V_{DD}/V_{SS} except for oscillator pins. No analog input. outputs unloaded. PWDN=V_{SS} FSKen=V_{DD}
3		Power Consumption	PO			44	mW	
4	$\overline{\text{TRIGin}}$, $\overline{\text{TRIGRC}}$, PWDN	Schmitt Input High Threshold	V_{T+}	0.48*V_{DD}		0.68*V_{DD}	V	
		Schmitt Input Low Threshold	V_{T-}	0.28*V_{DD}		0.48*V_{DD}	V	
5		Schmitt Hysteresis	V_{HYS}	0.2			V	
6	DCLK, MODE, FSKen	CMOS Input High Voltage	V_{IH}	0.7*V_{DD}		V_{DD}	V	
		CMOS Input Low Voltage	V_{IL}	V_{SS}		0.3*V_{DD}	V	

DC Electrical Characteristics† (continued)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
7	$\overline{\text{TRIGout}}$, DCLK, DATA, $\overline{\text{DR}}$, $\overline{\text{CD}}$, StD, ESt, St/GT	Output High Sourcing Current	I_{OH}	0.8			mA	V_{OH}=0.9*V_{DD}
8	$\overline{\text{TRIGout}}$, DCLK, DATA, $\overline{\text{DR}}$, $\overline{\text{CD}}$, StD, ESt, St/GT $\overline{\text{TRIGRC}}$, $\overline{\text{INT}}$	Output Low Sinking Current	I_{OL}	2			mA	V_{OL}=0.1*V_{DD}
9	IN+, IN-, TRIGin	Input Current	Iin1			1	µA	V_{in}=V_{DD} to V_{SS}
	PWDN, DCLK, MODE, FSKen		Iin2			10	µA	V_{in}=V_{DD} to V_{SS}
10	$\overline{\text{TRIGRC}}$	Output High-Impedance Current	Ioz1			1	µA	V_{out} =V_{DD} to V_{SS}
11	$\overline{\text{INT}}$		Ioz2			10	µA	
12	St/GT		Ioz3			5	µA	
13	V_{Ref}	Output Voltage	V_{Ref}	$0.5V_{DD}$ - 0.05		$0.5V_{DD}$+ 0.05	V	No Load
14		Output Resistance	R_{Ref}			2	kΩ	
15	St/GT	Comparator Threshold Voltage	V_{TGt}	$0.5V_{DD}$- 0.05		$0.5V_{DD}$+ 0.05	V	

† DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Dual Tone Alert Signal Detection

	Characteristic	Sym.	Min.	Typ.‡	Max.	Unit	Notes*
1	Low tone frequency	f_L	-	2130	-	Hz	
2	High tone frequency	f_H	-	2750	-	Hz	
3	Frequency deviation accept		1.1%	-	-		range within which tones are accepted
4	Frequency deviation reject		3.5%	-	-		ranges outside of which tones are rejected
5	Accept signal level per tone		-40 -37.78	-	-2 0.22	dBV[1] dBm[2]	See Note 3

AC Electrical Characteristics† - Dual Tone Alert Signal Detection

	Characteristic	Sym.	Min.	Typ.‡	Max.	Unit	Notes*
6	Reject signal level per tone		-	-	-46 -43.78	dBV dBm	See Note 3
7	Positive and negative twist accept		7	-	-	dB[3]	
8	Signal to Noise Ratio	SNR_{TONE}	20	-	-	dB	1,2

1. dBV = decibels above or below a reference voltage of 1Vrms. Signal level is per tone.
2. dBm = decibels above or below a reference power of 1mW into 600 ohms, 0 dBm = 0.7746Vrms. Signal level is per tone.
3. Twist = 20 log (f_H amplitude / f_L amplitude).

***Notes:**
1. Both tones have the same amplitude.
2. Band limited random noise 300-3400Hz. Measurement valid only when tone is present.
3. With gain setting as shown in Figure 10. Production tested at 3V ±10%, 5V ±10%.

=AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym	Level	Units	Notes
1	CMOS Threshold Voltage	V_{CT}	$0.5*V_{DD}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7*V_{DD}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3*V_{DD}$	V	

Electrical Characteristics† - Gain Setting Amplifier

	Characteristics	Sym.	Min.	Max.	Units	Test Conditions
1	Input Leakage Current	I_{IN}		1	μA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input Resistance	R_{in}	10		MΩ	
3	Input Offset Voltage	V_{OS}		25	mV	
4	Power Supply Rejection Ratio	PSRR	40		dB	1kHz ripple on V_{DD}
5	Common Mode Rejection	CMRR	40		dB	$V_{CMmin} \le V_{IN} \le V_{CMmax}$
6	DC Open Loop Voltage Gain	A_{VOL}	30		dB	
7	Unity Gain Bandwidth	f_C	0.3		MHz	
8	Output Voltage Swing	V_O	0.5	V_{DD}-0.5	V_{pp}	Load ≥ 50kΩ
9	Maximum Capacitive Load (GS)	C_L		100	pF	
10	Maximum Resistive Load (GS)	R_L	50		kΩ	
11	Common Mode Range Voltage	V_{CM}	1.0	V_{DD}-1.0	V	

† Electrical characteristics are over recommended operating conditions, unless otherwise stated.

AC Electrical Characteristics† - FSK Detection

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	Input Detection Level		-40 -37.78 10.0		-8 -5.78 398.1	dBV[1] dBm[2] mVrms	1,3
2	Transmission Rate		1188	1200	1212	baud	
3	Input Frequency Detection Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	
4	Signal to Noise Ratio	SNR_{FSK}	20			dB	1,2

1. dBV = decibels above or below a reference voltage of 1 Vrms.
2. dBm = decibels above or below a reference power of 1mW into 600 ohms. 0 dBm = 0.7746 Vrms.

*Notes
1. Both mark and space have the same amplitude.
2. Band limited random noise (200-3400Hz). Present when FSK signal is present. Note that the BT band is 300-3400Hz, the Bellcore band is 0-4kHz.
3. Production tested at V_{DD}=3V ±10%, 5V ±10%.

† AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are nominal values and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Dual Tone Alert Signal Timing

	Characteristics	Sym	Min	Max	Units	Notes*
1	Alert Signal present detect time	t_{DP}	0.5	10	ms	1
2	Alert Signal absent detect time	t_{DA}	0.1	8	ms	1

*Notes
1. Refer to Figures 1716 and 19

AC Electrical Characteristics† - 3-Wire Interface Timing

		Characteristics	Sym.	Min.	Max.	Units	Notes
1	PWDN OSC1	Power-up time	t_{PU}		50	ms	
2		Power-down time	t_{PD}		1	ms	
3	$\overline{CD}$	Input FSK to $\overline{CD}$ low delay	t_{CP}		25	ms	
4		Input FSK to $\overline{CD}$ high delay	t_{CA}	8		ms	
5		Hysteresis		8		ms	

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - 3-Wire Interface Timing (Mode 0)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	$\overline{DR}$	Rise time	t_{RR}			200	ns	into 50 pF Load
2		Fall time	t_{RF}			200	ns	into 50 pF Load
3		Low time	t_{RL}	415	416	417	µs	2
4	DATA	Rate		1188	1200	1212	baud	1
5		Input FSK to DATA delay	t_{IDD}		1	5	ms	
6	DATA DCLK	Rise time	t_R			200	ns	into 50 pF Load
7		Fall time	t_F			200	ns	into 50 pF Load
8		DATA to DCLK delay	t_{DCD}	6	416		µs	1, 2, 3
9		DCLK to DATA delay	t_{CDD}	6	416		µs	1, 2, 3
10	DCLK	Frequency	f_{DCLK0}	1201.6	1202.8	1204	Hz	2
11		High time	t_{CH}	415	416	417	µs	2
12		Low time	t_{CL}	415	416	417	µs	2
13	DCLK $\overline{DR}$	DCLK to $\overline{DR}$ delay	t_{CRD}	415	416	417	µs	2

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*Notes:
1. FSK input data at 1200 ±12 baud.
2. OSC1 at 3.579545 MHz ±0.1%.
3. Function of signal condition.

AC Electrical Characteristics† - 3-Wire Interface Timing (Mode 1)

		Characteristics	Sym.	Min.	Max.	Units	Notes
1	DCLK	Frequency	f_{DCLK1}		1	MHz	
2		Duty cycle		30	70	%	
3		Rise time	t_{R1}		20	ns	
4	DCLK, $\overline{DR}$	DCLK low set up to $\overline{DR}$	t_{DDS}	500		ns	
5		DCLK low hold time after $\overline{DR}$	t_{DDH}	500		ns	

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

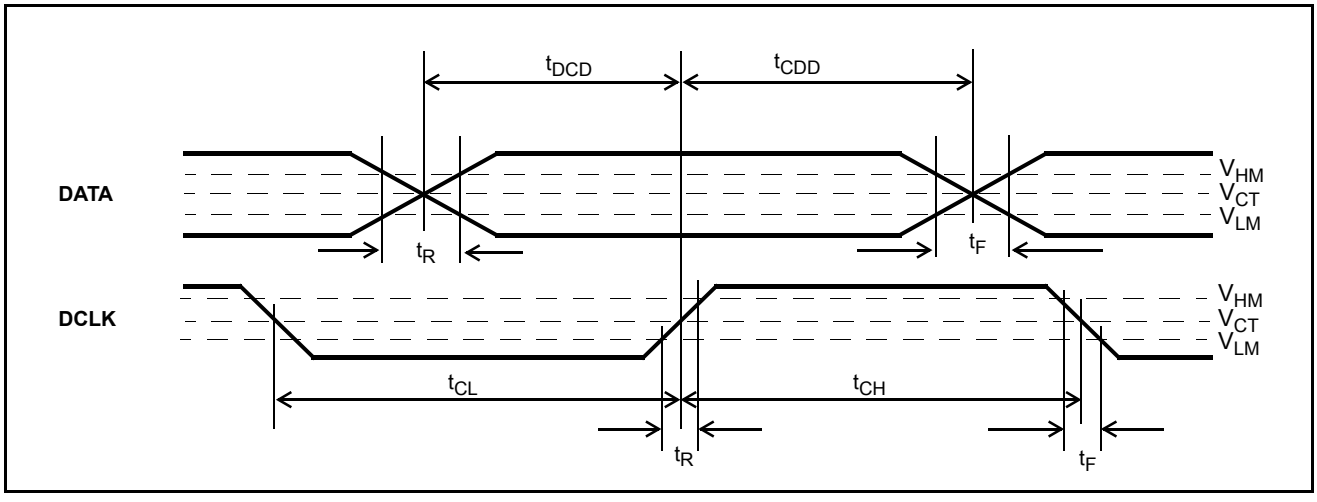


Figure 12 - DATA and DCLK Mode 0 Output Timing

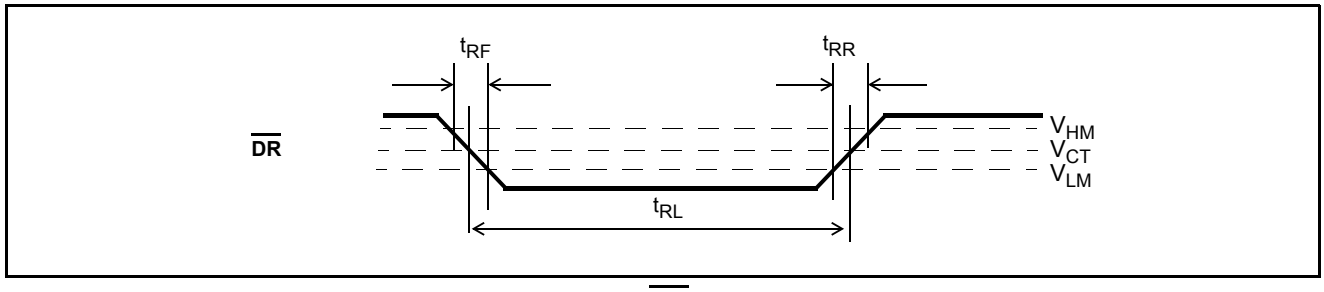


Figure 13 - $\overline{\text{DR}}$ Output Timing

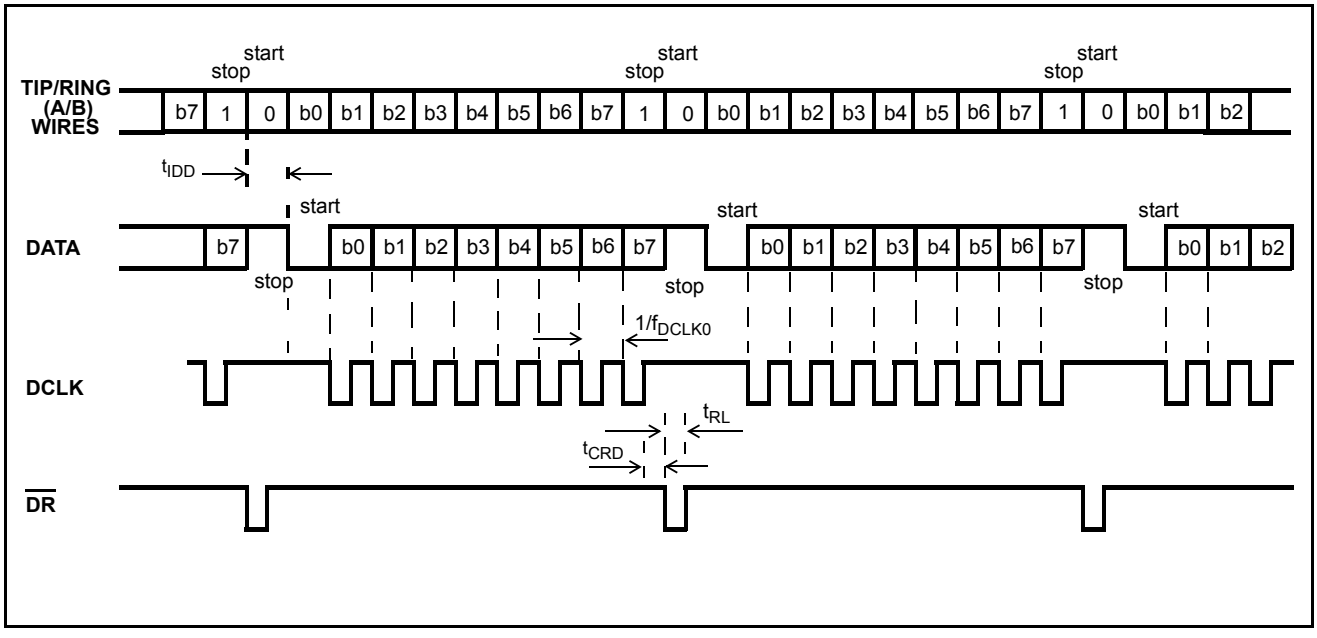


Figure 14 - Serial Data Interface Timing (MODE 0)

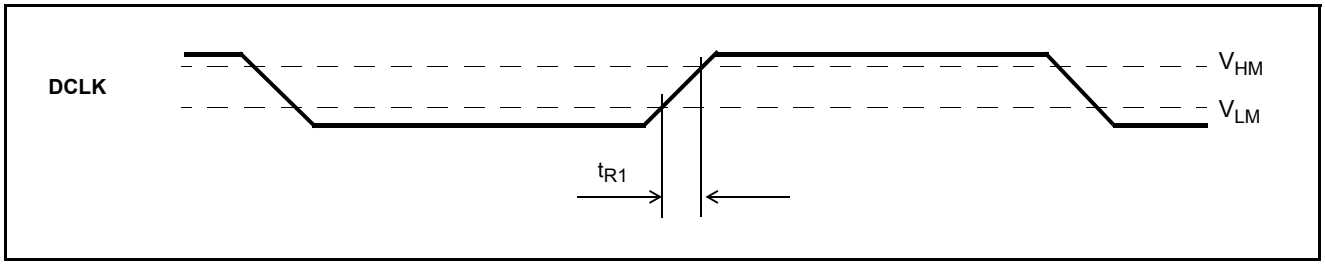


Figure 15 - DCLK Mode 1 Input Timing

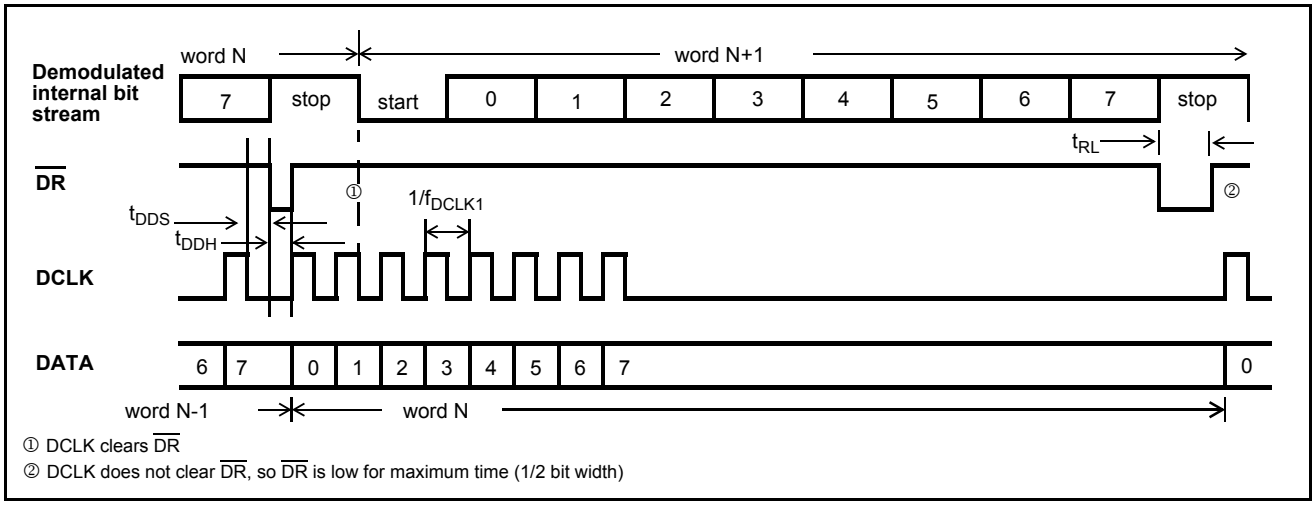


Figure 16 - Serial Data Interface Timing (Mode 1)

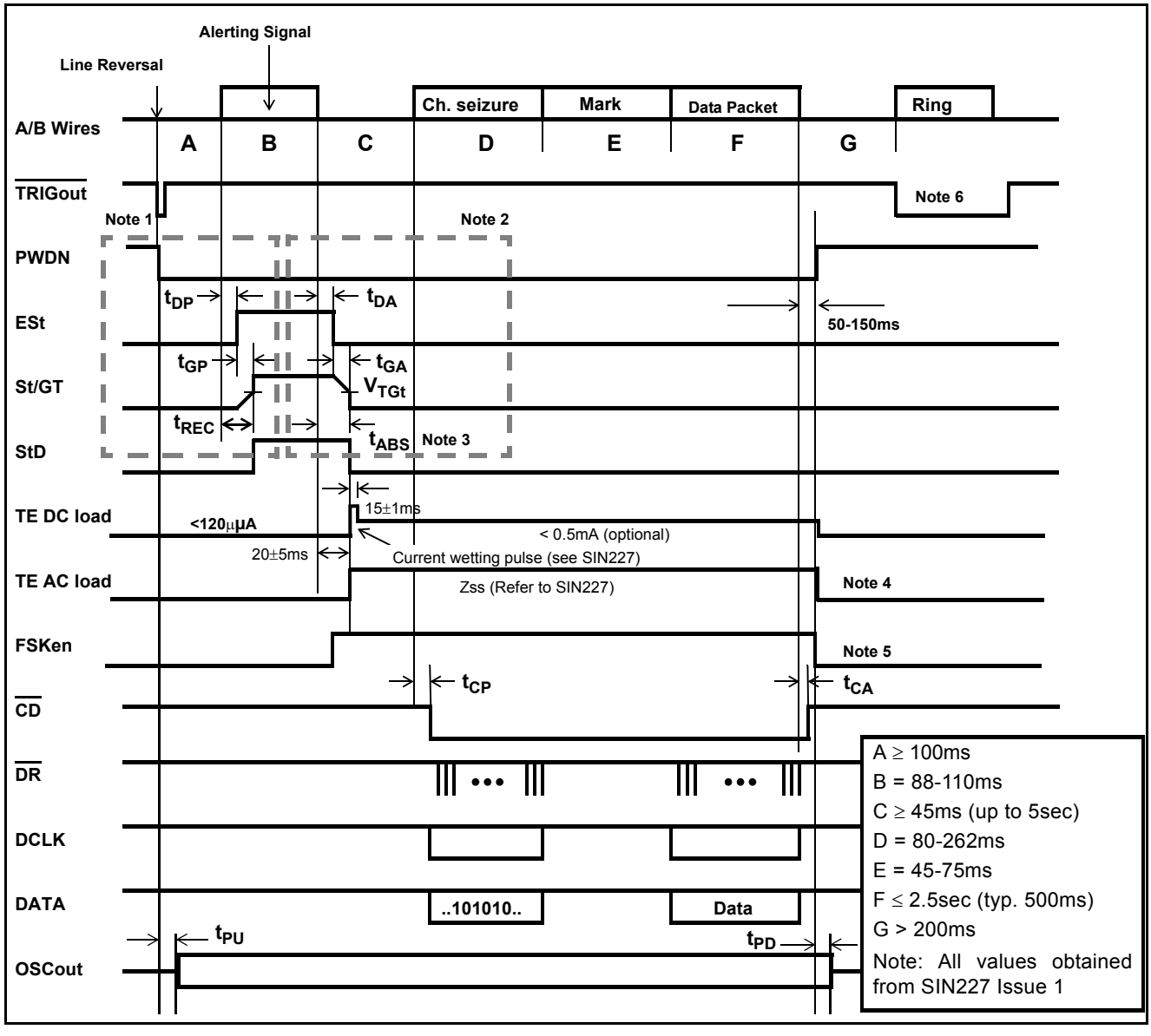


Figure 17 - Input and Output Timing for BT Caller Display Service (CDS), e.g., CLIP

Notes:

1) The total recognition time is $t_{REC} = t_{GP} + t_{DP}$, where t_{GP} is the tone present guard time and t_{DP} is the tone present detect time (refer to section "Dual Tone Detection Guard Time" on page 6 for details). V_{TGt} is the comparator threshold (refer to Figure 4).
2) The total tone absent time is $t_{ABS} = t_{GA} + t_{DA}$, where t_{GA} is the tone absent guard time and t_{DA} is the tone absent detect time (refer to section "Dual Tone Detection Guard Time" on page 6 for details). V_{TGt} is the comparator threshold (refer to Figure 4).
3) By choosing t_{GA}=15ms, t_{ABS} will be 15-25 ms so that the current wetting pulse and AC load can be applied right after the StD falling edge.
4) SIN227 specifies that the AC and DC loads should be removed between 50-150 ms after the end of the FSK signal, indicated by $\overline{CD}$ returning to high. The MT88E43 may also be powered down at this time.
5) FSKen should be set low when FSK is not expected to prevent the FSK demodulator from reacting to other in-band signals such as speech, tone alert signal and DTMF tones.
6) $\overline{TRIGout}$ is the ring envelope during ringing.

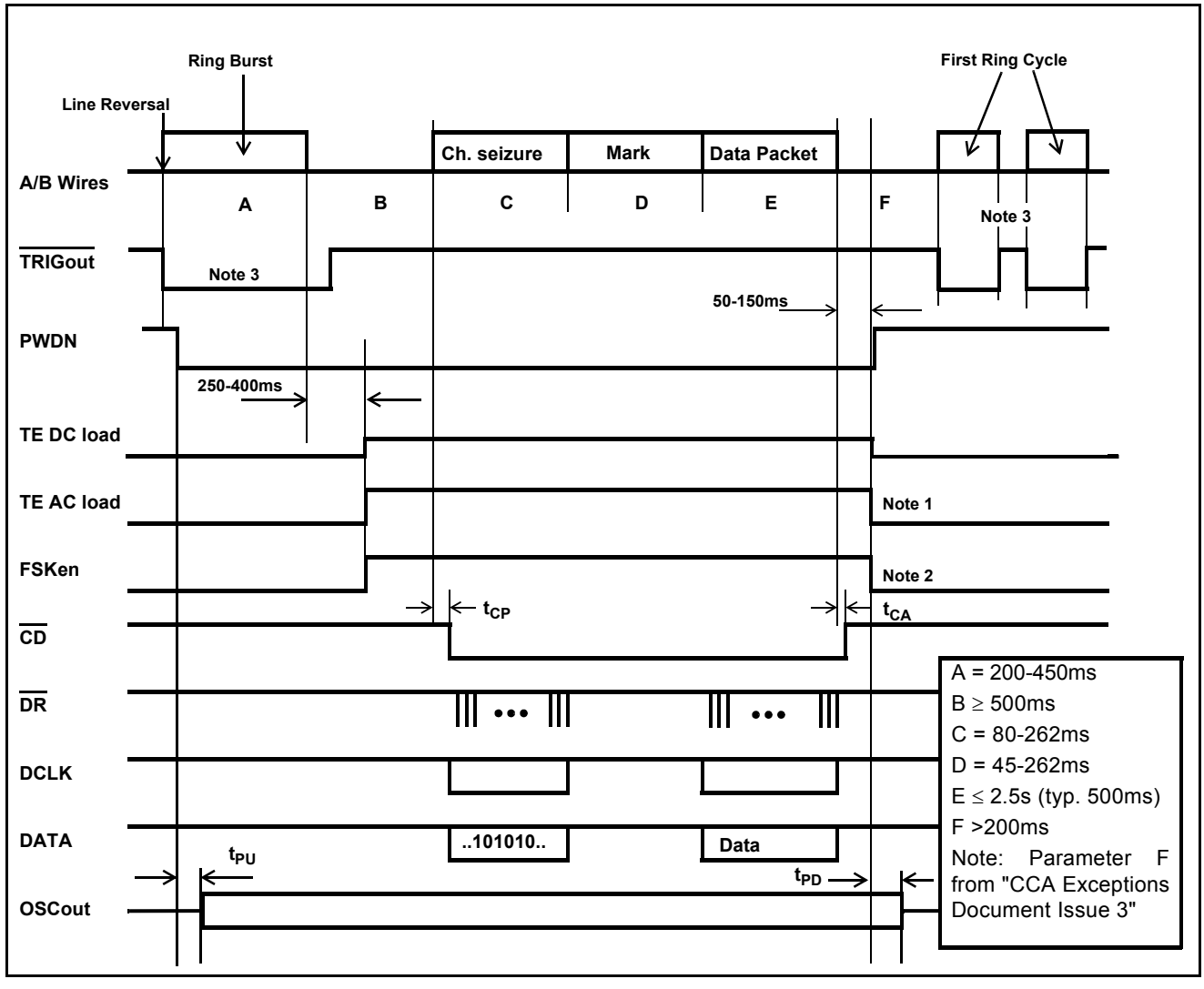


Figure 18 - Input and Output Timing for CCA Caller Display Service (CDS), e.g., CLIP

Notes:
1) TW/P&E/312 specifies that the AC and DC loads should be removed between 50 to 150 ms after the end of the FSK signal, indicated by CD returning to high. The MT88E43 may also be powered down at this time.
2) FSKen should be set low when FSK is not expected to prevent the FSK demodulator from reacting to other in-band signals such as speech, and DTMF tones.
3) TRIGout represents the ring envelope during ringing.

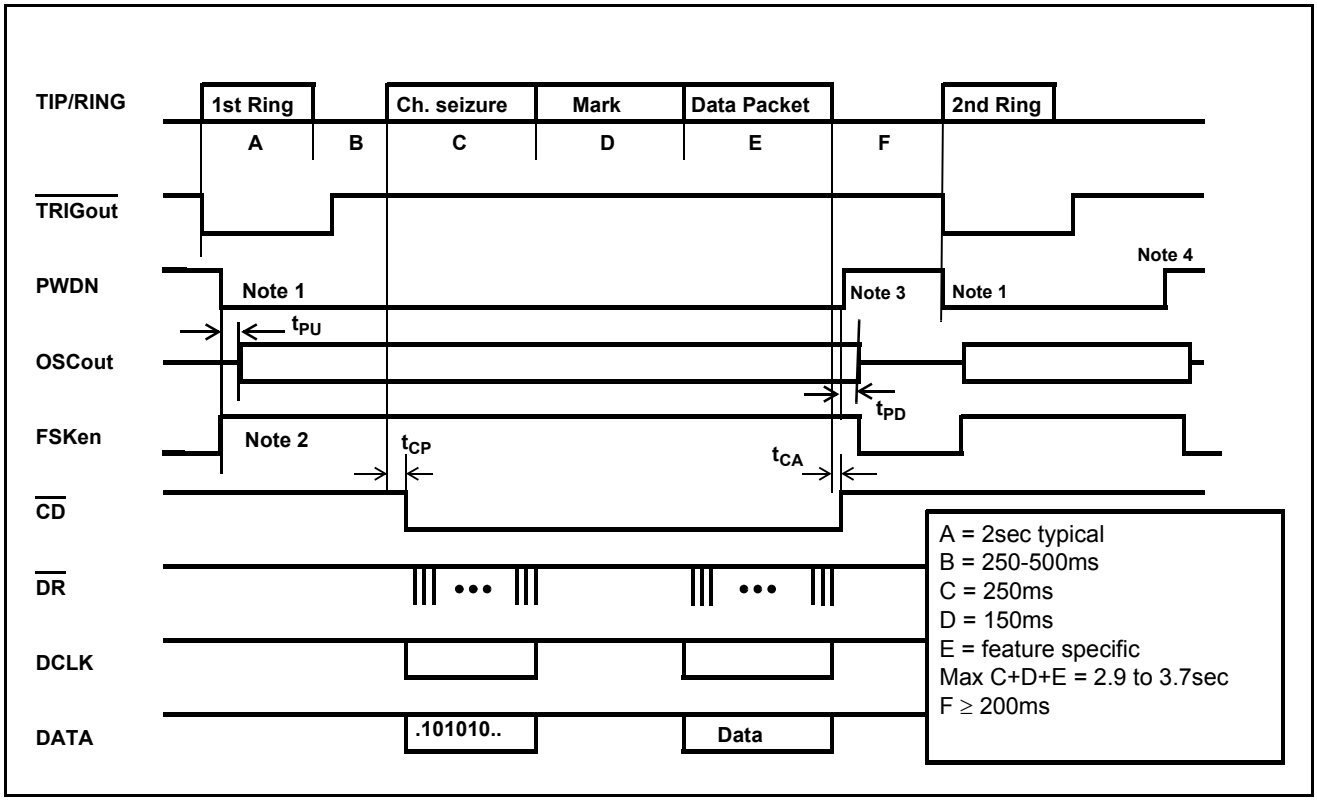


Figure 19 - Input and Output Timing for Bellcore On-hook Data Transmission Associated with Ringing, e.g., CID

Notes:
This on-hook case application is included because a CIDCW (off-hook) CPE should also be capable of receiving on-hook data transmission (with ringing) from the end office. TR-NWT-000575 specifies that CIDCW will be offered only to lines which subscribe to CID.

1) The CPE designer may choose to enable the MT88E43 only after the end of ringing to conserve power in a battery operated CPE. $\overline{CD}$ is not activated by ringing.
2) The CPE designer may choose to set FSKen always high while the CPE is on-hook. Setting FSKen low prevents the FSK demodulator from reacting to other in-band signals such as speech, CAS or DTMF tones.
3) The microcontroller in the CPE powers down the MT88E43 after $\overline{CD}$ has become inactive.
4) The microcontroller times out if $\overline{CD}$ is not activated.

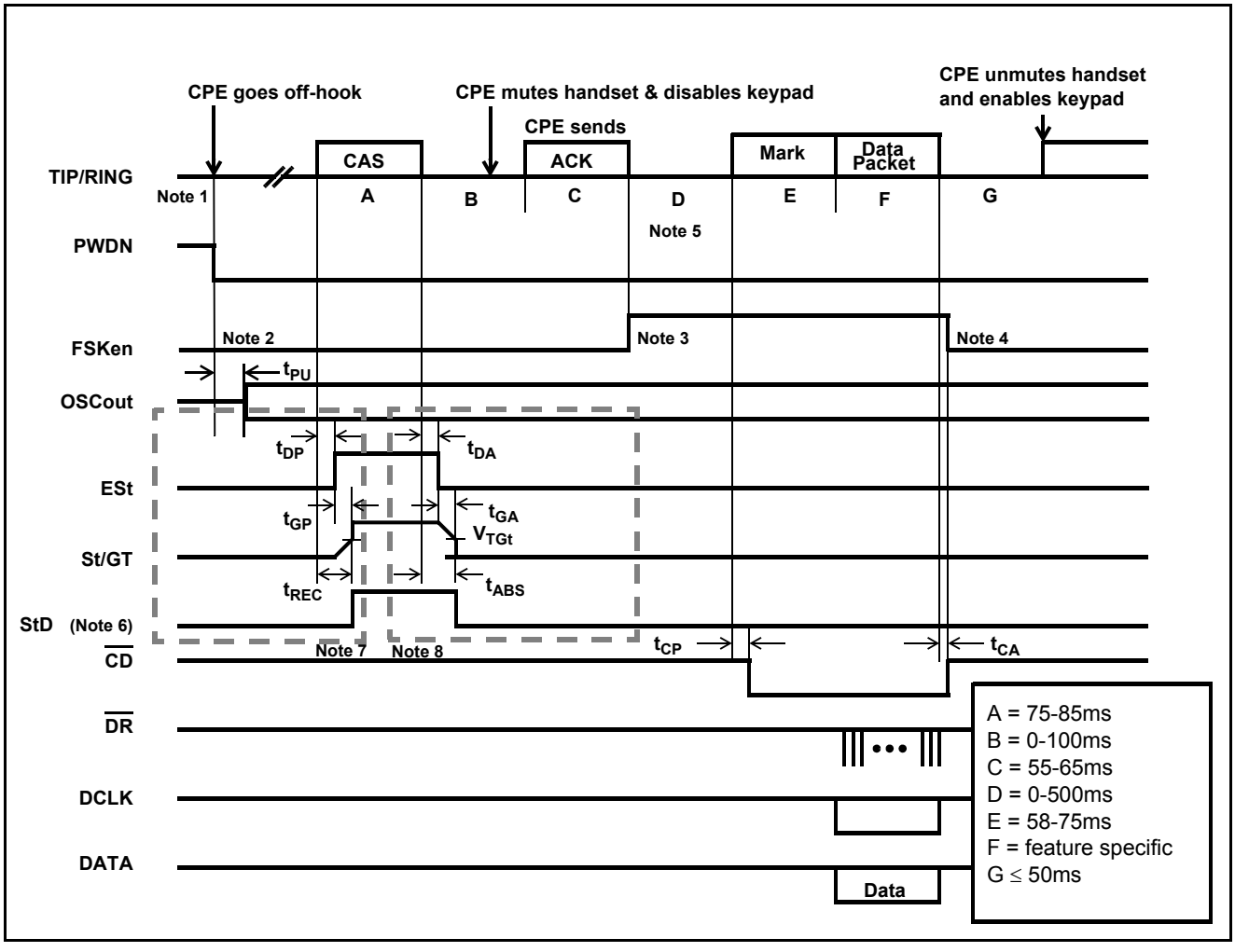
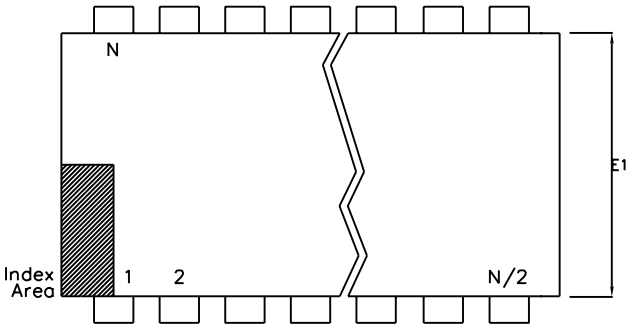
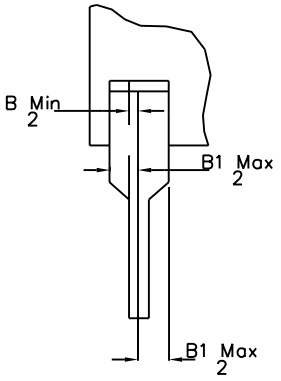


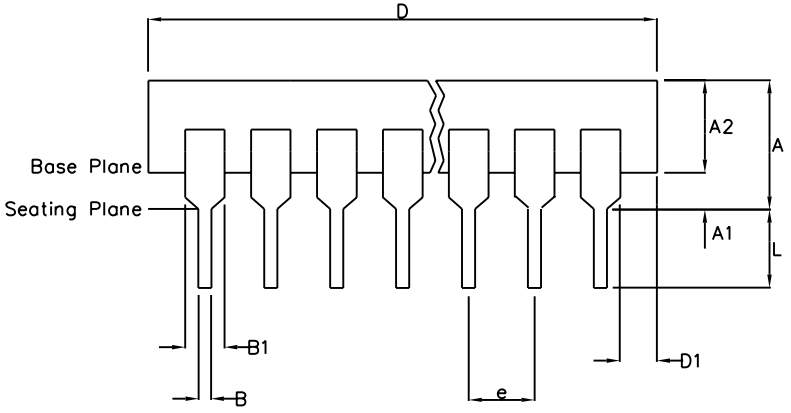
Figure 20 - Input and Output Timing for Bellcore Off-hook Data Transmission, e.g., CIDCW

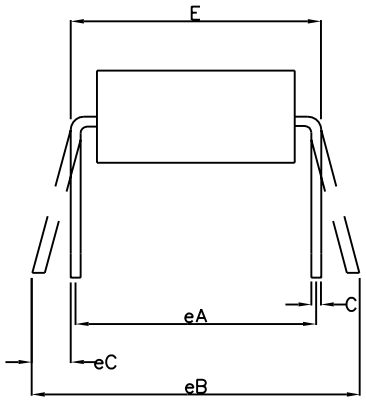
Notes:

1) In a CPE where AC power is not available, the designer may choose to switch over to line power when the CPE goes off-hook and use battery power while on-hook. The CPE should also be CID (on-hook) capable because TR-NWT-000575 specifies that CIDCW will be offered only to lines which subscribe to CID.
2) Non-FSK signals such as CAS, speech and DTMF tones are in the same frequency band as FSK. They will be demodulated and give false data. The FSKen pin should be set low to disable the FSK demodulator when FSK is not expected.
3) FSKen may be set high as soon as the CPE has finished sending the acknowledgment signal ACK. TR-NWT-000575 specifies that ACK = DTMF D for non-ADSI CPE, A for ADSI CPE.
4) FSKen should be set low when $\overline{CD}$ has become inactive.
5) In an unsuccessful attempt where the end office does not send the FSK signal, the CPE should unmute the handset and enable the keypad after this interval.
6) SR-TSV-002476 states that it is desirable that the CPE have an on/off switch for the CAS detector. See SW1 in Figure 4.
7) The total recognition time is $t_{REC} = t_{GP} + t_{DP}$, where t_{GP} is the tone present guard time and t_{DP} is the tone present detect time (refer to section “Dual Tone Detection Guard Time” on page 6 for details). V_{TGt} is the comparator threshold (refer to Figure 4).
8) The total tone absent time is $t_{ABS} = t_{GA} + t_{DA}$, where t_{GA} is the tone absent guard time and t_{DA} is the tone absent detect time (refer to section “Dual Tone Detection Guard Time” on page 6 for details). V_{TGt} is the comparator threshold (refer to Figure 4).









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	29.21	32.77	1.150	1.290
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	24		24	
Conforms to Jedec MS-011AA ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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ZARLINK SEMICONDUCTOR

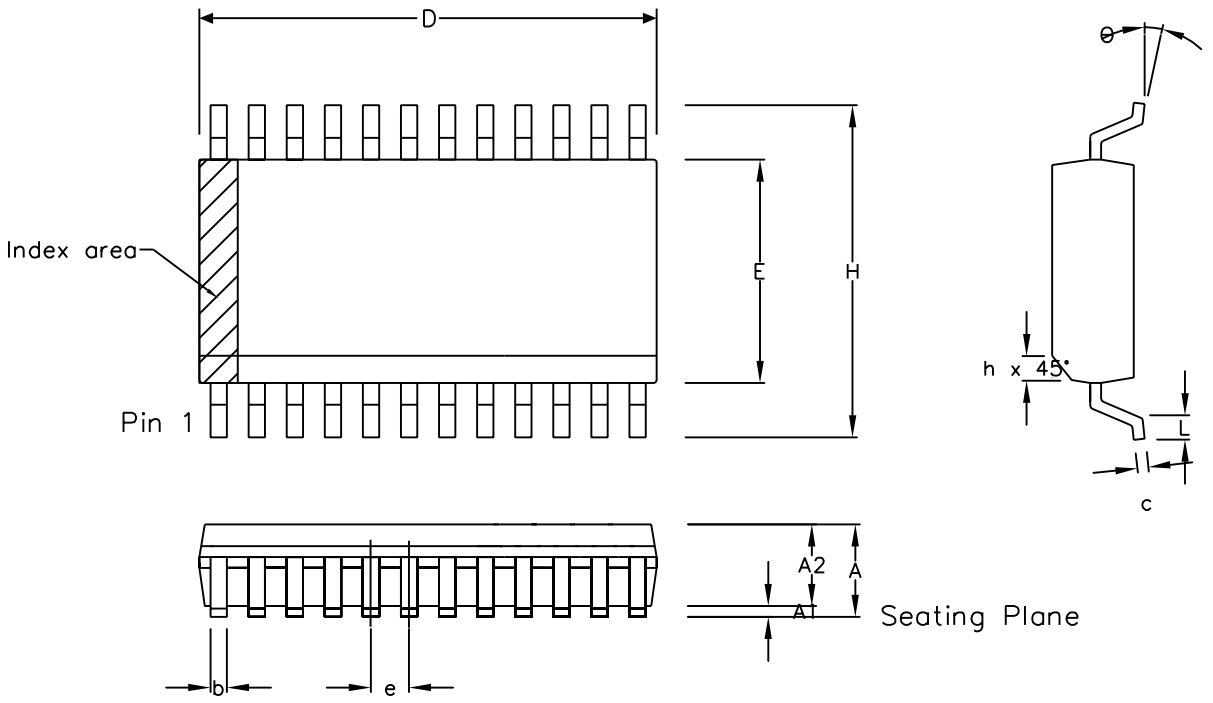
Previous package codes

DP / E

Package Code DA

Package Outline for 24 lead PDIP

GPD00071



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	15.20		15.60		0.599		0.614
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	24						
Conforms to JEDEC MS-013AD Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 24 lead SOIC (0.300" Body Width)

GPD00016



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