DDR2 SDRAM Unbuffered DIMM

MT16HTF6464A – 512MB

MT16HTF12864A – 1GB

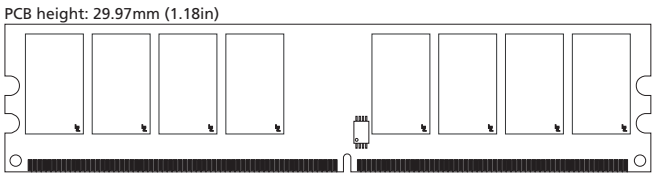
MT16HTF25664A – 2GB

For component specifications, refer to the Micron's Web site: www.micron.com/ddr2

Features

- 240-pin, unbuffered, dual in-line memory module (UDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 512MB (64 Meg x 64), 1GB (128 Meg x 64), and 2GB (256 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +1.8V
- V_{DDSPD} = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

Figure 1: 240-Pin DIMM (MO-237 R/C "B")



Options — Marking

- Package
  - 240-pin DIMM (lead-free) — Y
- Frequency/CL[1]
  - 2.5ns @ CL = 5 (DDR2-800)[2] — -80E
  - 3.0ns @ CL = 5 (DDR2-667)[3] — -667
  - 3.75ns @ CL = 4 (DDR2-533) — -53E
  - 5.0ns @ CL = 3 (DDR2-400) — -40E
- PCB height
  - 29.97mm (1.18in)

Notes: 1. CL = CAS (READ) latency.
2. Not available in 512MB density.
3. Not available in 2GB density.

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Table 1: Address Table

	512MB	1GB	2GB
Refresh count	8K	8K	8K
Row addressing	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column addressing	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module rank addressing	2 (S0#, S1#)	2 (S0#, S1#)	2 (S0#, S1#)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4	CL = 5			
-80E	–	533	800	12.5	12.5	55
-667	400	533	667	15	15	55
-53E	400	533	–	15	15	55
-40E	400	400	–	15	15	55

Table 3: Part Numbers and Timing Parameters

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT16HTF6464AY-667__	512MB	64 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF6464AY-53E__	512MB	64 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF6464AY-40E__	512MB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT16HTF12864AY-80E__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16HTF12864AY-667__	1GB	128 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF12864AY-53E__	1GB	128 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF12864AY-40E__	1GB	128 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT16HTF25664AY-80E__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16HTF25664AY-667__	2GB	256 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF25664AY-53E__	2GB	256 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF25664AY-40E__	2GB	256 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16HTF12864AY-80ED4.

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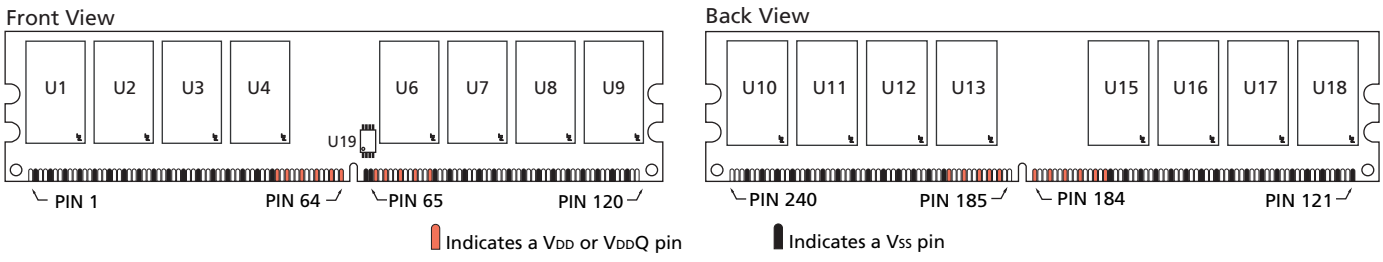
Pin Assignments and Descriptions

Table 4: Pin Assignment

240-pin DIMM Front								240-pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC	156	NC	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	CK2
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	NC	191	VDDQ	221	CK2#
12	DQ8	42	NC	72	VDDQ	102	NC	132	DQ13	162	NC	192	RAS#	222	VSS
13	DQ9	43	NC	73	WE#	103	VSS	133	VSS	163	VSS	193	S0#	223	DM6
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1	164	DM8	194	VDDQ	224	NC
15	DQS1#	45	NC	75	VDDQ	105	DQS6	135	NC	165	NC	195	ODT0	225	VSS
16	DQS1	46	NC	76	S1#	106	VSS	136	VSS	166	VSS	196	NC/A13	226	DQ54
17	VSS	47	VSS	77	ODT1	107	DQ50	137	CK1	167	NC	197	VDD	227	DQ55
18	NC	48	NC	78	VDDQ	108	DQ51	138	CK1#	168	NC	198	VSS	228	VSS
19	NC	49	NC	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4	232	DM7
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC	233	NC
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	NC	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

Note: Pin 196 is NC for 512MB, or A13 for 1GB and 2GB; pin 54 is NC for 512MB and 1GB, or BA2 for 2GB.

Figure 2: Pin Locations



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Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Table 4 on page 3 for more information

Pin Numbers	Symbol	Type	Description
77, 195	ODT0, ODT1	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
137, 138, 185, 186, 220, 221	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
52, 171	CKE0, CKE1	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all device banks idle), or ACTIVE power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level when V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, V_{REF} must be maintained to this input.
76, 193	S0#, S1#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
73, 74, 192	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
54 (2GB), 71, 190	BA0, BA1, BA2 (2GB)	Input	Bank address inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LMR command.
57, 58, 60, 61, 63, 70, 176, 177, 179, 180, 182, 183, 188, 196 (1GB, 2GB)	A0–A12 (512MB) A0–A13 (1GB, 2GB)	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the precharge applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LMR command.
125, 134, 146, 155, 202, 211, 223, 232	DM0–DM7	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.

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Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Table 4 on page 3 for more information

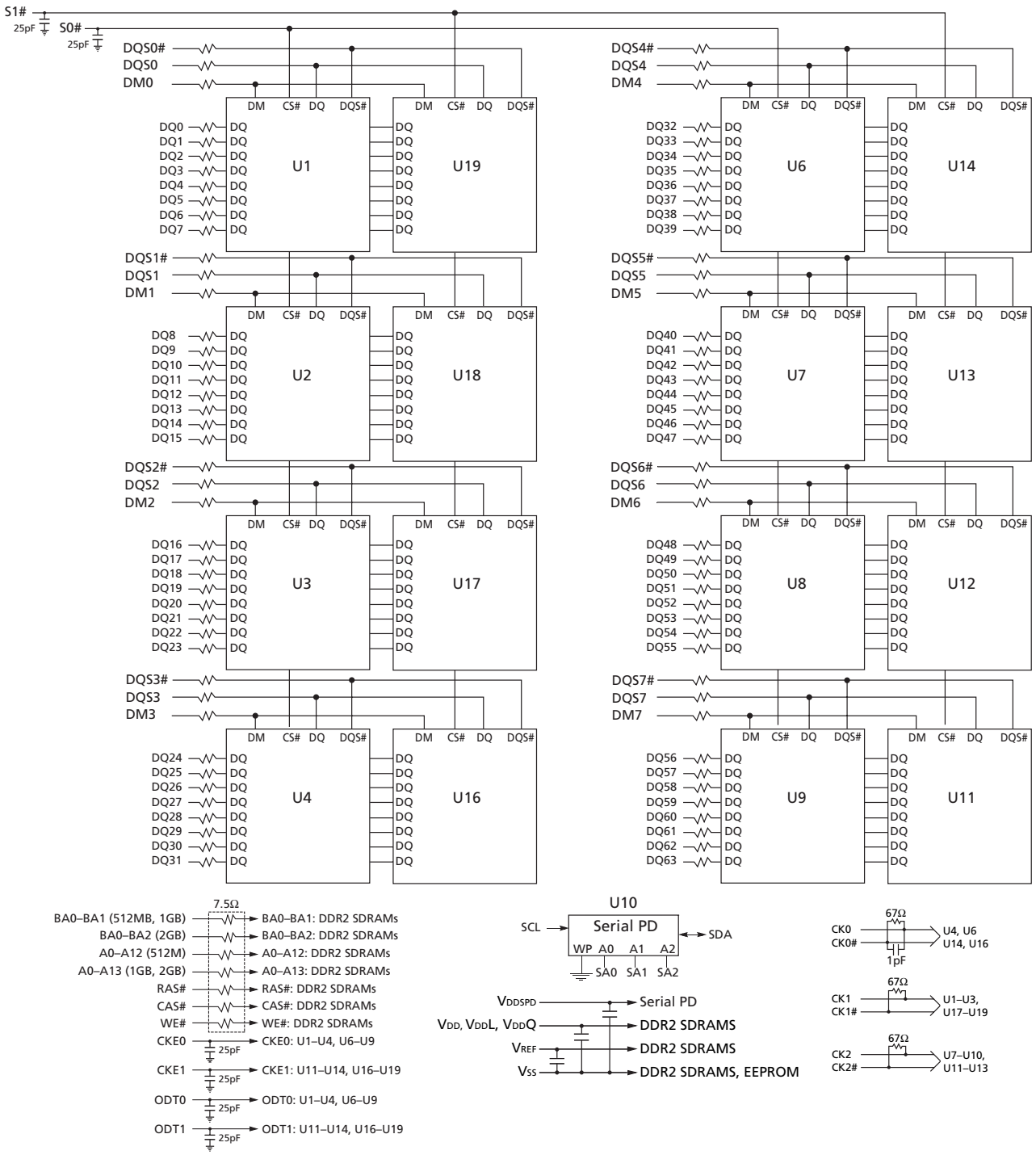
Pin Numbers	Symbol	Type	Description
120	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
101, 239, 240	SA0–SA2	Input	Presence-detect address inputs: These pins are used to configure the presence-detect device.
3, 4, 9, 10, 12, 13, 21, 22, 24, 25, 30, 31, 33, 34, 39, 40, 80, 81, 86, 87, 89, 90, 95, 96, 98, 99, 107, 108, 110, 111, 116, 117, 122, 123, 128, 129, 131, 132, 140, 141, 143, 144, 149, 150, 152, 153, 158, 159, 199, 200, 205, 206, 208, 209, 214, 215, 217, 218, 226, 227, 229, 230, 235, 236	DQ0–DQ63	I/O	Data Input/output: Bidirectional data bus.
6, 7, 15, 16, 27, 28, 36, 37, 83, 84, 92, 93, 104, 105, 113, 114,	DQS0–DQS7, DQS0#–DQS7#	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
119	SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197,	V_{DD}	Supply	Power supply: +1.8V ±0.1V.
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194,	$V_{DD}Q$	Supply	DQ Power supply: +1.8V ±0.1V.
1	V_{REF}	Supply	SSTL_18 reference voltage.
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97,100, 103, 106, 109,112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	Supply	Ground.
238	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
18, 19, 42, 43, 45, 46, 48, 49, 54 (512MB, 1GB), 55, 68, 76, 102, 125, 126, 134, 135, 146, 147, 155, 156, 161, 162, 164, 165, 167, 168, 171, 173, 174, 196 (512MB), 202, 203, 211, 212, 223, 224, 232, 233	NC	–	No connect: These pins should be left unconnected.

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Functional Block Diagram

Unless otherwise noted, resistor values are 22Ω. Micron module part numbers are explained in the module part numbering guide at www.micron.com/numbering.html. Modules use the following DDR2 SDRAM devices: MT47H32M8BT (512MB); MT47H64M8BT (1GB); and MT47H128M8BT (2GB).

Figure 3: Functional Block Diagram



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General Description

The MT16HTF6464A, MT16HTF12864A, and MT16HTF25664A DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 512MB, 1GB, and 2GB memory modules organized in x64 configuration. DDR2 modules use internally configured 4-bank (512MB, 1GB) or 8-bank (2GB) DDR2 devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DDR2 device core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DDR2 organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

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Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
VDD supply voltage relative to VSS		VDD	–1.0	2.3	V
VDDQ supply voltage relative to VSS		VDDQ	–0.5	2.3	V
VDDL supply voltage relative to VSS		VDDL[2]	–0.5	2.3	V
Voltage on any pin relative to VSS		VIN, VOUT	–0.5	2.3	V
Storage temperature		T_{STG}	–55	100	°C
DDR2 SDRAM device operating temperature (ambient)		T_{case}	0	85	°C
Operating temperature (ambient)		T_{OPR}	0	55	°C
Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤0.95V; (All other pins not under test = 0V)	Command/address, RAS#, CAS#, WE#	I_I	–80	80	µA
	S#, CKE[1]		–40	40	
	CK0, CK0#		–20	20	
	CK1, CK1#, CK2, CK2#		–30	30	
	DM		–10	10	
Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQ and ODT are disabled	DQ, DQS, DQS#	I_{OZ}	–10	10	µA
VREF leakage current; VREF = valid VREF level		–	–32	32	µA

Notes:
1. S# is defined to be S0# and S1#. CKE includes both CKE0 and CKE1.
2. VDDL is the power supply for the DDR2 devices' DLL; however, this power supply is not brought directy to a DIMM pin.

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

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Table 7: DDR2 IDD Specifications and Conditions – 512MB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one device bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	680	680	640	mA
Operating one device bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	760	760	720	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	80	80	80	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	560	560	400	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	640	560	480	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	480	400	320	mA
	Slow PDN exit MR[12] = 1		96	96	96	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	800	640	480	mA
Operating burst write current; All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	1,560	1,320	1,040	mA
Operating burst read current; All device banks open; Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	1,480	1,240	960	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	2,880	2,720	2,640	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	80	80	80	mA
Operating device bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching; See IDD7 conditions in component data sheet for detail		IDD7[a]	2,040	1,960	1,880	mA

Notes:
1. a = Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW).
2. b = Value calculated reflects all module ranks in this operating condition.

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Table 8: DDR2 IDD Specifications and Conditions – 1GB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-80E	-667	-53E	-40E	Units
Operating one device bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	856	776	696	696	mA
Operating one device bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	976	896	816	776	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	112	112	112	112	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	800	720	640	560	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	880	800	720	640	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	640	560	480	400	mA
	Slow PDN exit MR[12] = 1		192	192	192	192	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	1,120	1,040	880	720	mA
Operating burst write current; All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	1,616	1,416	1,1176	976	mA
Operating burst read current; All device banks open; Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	1,696	1,496	1,216	976	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	3,680	2,880	2,720	2,640	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	112	112	112	112	mA
Operating device bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching; See IDD7 conditions in component data sheet for detail		IDD7[a]	2,456	1,976	1,856	1,816	mA

Notes:
1. a = Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW).
2. b = Value calculated reflects all module ranks in this operating condition.

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Table 9: DDR2 IDD Specifications and Conditions – 2GB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-80E	-667	-53E	-40E	Units
Operating one device bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	856	776	696	616	mA
Operating one device bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	936	856	816	696	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	112	112	112	112	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	1,040	880	656	560	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	1,120	960	720	640	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	720	640	480	400	mA
	Slow PDN exit MR[12] = 1		160	160	160	160	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	1,200	1,120	880	720	mA
Operating burst write current; All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	1,536	1,336	1,096	936	mA
Operating burst read current; All device banks open; Ccontinuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	1,576	1,336	1,216	936	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	4,480	4,160	4,000	3,520	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	112	112	112	112	mA
Operating device bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching; See IDD7 conditions in component data sheet for detail		IDD7[a]	2,736	2,456	2,376	2,136	mA

Notes:
1. a = Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW).
2. b = Value calculated reflects all module ranks in this operating condition.

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AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site: www.micron.com/ddr2. Module speed grades correlate with component speed grades as shown in the following table:

Table 10: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-80E	-25E
-667	-3
-53E	-37E
-40E	-5E

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Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 4 and 5 on page 14).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting 8 bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the 8 bits of data (Figure 6 on page 14).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent 8-bit word. In the read mode the SPD device will transmit 8 bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

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Figure 4: Data Validity

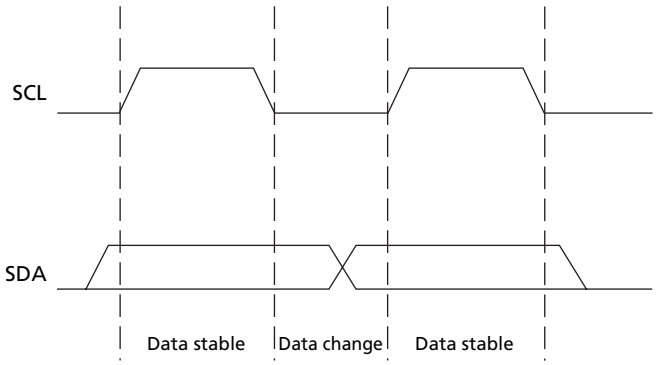


Figure 5: Definition of Start and Stop

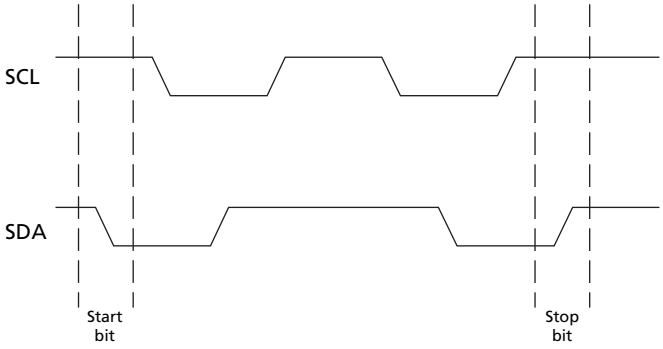
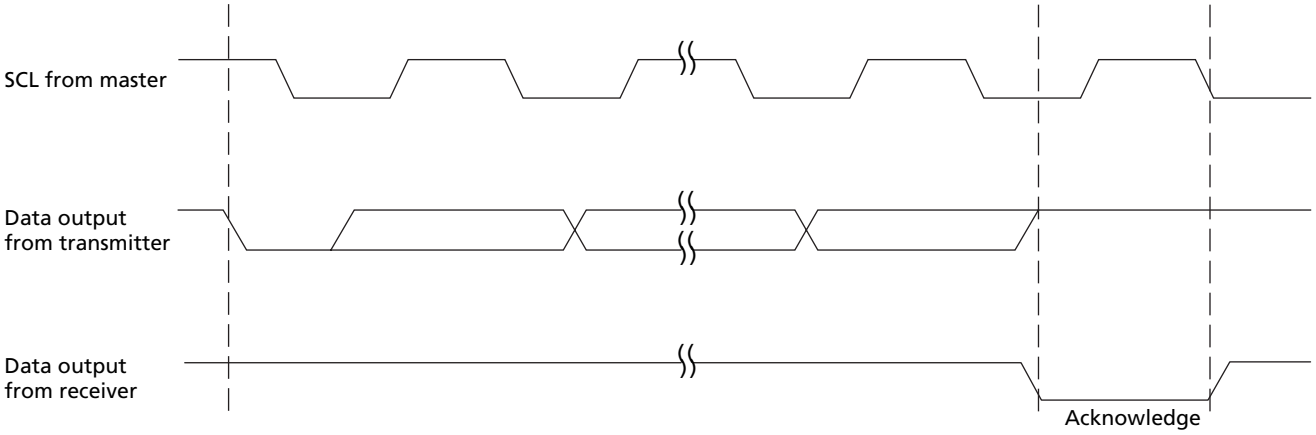


Figure 6: Acknowledge Response From Receiver



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Table 11: EEPROM Device Select Code

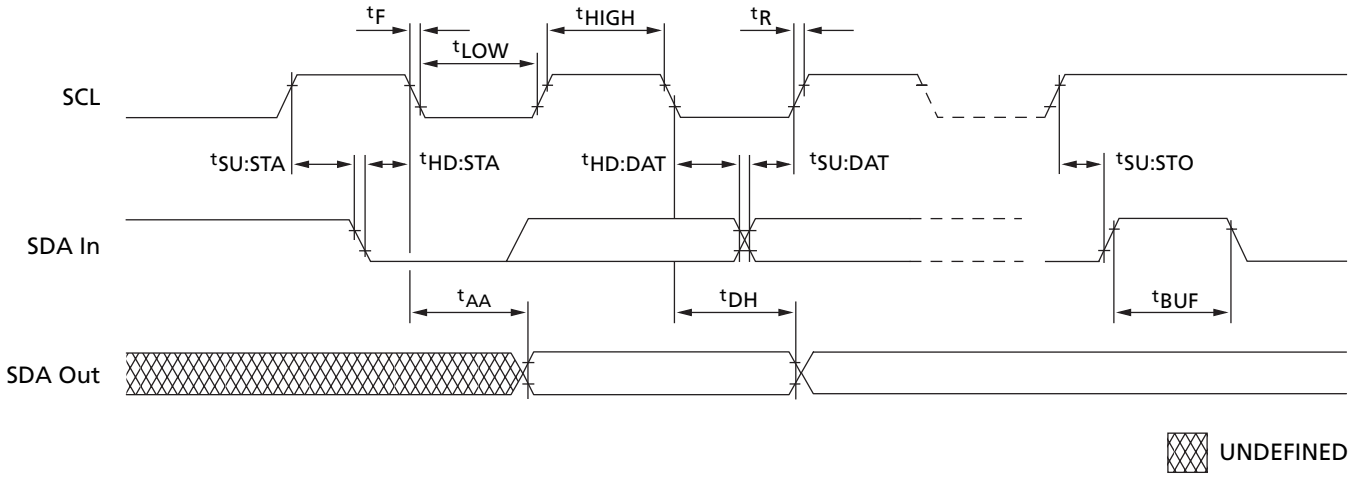
The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW

Table 12: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address READ	1	VIH or VIL	1	Start, device select, RW = 1
Random address READ	0	VIH or VIL	1	Start, device select, RW = 0, address
	1	VIH or VIL	1	Restart, device select, RW = 1
Sequential READ	1	VIH or VIL	≥ 1	Similar to current or random address READ
Byte WRITE	0	VIL	1	Start, device select, RW = 0
Page WRITE	0	VIL	≤ 16	Start, device select, RW = 0

Figure 7: SPD EEPROM Timing Diagram



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Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current:	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^tSCL	–	400	KHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

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Table 15: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 19

Byte	Description	Entry (Version)	MT16HTF6464A	MT16HTF12864A	MT16HTF25664A
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on assembly	13, 14	0D	0E	0E
4	Number of column addresses on assembly	10	0A	0A	0A
5	DIMM height and module ranks	1.18in, dual rank	61	61	61
6	Module data width	64	40	40	40
7	Reserved	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	DDR2 cycle time, ^{t}CK (CL = MAX value, see byte 18)	-80E -667 -53E -40E	– 30 3D 50	25 30 3D 50	25 30 3D 50
10	DDR2 access from clock,^{t}AC (CL = MAX value, see byte 18)	-80E -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
11	Module configuration type		00	00	00
12	Refresh rate/type	7.81µs/self	82	82	82
13	DDR2 SDRAM device width (primary device)	8	08	08	08
14	Error-checking DDR2 data width	N/A	00	00	00
15	Reserved	1 clock	00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on DDR2 device	4 or 8	04	04	08
18	CAS latencies supported	-80E (6, 5, 4) -667 (5, 4, 3) -53E/-40E (4, 3)	– 38 18	30 38 18	30 38 18
19	Module thickness		01	01	01
20	DDR2 DIMM type	Unbuffered	02	02	02
21	DDR2 module attributes		00	00	00
22	DDR2 device attributes: weak driver (01) or 50Ω ODT (03)	-80E/-667 -53E/-40E	03 01	03 01	03 01
23	DDR2 cycle time, ^{t}CK, MAX CL - 1	-80E/-667 -53E -40E	3D 50 50	3D 50 50	3D 50 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-80E -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-80E -667 -53E/-40E(N/A)	– 50 00	00 50 00	00 50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-80E -667 -53E/-40E(N/A)	– 45 00	00 45 00	00 45 00
27	MIN row precharge time, ^{t}RP	-80E -667/-53E/-40E	– 3C	32 3C	32 3C

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Table 15: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 19

Byte	Description	Entry (Version)	MT16HTF6464A	MT16HTF12864A	MT16HTF25664A
28	MIN row active to row active, ^{t}RRD		1E	1E	1E
29	MIN RAS#-to-CAS# delay, ^{t}RCD	-80E -667/-53E/-40E	– 3C	32 3C	32 3C
30	MIN RAS# pulse width, ^{t}RAS	-80E/-667/-53E -40E	2D 28	2D 28	2D 28
31	Module rank density	256MB, 512MB, 1GB	40	80	01
32	Address and command setup time, $^{t}IS_{b}$	-80E -667 -53E -40E	– 20 25 35	17 20 25 35	17 20 25 35
33	Address and command hold time, $^{t}IH_{b}$	-80E -667 -53E -40E	– 27 37 47	25 27 37 47	25 27 37 47
34	Data/data mask input setup time, $^{t}DS_{b}$	-80E -667/-53E -40E	– 10 15	05 10 15	05 10 15
35	Data/data mask input hold time, $^{t}DH_{b}$	-80E -667 -53E -40E	– 17 22 27	12 17 22 27	12 17 22 27
36	Write recovery time, ^{t}WR		3C	3C	3C
37	WRITE-to-READ command delay, ^{t}WTR	-80E/-667/-53E -40E	1E 28	1E 28	1E 28
38	READ-to-PRECHARGE command delay, ^{t}RTP		1E	1E	1E
39	Mem analysis probe		00	00	00
40	Extension for bytes 41 and 42	-80E -667/-53E/-40E	– 00	30 00	36 06
41	MIN active auto refresh time, ^{t}RC	-80E -667/-53E -40E	– 3C 37	39 3C 37	39 3C 37
42	MIN AUTO REFRESH-to-ACTIVE/ AUTO REFRESH command period, ^{t}RFC		69	69	7F
43	DDR2 device MAX cycle time, ^{t}CKMAX		80	80	80
44	DDR2 device MAX DQS-DQ skew time, ^{t}DQSQ	-80E -667 -53E -40E	– 18 1E 23	14 18 1E 23	14 18 1E 23
45	DDR2 device MAX read data hold skew factor, ^{t}QHS	-80E -667 -53E -40E	– 22 28 2D	1E 22 28 2D	1E 22 28 2D
46	PLL relock time		00	00	00
47–61	Optional features, not supported		00	00	00
62	SPD revision	Release 1.2	12	12	12
63	Checksum for bytes 0–62	-80E -667 -53E -40E	– ED 98 FF	90 4C F7 5E	31 ED 98 FF

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Table 15: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 19

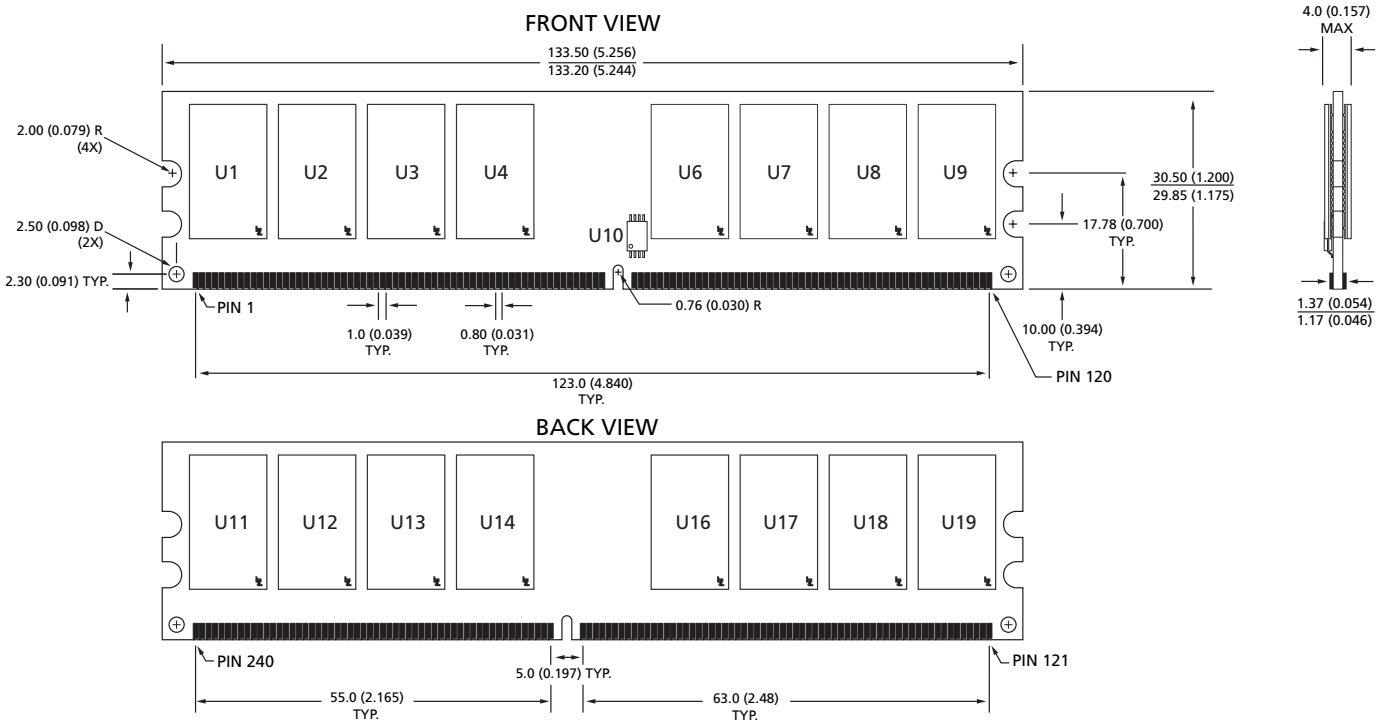
Byte	Description	Entry (Version)	MT16HTF6464A	MT16HTF12864A	MT16HTF25664A
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID code	(Continued)	FF	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C	01–0C
73-90	Module part number (ASCII)		Variable data	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable data	Variable data	Variable data
94	Week of manufacture in BCD		Variable data	Variable data	Variable data
95-98	Module serial number		Variable data	Variable data	Variable data
99-127	Manufacturer-specific data (RSVD)		–	–	–

Notes: 1. The ^{t}RAS SPD value shown is based on the JEDEC standard value of 45ns; the actual device specification is ^{t}RAS = 40ns.

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Module Dimensions

Figure 8: 240-pin DIMM DDR2 Module Dimensions



Notes:
1. All dimensions are in millimeters (inches); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. D, Released (No Mark) **4/06**
- Added -80E speed grade to 1GB and 2GB densities
- Removed component data
- Updated format, style

Rev. C, Released (No Mark) **5/05**
- Corrected 1GB -53E SPD

Rev. C, Released (No Mark) **3/05**
- Added -667 speed grade
- Updated Initialization process
- Updated Idds

Rev. B, Released (No Mark) (MT16HTF6464A), Preliminary (MT16HTF12864A, MT16HTF25664A) **8/04**
- Updated features list
- Updated part numbers
- Removed OCD, updated General Description
- Updated Initialization diagram, EMR diagrams
- Updated Table 15, AC Operating Conditions
- Updated SPD

Rev. A, Pub. 11/03, Preliminary (MT16HTF6464A), Advance (MT16HTF12864A and MT16HTF25664A) **11/03**
- New Datasheet, lvg'd from HTF8C32_64_128x72AG

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