Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues

SINGLE-SUPPLY OP AMP ISSUES

Single-supply operation has become an increasingly important requirement because of market demands. Automotive, set-top box, camera/camcorder, PC, and laptop computer applications are demanding IC vendors to supply an array of linear devices that operate on a single-supply rail, with the same performance of dual supply parts. Power consumption is now a key parameter for line or battery operated systems, and in some instances, more important than cost. This makes low-voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of "doing more with less" in their amplifier designs.

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1 mV are less than a 0.04 LSB error source in a 12-bit, 10 V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1 mV represents a 0.8 LSB error in a 5 V fullscale system (or 1.6 LSB for 2.5 V fullscale).

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers with ~120 dB open-loop gains typically operate on dual supplies—for example OP07 types. However, many single-supply/rail-to-rail amplifiers for precision applications typically have open-loop gains between 25,000 and 30,000 under light loading (>10 kΩ). Selected devices, like the OP113/OP213/OP413 family, do have high open-loop gains (>120 dB), for use in demanding applications. Another example would be the AD855x chopper-stabilized op amp series.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers now become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. Amplifier voltage noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low-power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0 V) is very convenient, as there is equal supply headroom in each direction, and 0 V is generally the voltage on the low impedance ground plane. In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as

the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0 V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0 V input.

The need for rail-to-rail amplifier output stages is also driven by the need to maintain wide dynamic range in low-supply voltage applications. A single-supply/rail-to-rail amplifier should have output voltage swings that are within at least 100 mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current. Single-supply op amp design issues are summarized in Figure 1.

- **Single Supply Offers:**
  - **Lower Power**
  - **Battery Operated Portable Equipment**
  - **Requires Only One Voltage**

- **Design Tradeoffs:**
  - **Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.**
  - **Must Usually Share Noisy Digital Supply**
  - **Rail-to-Rail Input and Output Needed to Increase Signal Swing**
  - **Precision Less than the best Dual Supply Op Amps but not Required for All Applications**
  - **Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs**

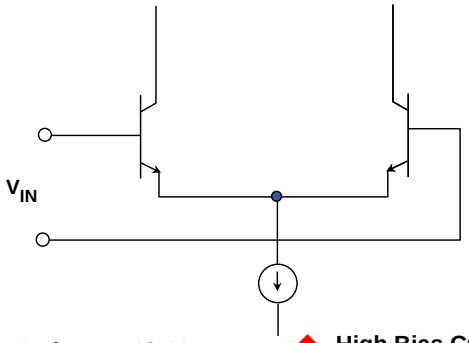
Figure 1: Single-Supply Op Amp Design Issues

OP AMP INPUT STAGES

It is extremely important to understand input and output structures of op amps in order to properly design the required interfaces. For ease of discussion, the two can be examined separately, as there is no particular reason to relate them at this point.

Bipolar Input Stages

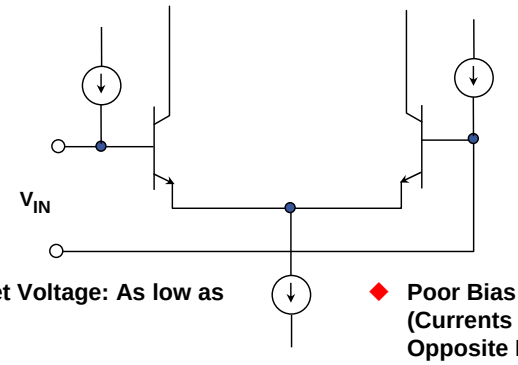
The very common and basic bipolar input stage of Figure 2 consists of a "long-tailed pair" built with bipolar transistors. It has a number of advantages: it is simple, has very low offset, the bias currents in the inverting and non-inverting inputs are well-matched and do not vary greatly with temperature. In addition, minimizing the initial offset voltage of a bipolar op amp by laser trimming also minimizes its drift over temperature. This architecture was used in the very earliest monolithic op amps such as the µA709. It is also used with modern high speed types. Although NPN bipolars are shown, the concept also applies with the use of PNP bipolars.



- Low Offset: As low as 10µV
- Low Offset Drift: As low as 0.1µV/°C
- Temperature Stable I_B
- Well-Matched Bias Currents
- Low Voltage Noise: As low as 1nV/√Hz
- High Bias Currents: 50nA - 10µA
- (Except Super-Beta: 50pA - 5nA, More Complex and Slower)
- Medium Current Noise: 1pA/√Hz
- Matching source impedances minimize offset error due to bias current

Figure 2: A Bipolar Transistor Input Stage

Bias Current Compensated Bipolar Input Stage



- Low Offset Voltage: As low as 10µV
- Low Offset Drift: As low as 0.1µV/°C
- Temperature Stable I_{bias}
- Low Bias Currents: <0.5 - 10nA
- Low Voltage Noise: As low as 1nV/√Hz
- Poor Bias Current Match (Currents May Even Flow in Opposite Directions)
- Higher Current Noise
- Not Very Useful at HF
- Matching source impedances makes offset error due to bias current worse because of additional impedance

Figure 3: A Bias Current Compensated Bipolar Input Stage

A simple bipolar input stage such as used in Figure 2 exhibits high bias current because the currents seen externally are in fact the base currents of the two input transistors. By providing this necessary bias currents via an internal current source, as in Figure 3, the only *external*

current then flowing in the input terminals is the difference current between the base current and the current source, which can be quite small.

Most modern precision op amps use some means of internal bias current compensation, examples would be the familiar OP07 and OP27 series.

Bias current compensated input stages have many of the good features of the simple bipolar input stage, namely: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor.

These latter two undesired side effects result from the external bias current being the *difference* between the compensating current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add in a root-sum-of-squares fashion (even though the dc currents subtract). Since the resulting external bias current is the difference between two nearly equal currents, there is no reason why the net current should have a defined polarity. As a result, the bias currents of a bias-compensated op amp may not only be mismatched, they can actually flow in opposite directions.

In many cases, the bias current compensation feature is not mentioned on an op amp data sheet, and a simplified schematic isn't supplied. It is easy to determine if bias current compensation is used by examining the bias current specification. If the bias current is specified as a "±" value, the op amp is most likely compensated for bias current.

Note that this can easily be verified, by examining the *offset current* specification (the difference in the bias currents). If internal bias current compensation exists, the offset current will be of the same magnitude as the bias current. Without bias current compensation, the offset current will generally be at least a factor of 10 smaller than the bias current. Note that these relationships generally hold, regardless of the exact magnitude of the bias currents.

The effects of bias current on the output offset voltage of an op amp can often be cancelled by making the source resistances at the two inputs equal. But, there is an important caveat here. The validity of this practice only holds true for bipolar input op amps *without* bias current compensation, that is, where the input currents are well matched. In a case of an op amp using internal bias current compensation, adding an extra resistance to either input will usually make the output offset worse!

FET Input Stages

Field-Effect Transistors (FETs) have much higher input impedance than do bipolar junction transistors (BJTs) and would therefore seem to be ideal devices for op amp input stages. However, they cannot be manufactured on all bipolar IC processes, and when a process does allow their manufacture, they often have their own problems.

FETs have high input impedance, low bias current, and good high frequency performance (in an op amp, the lower g_m of the FET devices allows higher tail currents, thereby increasing the maximum slew rate). FETs also have much lower current noise.

On the other hand, the input offset voltage of FET long-tailed pairs, however, is not as good as the offset of corresponding BJTs, and trimming for minimum offset does not simultaneously minimize drift. A separate trim is needed for drift, and as a result, offset and drift in a JFET op amp, while good, aren't as good as the best BJT ones.

It is possible to make JFET op amps with very low voltage noise, but the devices involved are very large and have quite high input capacitance, which varies with input voltage, and so a trade-off is involved between voltage noise and input capacitance.

The bias current of an FET op amp is the leakage current of the gate diffusion (or the leakage of the gate protection diode, which has similar characteristics for a MOSFET). Such leakage currents double with every 10°C increase in chip temperature so that a FET op amp bias current is *one thousand times greater* at 125°C than at 25°C. Obviously this can be important when choosing between a bipolar or FET input op amp, especially in high temperature applications where bipolar op amp input bias current actually decreases.

Thus far, we have spoken generally of all kinds of FETs, that is junction (JFETs) and MOS (MOSFETs). In practice, combined bipolar/JFET technology op amps (i.e., BiFET) achieve better performance than op amps using purely MOSFET or CMOS technology. While ADI and others make high performance op amps with MOS or CMOS input stages, in general these op amps have worse offset and drift, voltage noise, high-frequency performance than the precision bipolar counterparts. The power consumption is usually somewhat lower than that of bipolar op amps with comparable, or even better, performance.

JFET devices require more headroom than do BJTs, since their pinchoff voltage is typically greater than a BJTs base-emitter voltage. Consequently, they are more difficult to operate at very low power supply voltages (1-2 V). In this respect, CMOS has the advantage of requiring less headroom than JFETs.

Rail-Rail Input Stages

Today, there is common demand for op amps with input CM voltage that includes *both* supply rails, i.e., *rail-to-rail* CM operation. While such a feature is undoubtedly useful in some applications, engineers should recognize that there are still relatively few applications where it is absolutely essential. These applications should be distinguished from the many more applications where a CM range *close* to the supplies, or one that includes *one* supply is necessary, but true input rail-to-rail operation is not.

In many single-supply applications, it is required that the input CM voltage range extend to one of the supply rails (usually ground). High-side or low-side current-sensing applications are examples of this. Many amplifiers can handle 0 V CM inputs, and they are easily designed using PNP (or PMOS) differential pairs (or N-channel JFET pairs) as shown in Figure 4. The input CM

range of such an op amp generally extends from about 200 mV below the negative rail ($-V_S$ or ground), to about 1-2 V of the positive rail, $+V_S$.

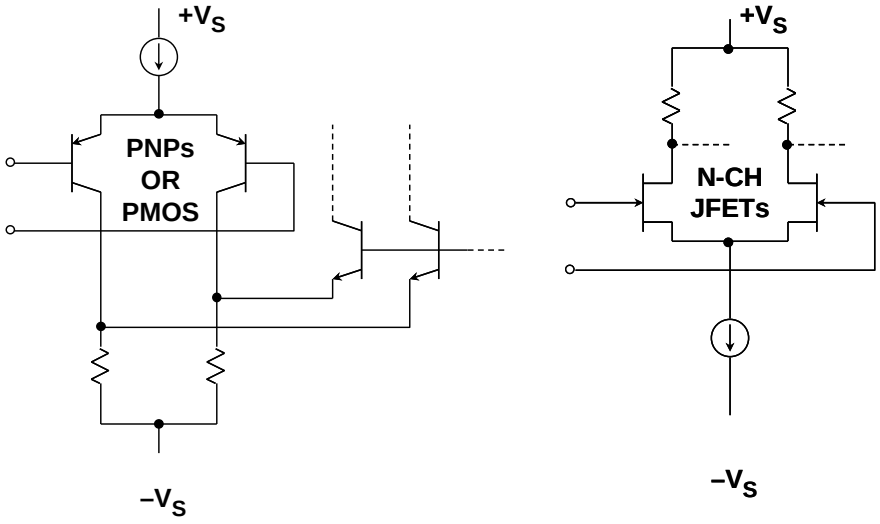


Figure 4: PNP/PMOS or N-Channel JFET Stages Allow CM Inputs to the Negative Rail

An input stage could also be designed with NPN (or NMOS) transistors (or P-channel JFETs), in which case the input CM range would include the positive rail, and go to within about 1-2 V of the negative rail. This requirement typically occurs in applications such as high-side current sensing. The OP282/OP482 input stage uses a P-channel JFET input pair whose input CM range includes the positive rail, making it suitable for high-side sensing.

A simplified diagram of a true rail-to-rail input stage is shown in Figure 6. Note that this requires use of *two* long-tailed pairs, one of PNP bipolar transistors Q1-Q2, the other of NPN transistors Q3-Q4. Similar input stages can also be made with CMOS pairs.

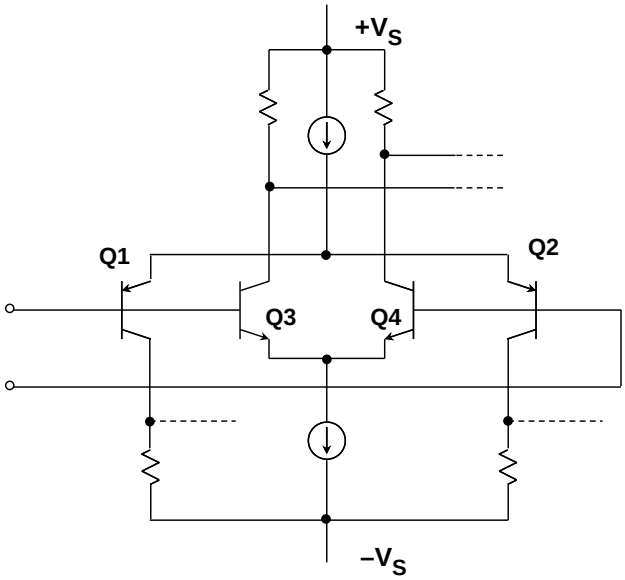


Figure 5: A True Rail-To-Rail Bipolar Transistor Input Stage

It should be noted that these two pairs will exhibit *different* offsets and bias currents, so when the applied CM voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout most of the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the two pairs. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. As noted, a true rail-to-rail input stage can also be constructed from CMOS transistors, for example as in the case of the CMOS AD8531/AD8532/AD8534 op amp family.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the CM input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-to-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices, and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair, somewhere along the input CM voltage range. Some devices like the OP191/OP291/OP491 family and the OP279 have a common-mode crossover threshold at approximately 1 V below the positive supply (where signals do not often occur). The PNP differential input stage is active from about 200 mV below the negative supply to within about 1 V of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly.

Also, as noted previously, amplifier bias currents are dominated by the PNP differential pair over most of the input common-mode range, and change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/OP284/OP484 family utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout most of the entire input CM voltage range. With this approach to biasing, there is no CM crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages, and offset voltage exhibits a smooth transition throughout the entire input CM range, due to careful laser trimming of input stage resistors.

In the same manner, through careful input stage current balancing and input transistor design, the OP184 family input bias currents also exhibit a smooth transition throughout the entire CM input voltage range. The exception occurs at the very extremes of the input range, where amplifier offset voltages and bias currents increase sharply, due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1 V of either supply rail.

When *both* differential pairs are active throughout most of the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of √2 for JFET input stages. This is due to the higher transconductance of two operating input stages.

Input stage g_m determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1 V of either supply rail, and the behavior is similar to that of the input bias currents.

In light of the many quirks of true rail-to-rail op amp input stages, applications which do require true rail-to-rail inputs should be carefully evaluated, and an amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.

OUTPUT STAGES

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 6A. Naturally, the slew rates were greater for positive-going than they were for negative-going signals.

While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on ac signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in an ability of the output to approach one supply more closely than the other in terms of saturation voltage.

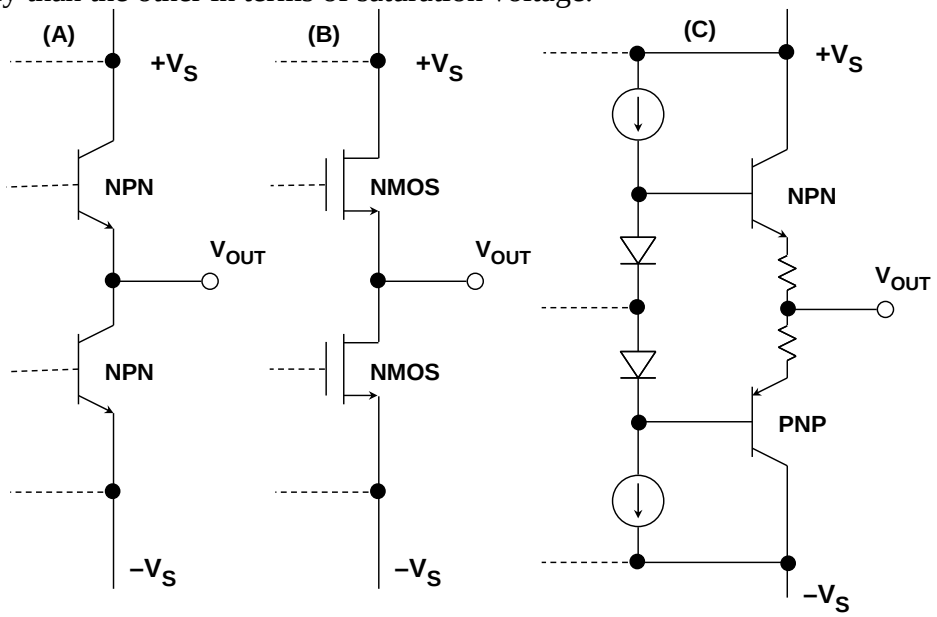


Figure 6: Some Traditional Op Amp Output Stages

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity, as shown in Figure 6B.

With modern complementary bipolar (CB) processes, well matched high speed PNP and NPN transistors are readily available. The complementary emitter follower output stage shown in Figure 6C has many advantages, but the most outstanding one is the low output impedance. However, the output voltage of this stage can only swing within about one V_{BE} drop of either rail. Therefore an output swing of +1 V to +4 V is typical of such a stage, when operated on a single +5 V supply.

The complementary common-emitter/common-source output stages shown in Figure 7A and B allow the op amp output voltage to swing much closer to the rails, but these stages have much higher open-loop output impedance than do the emitter follower-based stages of Figure 6C. In practice, however, the amplifier's high open-loop gain and the applied feedback can still produce an application with low output impedance (particularly at frequencies below 10 Hz). What should be carefully evaluated with this type of output stage is the loop gain within the application, with the load in place. Typically, the op amp will be specified for a minimum gain with a load resistance of 10 kΩ (or more). Care should be taken that the application loading doesn't drop lower than the rated load, or gain accuracy may be lost.

It should also be noted these output stages can cause the op amp to be more sensitive to capacitive loading than the emitter-follower type. Again, this will be noted on the device data sheet, which will indicate a maximum of capacitive loading before overshoot or instability will be noted.

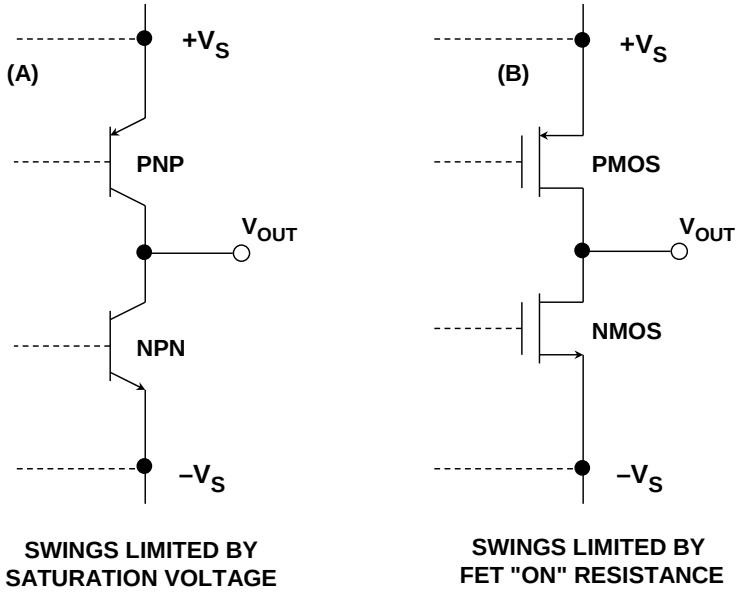


Figure 7: "Almost" Rail-To-Rail Output Structures

The complementary common emitter output stage using BJTs (Figure 7A) cannot swing completely to the rails, but only to within the transistor saturation voltage (V_{CESAT}) of the rails. For small amounts of load current (less than 100 µA), the saturation voltage may be as low as 5 to 10 mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500 mV at 50 mA).

On the other hand, an output stage constructed of CMOS FETs (Figure 7B) can provide nearly true rail-to-rail performance, but only under no-load conditions. If the op amp output must source or sink substantial current, the output voltage swing will be reduced by the I×R drop across the FETs internal "on" resistance. Typically this resistance will be on the order of 100 Ω for precision amplifiers, but it can be less than 10 Ω for high current drive CMOS amplifiers.

For the above basic reasons, it should be apparent that there is no such thing as a *true* rail-to-rail output stage, hence the caption of Figure 7 ("Almost" Rail-to-Rail Output Structures). The best any op amp output stage can do is an almost rail-to-rail swing, when it is lightly loaded.

CIRCUIT DESIGN CONSIDERATIONS FOR SINGLE SUPPLY SYSTEMS

Many waveforms are bipolar in nature. This means that the signal naturally swings around the reference level, which is typically ground. This obviously won't work in a single supply environment. What is required is to ac couple the signals.

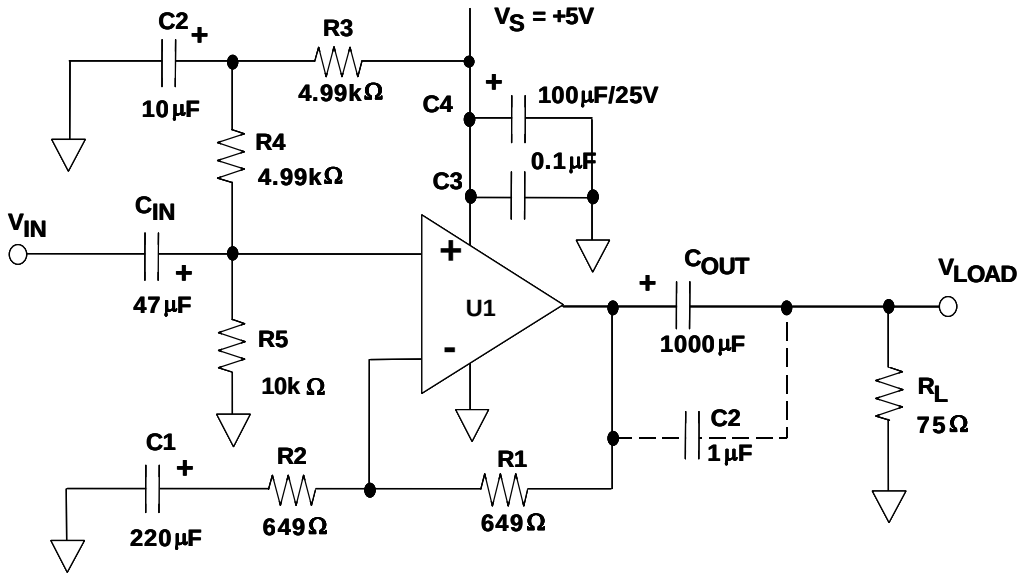


Figure 8: Single Supply Biasing

AC coupling is simply applying a high pass filter and establishing a new reference level typically somewhere around the center of the supply voltage range as shown in Figure 8. The series capacitor will block the dc component of the input signal. The corner frequency (the frequency at which the response is 3 dB down from the midband level) is determined by the value of the components:

$$f_C = \frac{1}{2\pi R_{EQ} C}, \qquad \text{Eq. 1}$$

where:

$$R_{EQ} = \frac{R4R5}{R4 + R5}. \qquad \text{Eq. 2}$$

It should be noted that if multiple sections are ac coupled, each section will be 3 dB down at the corner frequency. So if there are two sections with the same corner frequency, the total response will be 6 dB down, three sections would be 9 dB down etc. This should be taken into account so that the overall response of the system will be adequate. Also keep in mind that the amplitude response starts to roll off a decade, or more, from the corner frequency.

The ac coupling of arbitrary waveforms can actually introduce problems which don't exist at all in dc coupled systems. These problems have to do with the waveform duty cycle, and are particularly acute with signals which approach the rails, as they can in low supply voltage systems which are ac coupled.

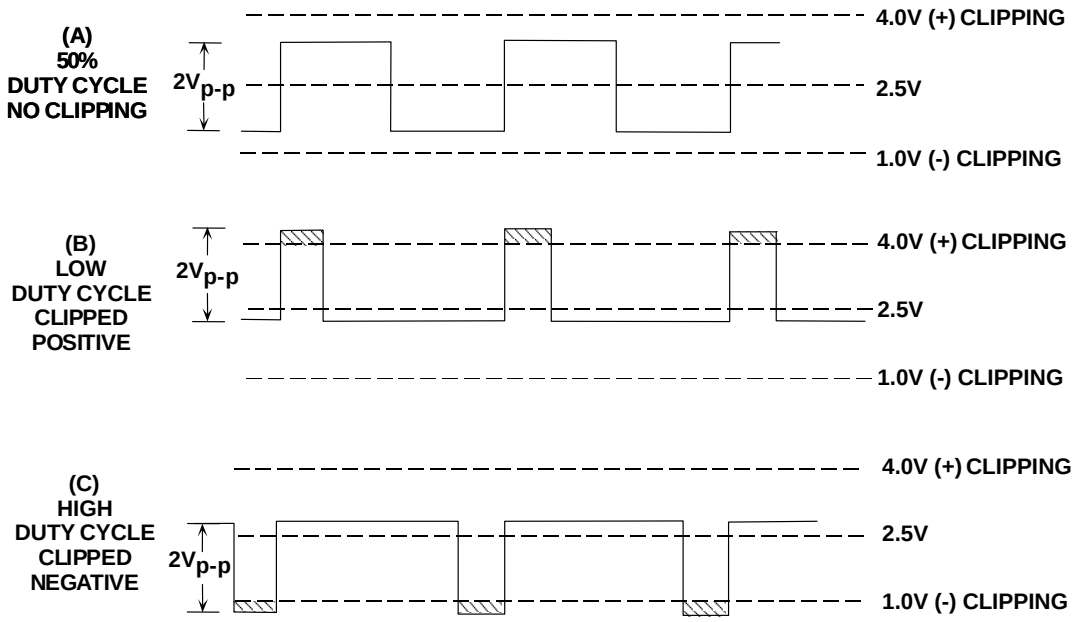


Figure 9: Headroom Issues with Single Supply Biasing

In an amplifier circuit such as that of Figure 8, the output bias point will be equal to the dc bias as applied to the op amp's (+) input. For a symmetric (50% duty cycle) waveform of a 2 Vp-p output level, the output signal will swing symmetrically about the bias point, or nominally 2.5 V ±1 V (using the values given in Figure 9). If however the pulsed waveform is of a very high (or low) duty cycle, the ac averaging effect of C_{IN} and R4||R5 will shift the effective peak level

either high or low, dependent upon the duty cycle. This phenomenon has the net effect of reducing the working headroom of the amplifier, and is illustrated in Figure 9.

In Figure 9 (A), an example of a 50% duty cycle square wave of about 2 Vp-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5 V supply amplifier. This amplifier, for example, (an AD817 biased similarly to Figure 8) can only swing to the limited dc levels as marked, about 1 V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

REFERENCES:

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 1.

2. Walter G. Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Also available as *Op Amp Applications Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 1.

Copyright 2009, Analog Devices, Inc. All rights reserved. Analog Devices assumes no responsibility for customer product design or the use or application of customers' products or for any infringements of patents or rights of others which may result from Analog Devices assistance. All trademarks and logos are property of their respective holders. Information furnished by Analog Devices applications and development tools engineers is believed to be accurate and reliable, however no responsibility is assumed by Analog Devices regarding technical accuracy and topicality of the content provided in Analog Devices Tutorials.