MSTM-S3-T2F1
Stratum 3
Timing Module

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Application

The Connor-Winfield MSTM-S3-T2F1 Simplified Control Timing Module acts as a complete system clock module for Stratum 3 timing applications in accordance with GR-1244, Issue 2 and GR-253, Issue 3.

Connor Winfield's Stratum 3 timing modules helps reduce the cost of your design by minimizing your development time and maximizing your control of the system clock with our simplified design.

Features

- 5V Miniature Timing Module
- Redundant 19.44 MHz References
- 40 sec., Filtered, Hold Over History
- Operational Status Flags

Bulletin	**TM030**
Page	**1 of 16**
Revision	**Advance A00**
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General Description

The Connor-Winfield Stratum 3 Miniature Simplified Control Timing Module acts as a complete system clock module for general Stratum 3 timing applications. The MSTM is designed for external control functions. Full external control input allows for selections and monitoring of any of four possible operating states: 1) Holdover, 2) External Reference #1, 3) External Reference #2, and 4) Free Run. The Table 5 (pg. 4) illustrates the control signal inputs and corresponding operational states:

In the absence of External Control Inputs (A,B), the MSTM enters the Free Run mode and signals an External Alarm. The MSTM will enter other operating modes upon application of a proper control signal. Mode 1 operation (A=1, B=0) results in an output signal that is phase locked to the External Reference Input #1. Mode 2 operation (A=0, B=1) results in an output signal that is phase locked to External Reference Input #2. Holdover mode operation (A=1, B=1) results in an output signal at or near the frequency as determined by the latest (last) locked-signal input values and the holdover performance of the MSTM.

The primary feature of this model is the Reference Frequency Detector (RFD). This is an independent circuit that monitors both reference inputs simultaneously to determine that a signal is present and its frequency is within a valid range. A logical one on the outputs VALID_R1 and VALID_R2 indicates that the signals applied to EX_REF1 and EX_REF2 respectively have been detected and have a frequency that is within at least +/- 4.6 ppm of nominal. A range of +/-4.6 ppm is guaranteed for the life of the module. The actual range is somewhat more than twice that to account for normal drift and aging that will occur. When, for example, the reference applied to EX_REF1 disappears, VALID_R1 will go to a logical zero within 500 microseconds. When the signal returns at a frequency within +/- 4.6 ppm of nominal the VALID_R1 output will return to a logical one after a 4-second delay. The delay is a validation period that requires the output of the frequency detector to remain stable for 4 seconds before confirming the status of the reference applied. This eliminates the incessant toggling of the frequency detector that occurs when the reference frequency is at the threshold frequency of the detector

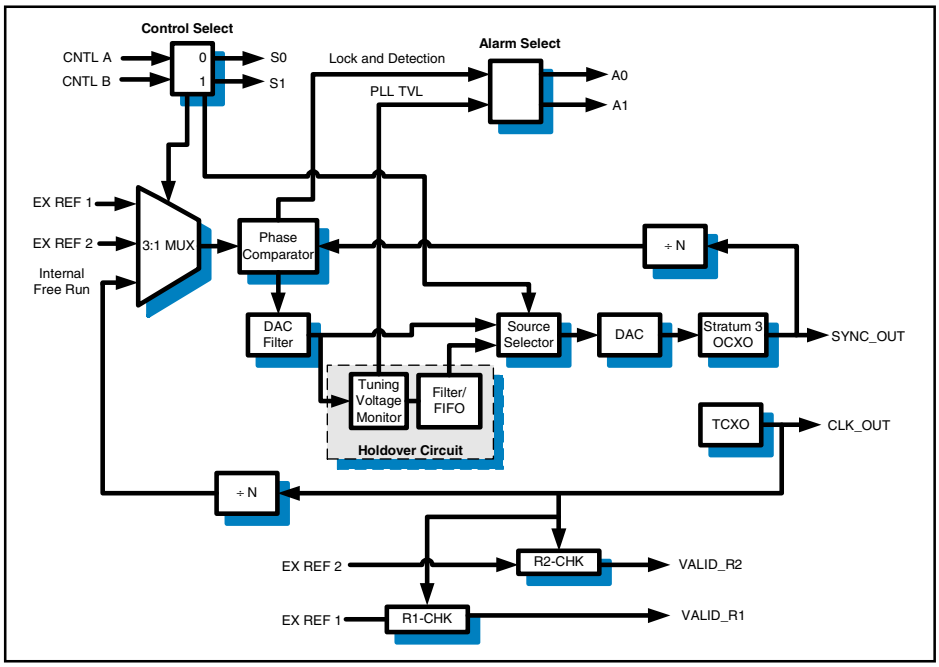
The function of the RFD is not related to the operational alarms, LOL and TVL, which monitor the operation of the PLL relative to the selected active reference. In fact the operational alarms function only at the extreme edge of the PLL operating range. This means that it is quite possible for the active reference to drift out of range of the Reference Frequency Detector and still remain well within the capture range of the PLL and not activate the operational alarms. If the other reference was still marked valid by the RFD it might make sense to switch to the better reference before the selected reference drifts completely out of range.

Alarm signals are generated at the Alarm Output during Holdover and Free Run operation. Alarm Signals are also generated by loss-of-lock, loss of Reference, and by a Tune-Limit indication from the PLL. A Tune-Limit alarm signal indicates that the OCXO tuning voltage is approaching within 10% the limits of its lock capability and that the External Reference Input may be erroneous. A high level indicates an alarm condition. Real-time indication of the operational mode is available from outputs S0 and S1, which are determined from internal mode registers.

Control loop filters effectively attenuate any reference jitter and smooth out phase transients.

Functional Block Diagram

Figure 1



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Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5		7.0	Volts	1.0
V_I	Input Voltage	-0.5		V_{CC} + 0.5	Volts	1.0
T_s	Storage Temperature	-55		100	deg. C	1.0

Recommended Operating Conditions

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power supply voltage	4.75	5.00	5.25	Volts	
V_{IH}	High level input voltage - TTL	2.0		V_{CC}	Volts	
V_{IL}	Low level input voltage - TTL	0		0.8	Volts	
t_{IN}	Input signal transition - TTL			250	ns	
C_{IN}	Input capacitance			15	pF	
V_{OH}	High level output voltage, I_{OH} = -4.0mA, V_{CC} = min.	2.4		5.25	Volts	2.0
V_{OL}	Low level output voltage, I_{OL} = 12.0 mA, V_{CC} = min.			0.4	Volts	
t_{TRANS}	Clock out transition time		4.0		ns	
t_{PULSE}	8kHz input reference pulse width(positive or negative)	30			ns	
T_{OP}	Operating temperature	0		70	°C	

Specifications

Table 3

Parameter	Specifications	Notes
Synchronized Output Frequency (SYNC_OUT)	19.44 MHz	
Non-synchronized Output Frequency (CLK_OUT)	19.44 MHz	
Input Reference Frequency	Dual 19.44 MHz references	
Supply Current	250 mA typical, 400 mA during warm-up (Maximum)	3.0
Jitter, Wander and Phase Transient Tolerances	GR-1244-CORE 4.2-4.4, GR-253-CORE 5.4.4.3.6	
Wander Generation	GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	
Wander Transfer	GR-1244-CORE 5.4	
Jitter Generation	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3	
Jitter Transfer	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1	
Phase Transients	GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3	
Free Run Accuracy	4.6 ppm over T_{OP}	
Hold Over Stability	±0.37 ppm for initial 24 hrs	4.0
Inital Offset	±0.05 ppm	
Temperature	±0.28 ppm	
Drift	±0.04 ppm	
Maximum Hold Over History	40 seconds	
Pull-in/ Hold-in Range	±4.6 ppm minimum	5.0
Lock Time	<100 sec.	
PLL_TVL Alarm Limit	Extreme 10% ranges of Pull-in/Hold-in Range	

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Pin Description

Table 4

Pin #	Connection	Description
1	S0	Condition state output bit 0
2	S1	Condition state output bit 1
3	VALID_R1	Reference #1 validation
4	VALID_R2	Reference #2 validation
5	GND	Ground
6	A0	Alarm bit 0
7	CNTL A	Mode control input
8	CNTL B	Mode control input
9	A1	Alarm bit 1
10	GND	Ground
11	SYNC_OUT	Primary timing output signal. Signal is sychronized to reference.
12	GND	Ground
13	CLK_OUT	Stratum 3 TCXO output (non-sychronized 19.44 MHz, ±4.6 output)
14	GND	Ground
15	EX_REF_2	External 19.44 MHz Input Reference #2
16	GND	Ground
17	EX_REF_1	External 19.44 MHz Input Reference #1
18	V_{CC}	+5V DC supply

Function Control Table

Table 5

Control Inputs		Operational Mode		Alarm Outputs		Condition State Output	
A	**B**			**A0**	**A1**	**S0**	**S1**
0	0	Free Run (Default Mode)		0	0	0	0
1	0	External Reference #1	Normal	0	0	1	0
			Tune Limit	1	0	1	0
			LOR	0	1	1	0
			LOL (>17 ppm)	1	1	1	0
0	1	External Reference #2	Normal	0	0	0	1
			Tune Limit	1	0	0	1
			LOR	0	1	0	1
			LOL (>17 ppm)	1	1	0	1
1	1	Hold Over		0	0	1	1

NOTES:

1.0: Stresses beyond those listed under Absolute Maximum Rating may cause damage to the device. Operation beyond Recommended Conditions is not implied.

2.0: Logic is 3.3V CMOS

3.0: GR-1244-CORE 3.2.1

4.0: Hold Over stability is the cumulative fractional frequency offset as described by GR-1244-CORE, 5.2

5.0: Pull-in Range is the maximum frequency deviation from nominal clock rate on the reference inputs to the timing module that can be overcome to pull into synchronization with the reference

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Qualification Outputs

Table 6

Condition	Valid_R1	Valid_R2
Ref 1 is within ±4.6 ppm	1	X
Ref 1 > ±4.6 ppm	0	X
Ref 1 (No Signal)	0	X
Ref 2 is within ±4.6 ppm	X	1
Ref 2 > ±4.6 ppm	X	0
Ref 2 (No Signal)	X	0

Valid Reference Thresholds

Table 7

	Minimum	Nominal	Maximum
VALID_R1	±4.6 ppm	±9.2 ppm	±13.8 ppm
VALID_R2	±4.6 ppm	±9.2 ppm	±13.8 ppm

Frequency Detector Range Over Lifetime

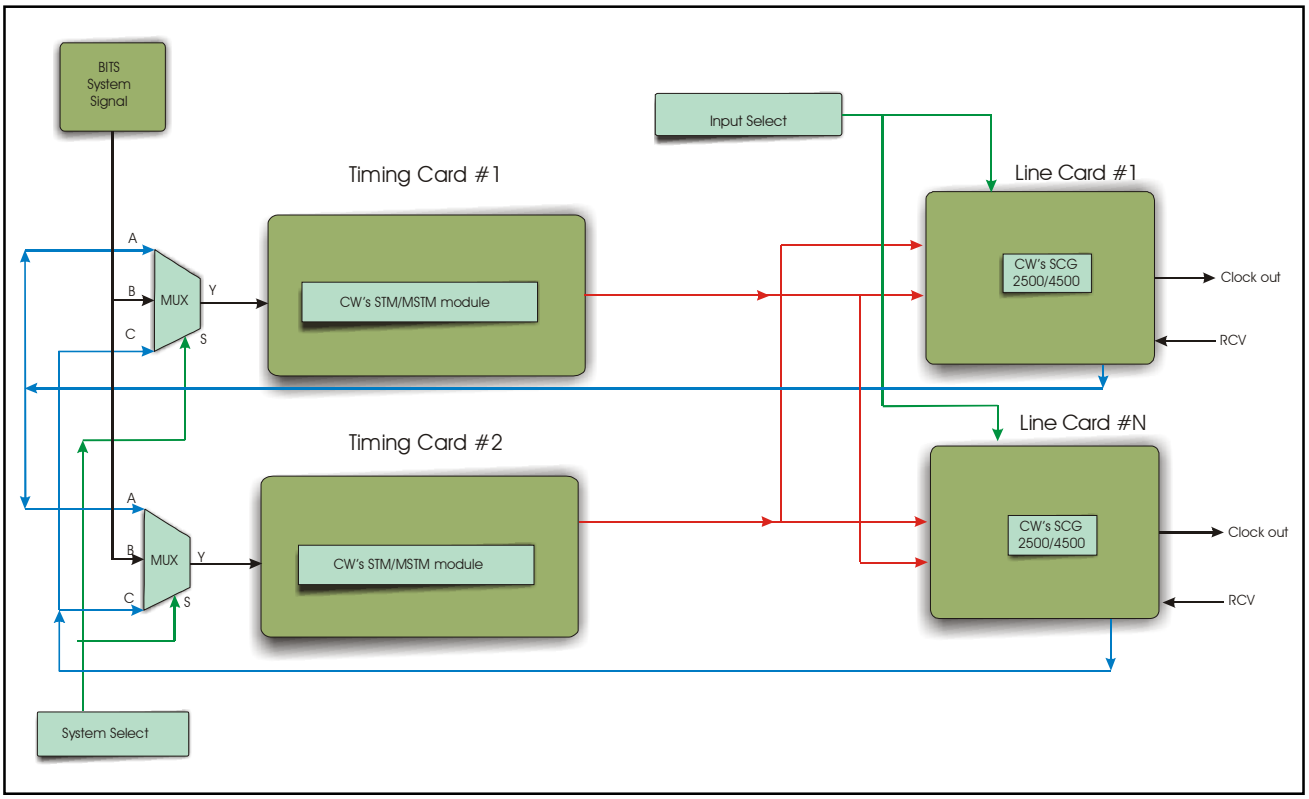
Table 8

Detector Frequency Offset	VALID_R1/R2 Range
0 ppm	±9.2 ppm
+4.6 ppm	+13.8 ppm -4.6 ppm
-4.6 ppm	+4.6 ppm -13.8 ppm

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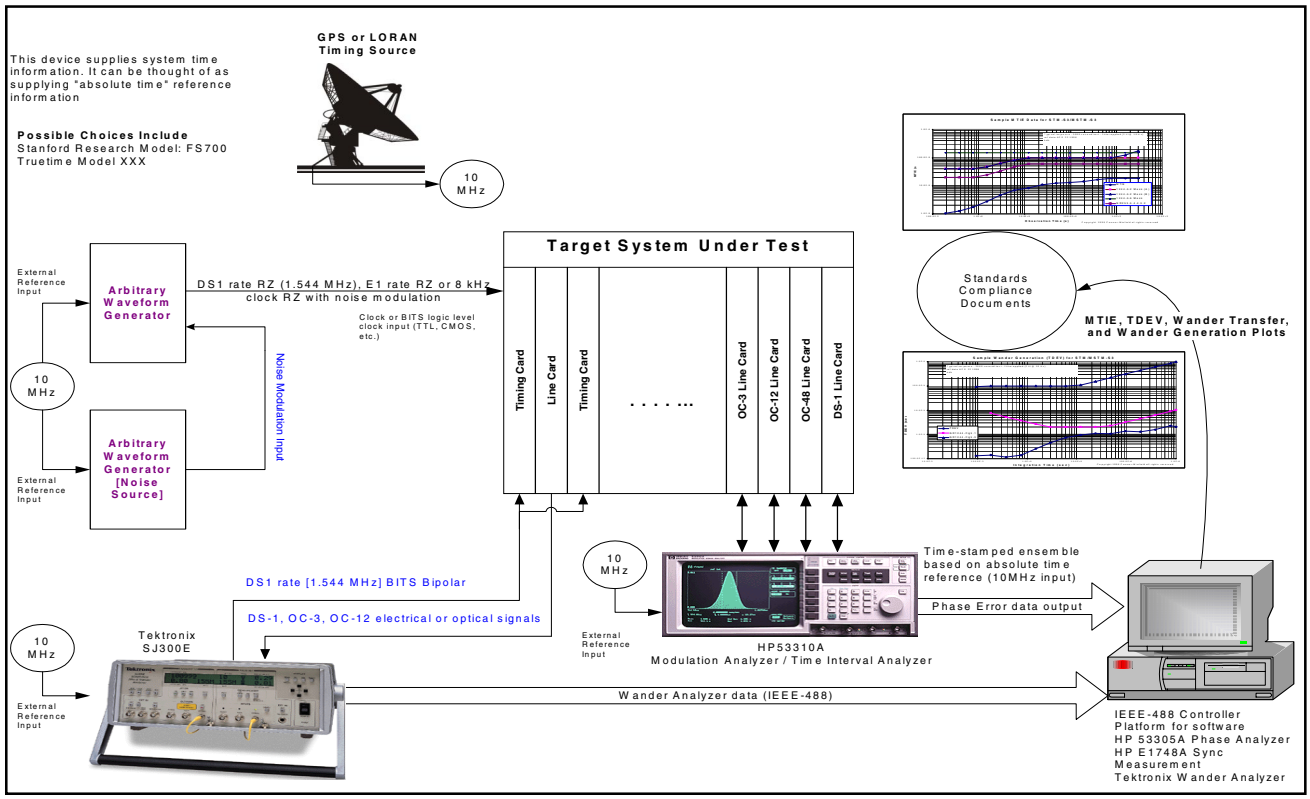
Typical Application

Figure 2



Typical System Test Set-up

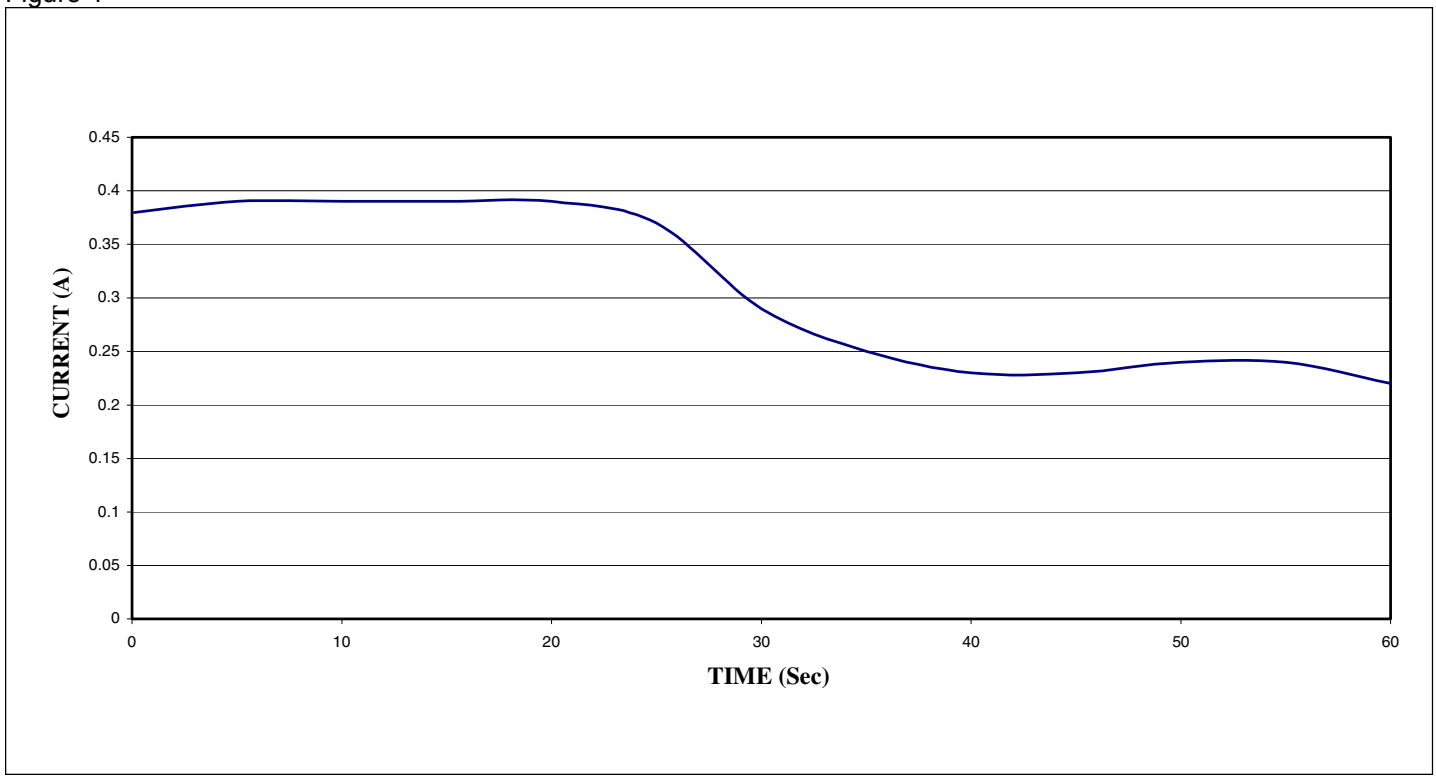
Figure 3



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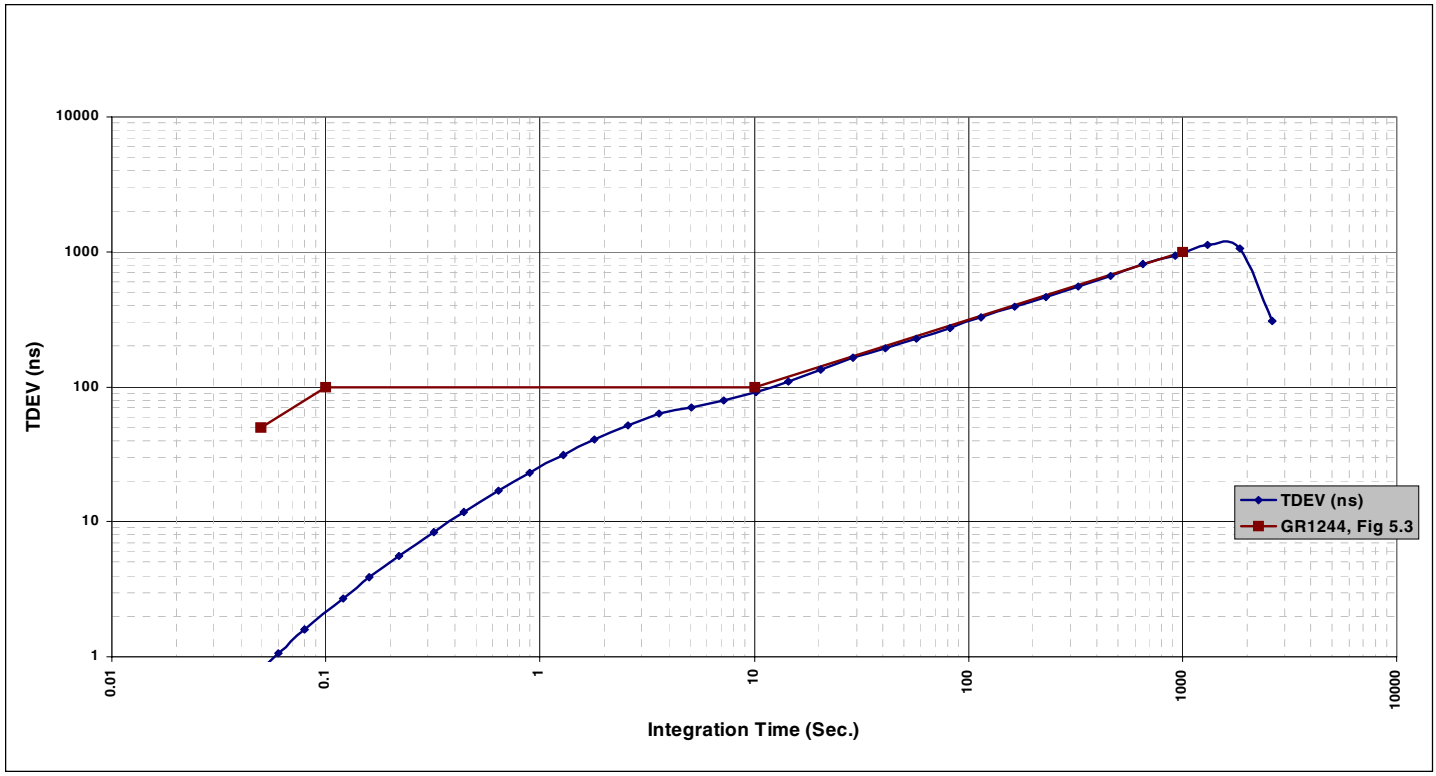
MSTM-S3-T2F1 Typical Current Draw

Figure 4



Typical Calibrated Wander Transfer TDEV

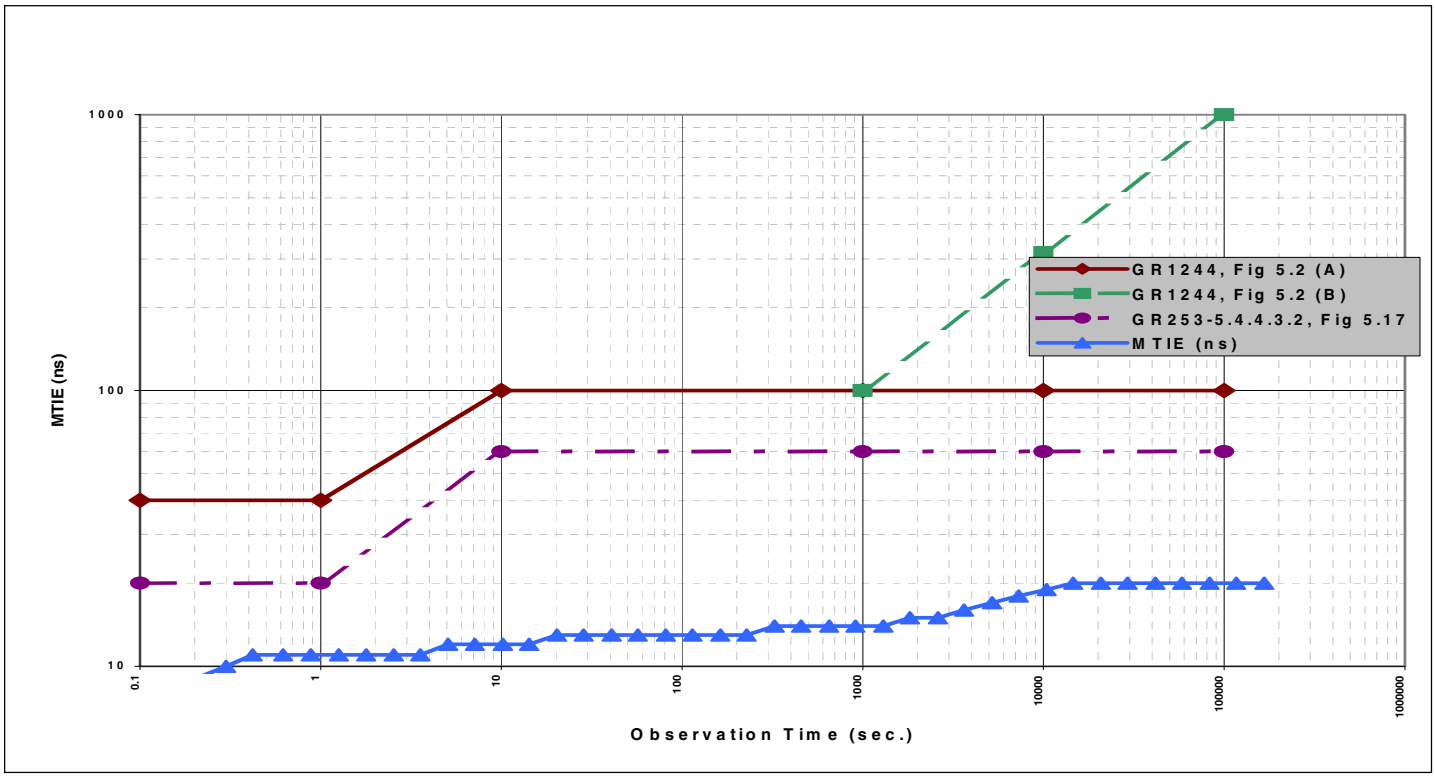
Figure 5



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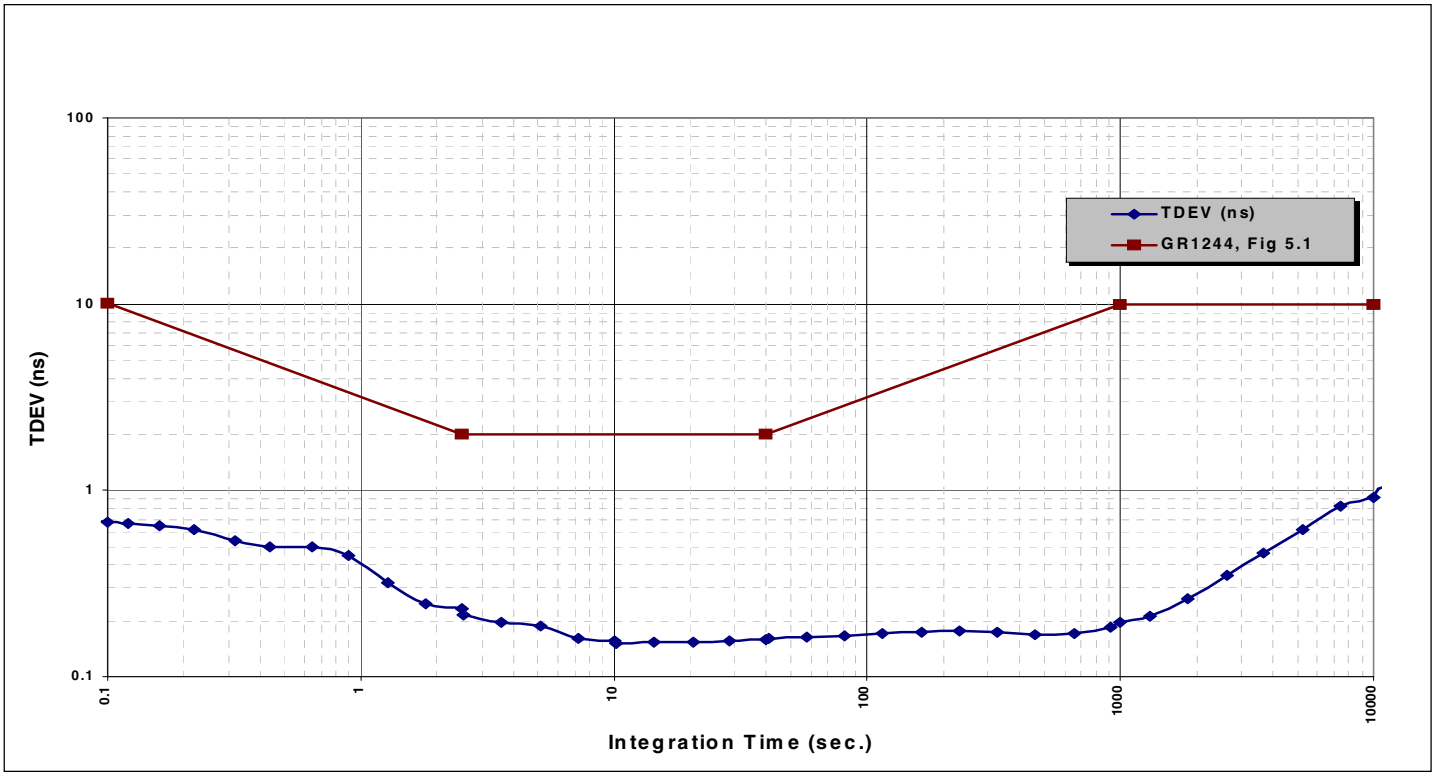
Typical Wander Generation MTIE

Figure 6



Typical Wander Generation TDEV

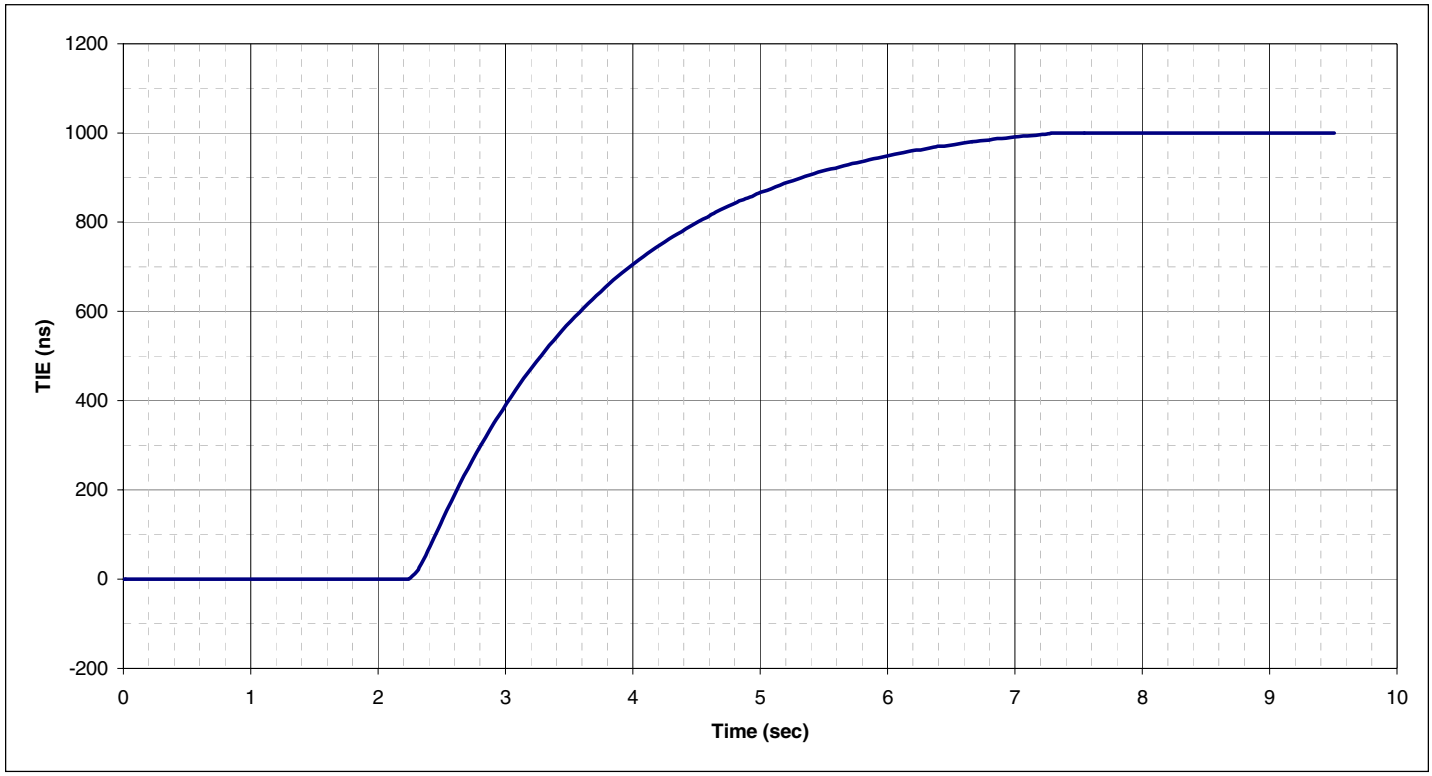
Figure 7



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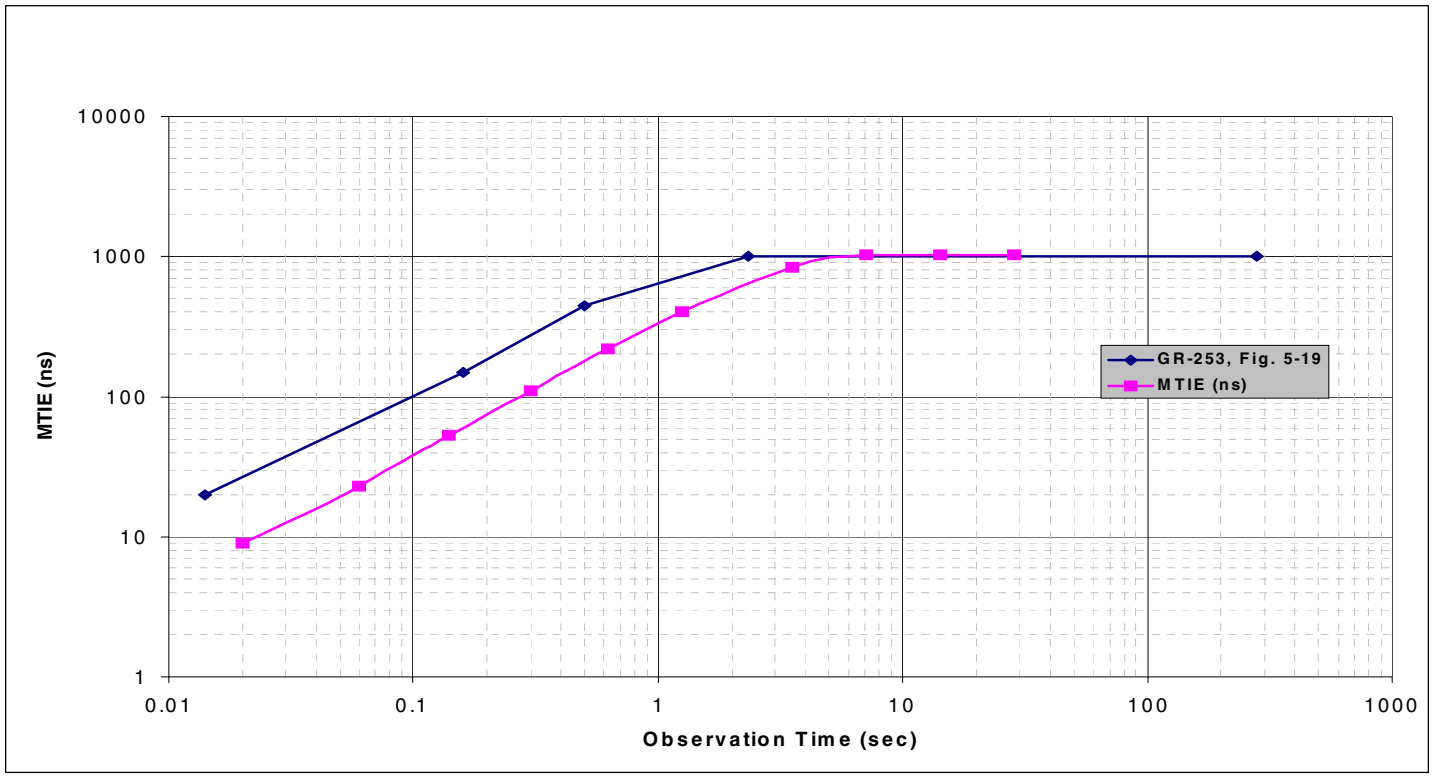
1µs Phase Transient TIE

Figure 8



1µs Phase Transient MTIE

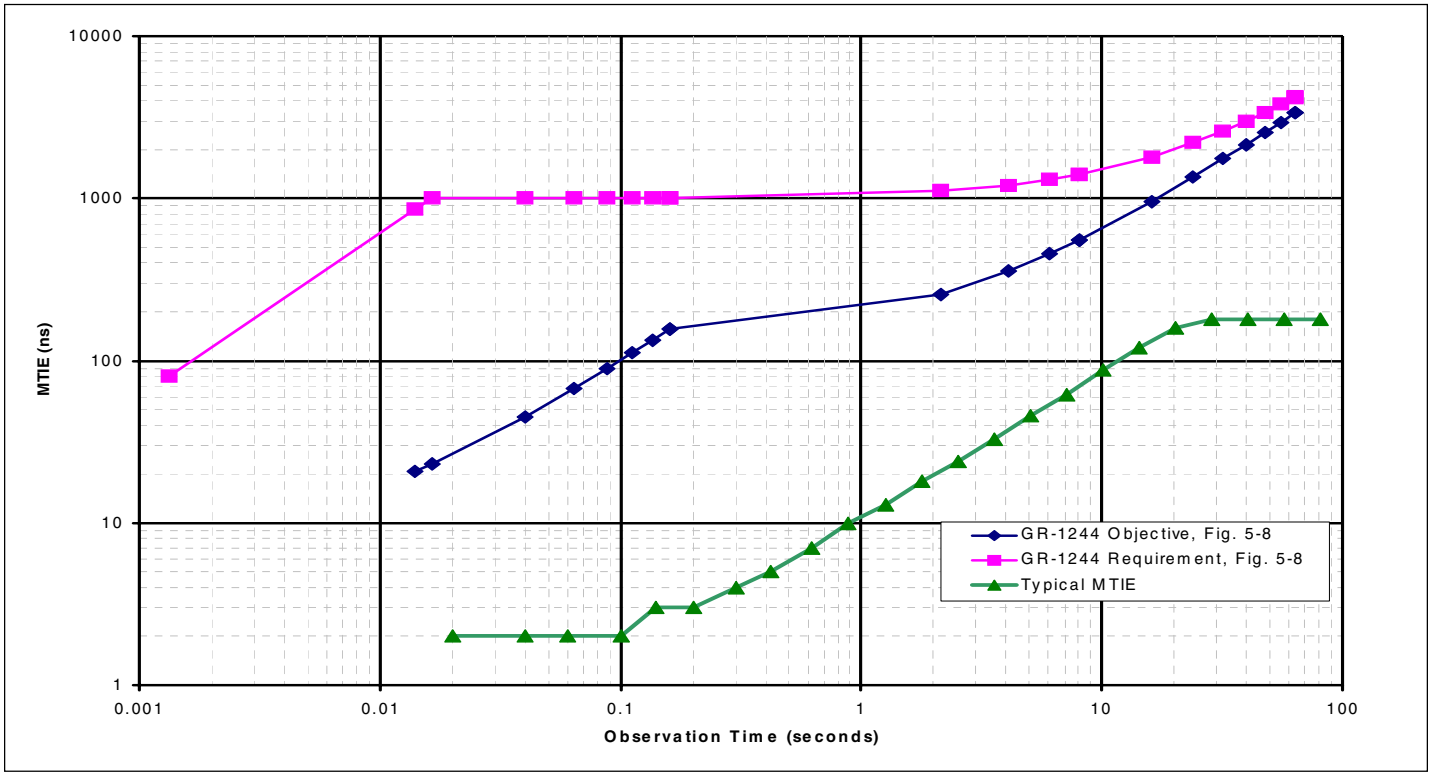
Figure 9



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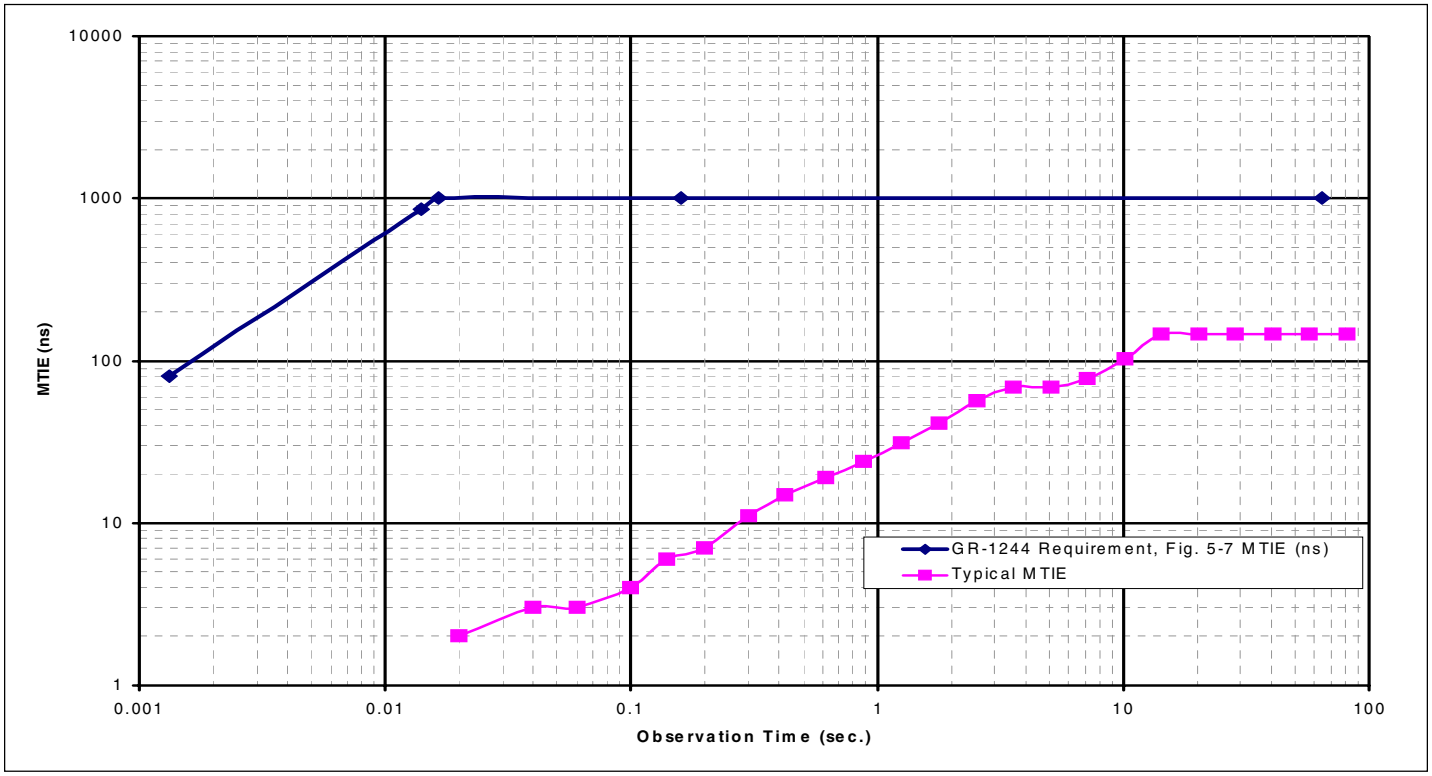
Entry Into Hold Over

Figure 10



Return from Hold Over

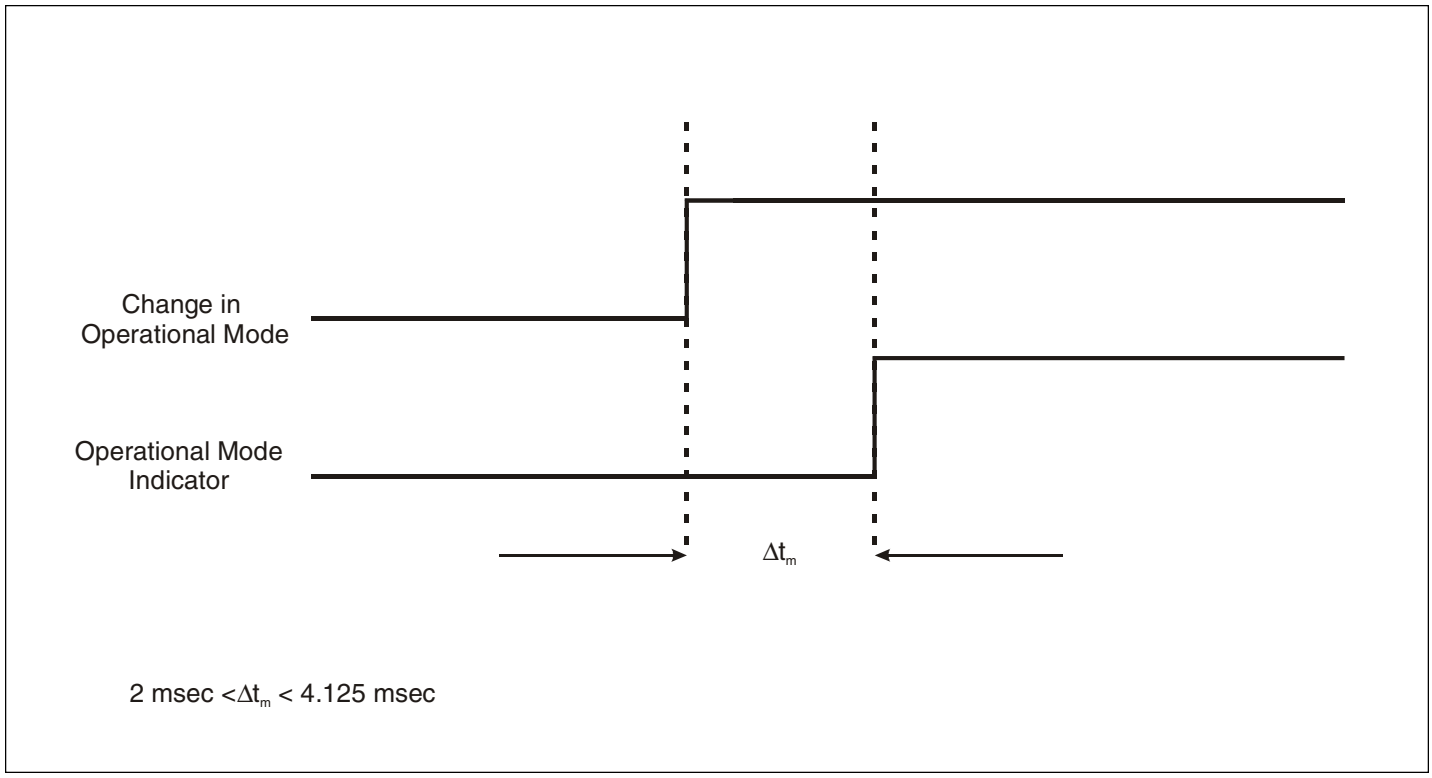
Figure 11



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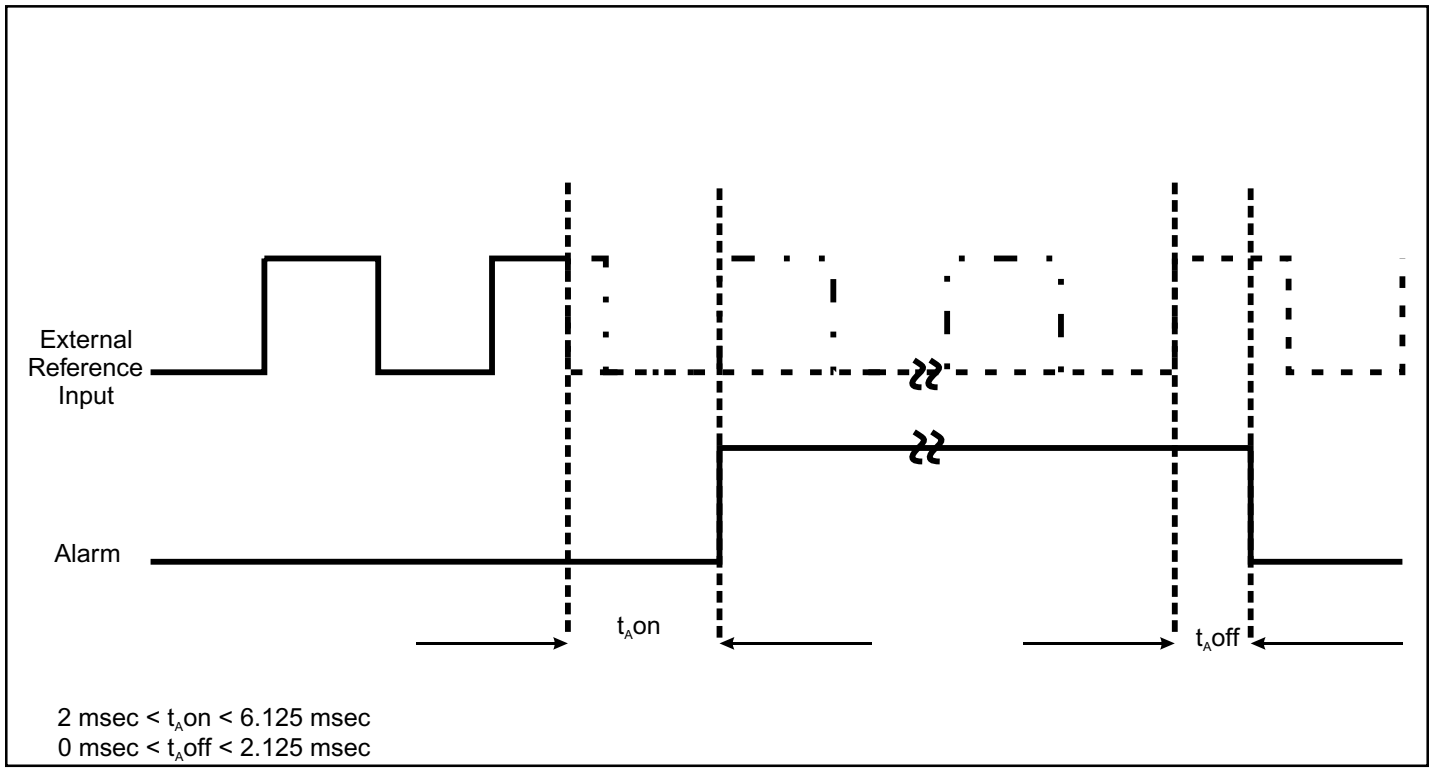
MSTM-S3-T2F1 Mode Indicator Delay

Figure 12



Loss of Reference Timing Diagram

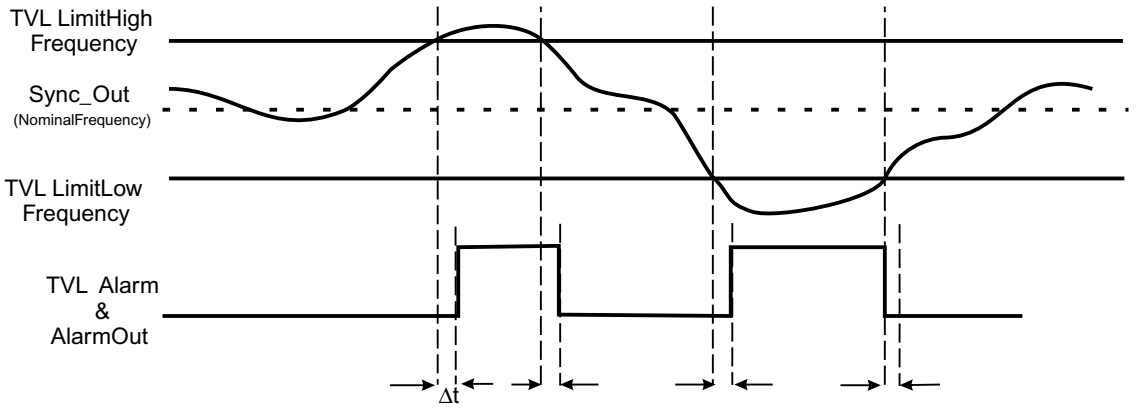
Figure 13



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Tuning Voltage Limit Alarm Timing Diagram

Figure 14

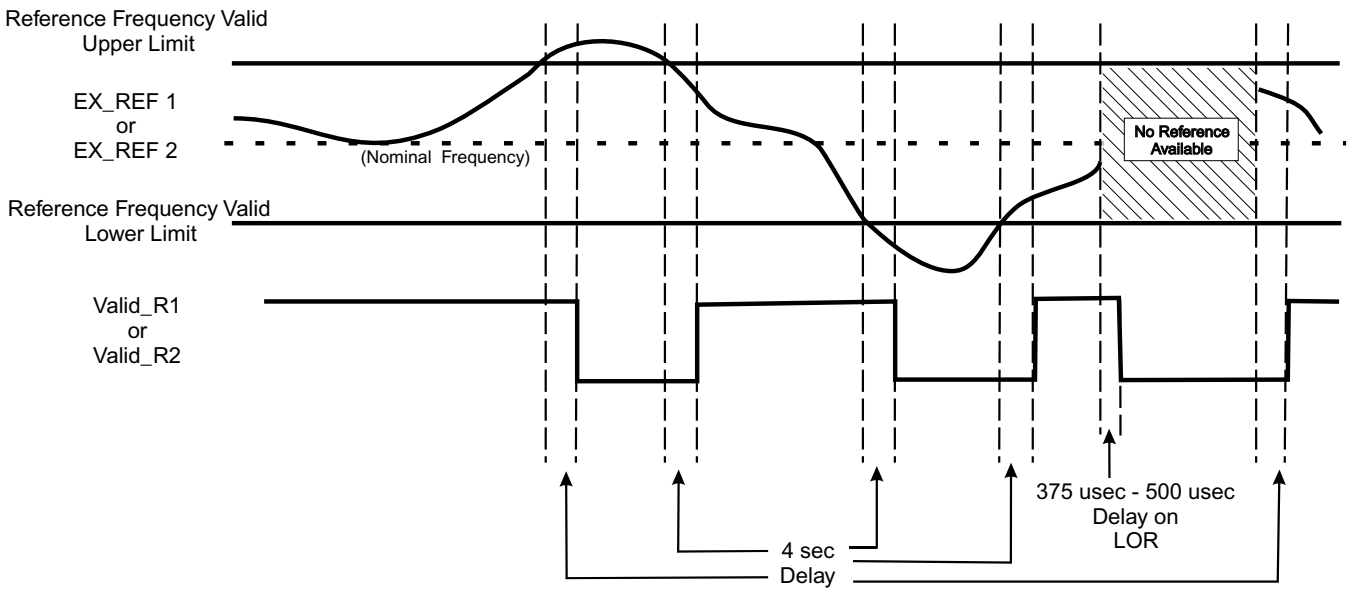


0< Δt<2.125msec

*The DAC is updated only when the output changes level. The maximum update rate is 8kHz

Valid Reference Qualification Timing Diagram

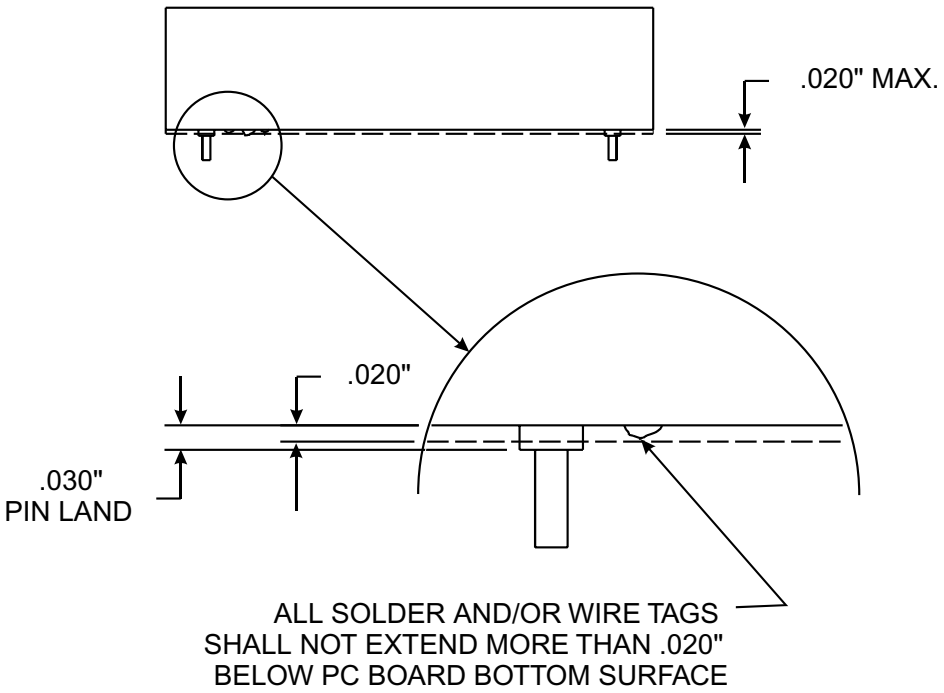
Figure 15



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Solder Clearance

Figure 16



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MECHANICAL OUTLINE:

The mechanical outline of the MSTM-S3-T2F1 is shown in Figure 17. The board space required is 2" x 2". The pins are .040" in diameter and are .150" in length. The unit is spaced off the PCB by .030" shoulders on the pins. Due to the height of the device it is recommended to have heat sensitive devices away where the air flow might not be blocked.

PAD ARRAY AND PAD SPACING:

The pins are arranged in a dual-in-line configuration as shown in Figure 16. There is .2" space between the pins in-line and each line is separated by 1.6". See Figures 17 & 18 and Table 6.

PAD CONSTRUCTION:

The recommended pad construction is shown in Figure 18. For the pin diameter of .040" a hole diameter of .055" is suggested for ease of insertion and rework. A pad diameter of .150" is also suggested for support. This leaves a spacing of .050" between the pads which is sufficient for most signal lines to pass through.

SOLDER MASK:

A solder mask is recommended to cover most the top pad to avoid excessive solder underneath the shoulder of the pin to avoid rework damage. See Table 6 and Figure 19.

VIA KEEP OUT AREA:

It is recommended that there be no vias or feed throughs underneath the main body of the module between the pins. It is suggested that the traces in this area be kept to a minimum and protected by a layer of solder mask. See Figure 18.

GROUND AND POWER SUPPLY LINES:

Power specifications will vary depending primarily on the temperature range. At wider temperature ranges starting at 0 to 70 deg. C., an ovenized oscillator, OCXO, will be incorporated. The turn-on current for an OCXO requires a peak current of about .4A for about a minute. The steady state current will the vary from 50-150 mA depending on the temperature. It is suggested to plan for the peak current in the power and ground traces pin 18 and pin 5. The other four ground pins 10, 12, 14, and 16 are intended for signal grounds.

POWER SUPPLY REGULATION:

Good power supply regulation is recommended for the MSTM-S3-T2F1 The internal oscillators are regulated to operate from 4.75 - 5.25 volts. Large jumps within this range may still produce varying degrees of wander. If the host system is subject to large voltage jumps due to hot-swapping and the like, it is suggested that there be some form of external regulation such as a DC/DC converter.

SOLDERING RECOMMENDATIONS:

Due to the sensitive nature of this part, hand soldering or wave soldering of the pins is recommended after reflow processes.

WASHING RECOMMENDATIONS:

The MSTM-S3-T2F1 is not in a hermetic enclosure. It is recommended that the leads be hand cleaned after soldering. Do not completely immerse the module.

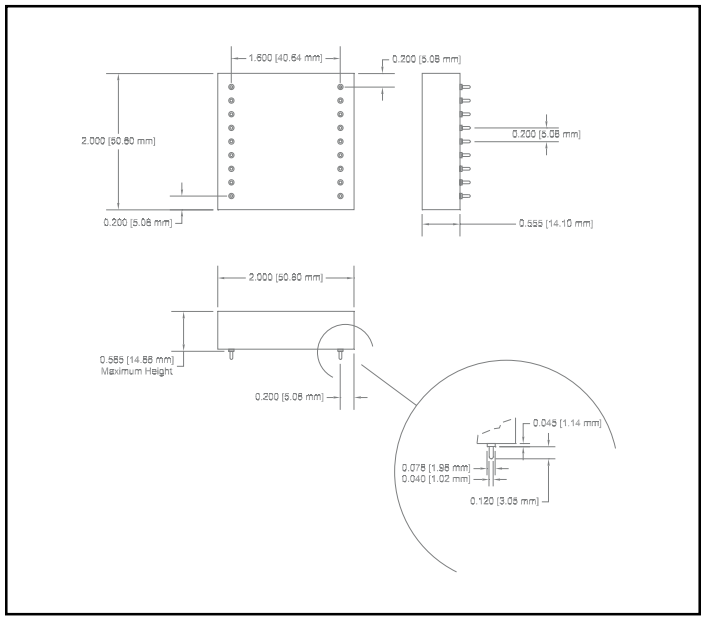
MODULE BAKEOUT:

Do not bakeout the MSTM-S3-T2F1

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Package Dimensions

Figure 17



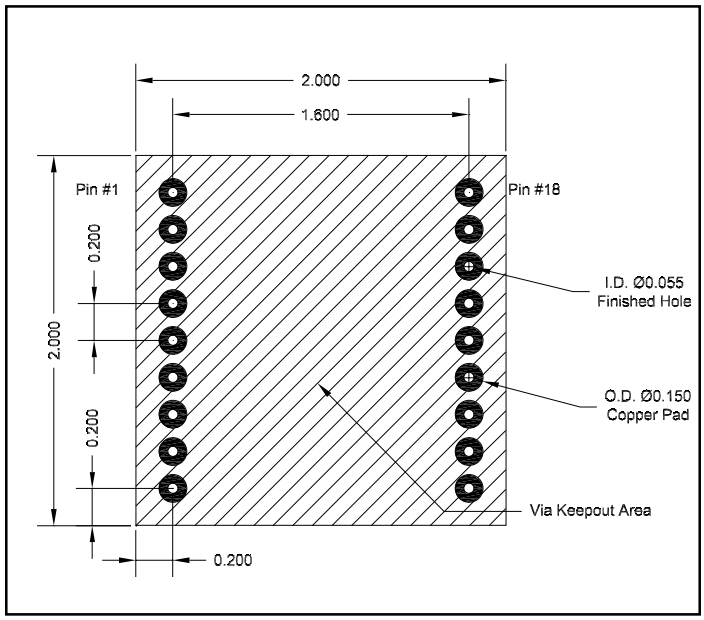
Characteristic Measurements

Table 9

Characteristic Item	Measurement (inches)
Pad to Pad Spacing	0.200
Solder pad top O.D.	0.150
Solder pad top I.D.	0.055
Solder pad bottom O.D.	0.150
Solder pad bottom I.D.	0.055
Solder mask top dia.	0.070
Solder mask bottom dia.	0.155
Pin row to row spacing	1.600

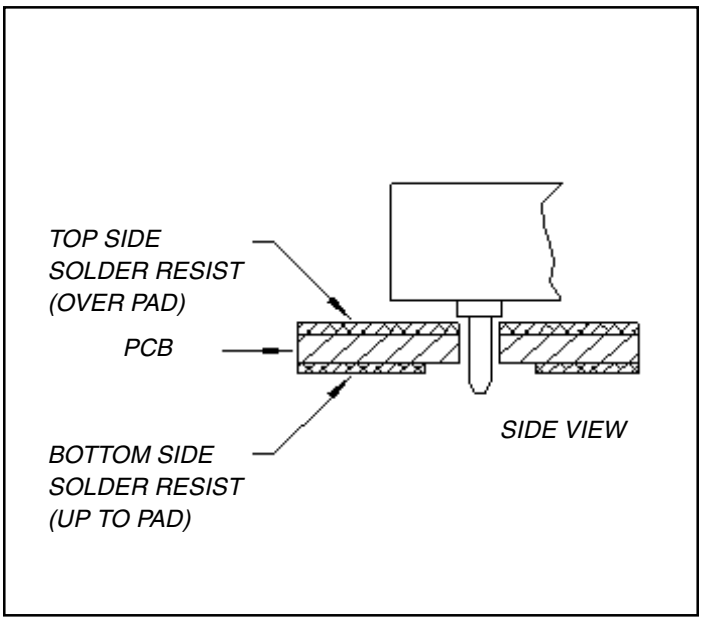
Recommended Footprint Dimensions

Figure 18



Side Assembly View

Figure 19



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Revision	Revision Date	Note
A00	10/03/01	Advance Info Data Sheet