mosaic

MSM8512C - 020

Issue 5.2 April 2001

Description

The MSM8512C is a 512K x 8 SRAM monolithic device available in Chip Size BGA (Ball Grid Array) package, with access times of 20ns. The device is available to commercial and industrial temperature grades.

The Chip Size BGA provides an ultra high density memory packaging solution.

The Chip Size BGA occupies less than 50% of the board area of conventional SOP, SOJ and TSOP II packages.

Features

- Access times of 20 ns.
- 5V ± 10%, (3.3V Under Development)
- Commercial & Industrial temperature grades
- Chip Size BGA.
- 48 pad, 1mm pad pitch, package.
- Eutectic 63/67 solder ball attach.
- Low Power Dissipation.

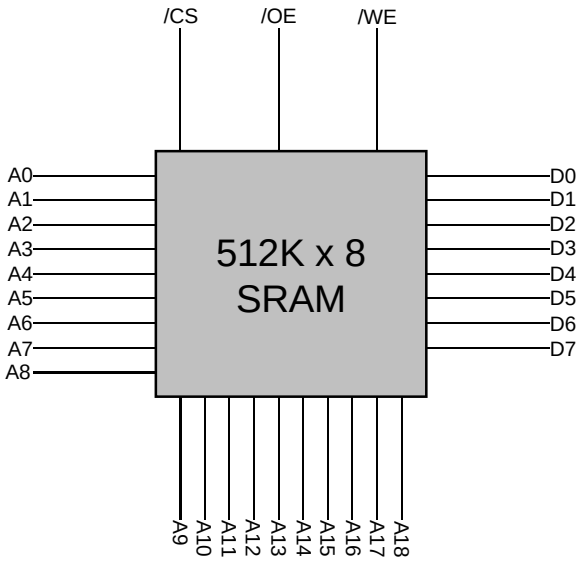
Operating	1 W (max)
Standby (CMOS)	66mW (max)

- Completely Static Operation.
- 4 layer BT substrate with power and ground planes.
- Pinout and footprint will remain the same in the event of a die shrink.

Package Details

48D - 48 Ball, 1mm pitch Chip Size BGA
Max. Dimensions (mm) - 8.00 x 10.00 x 1.40

Block Diagram



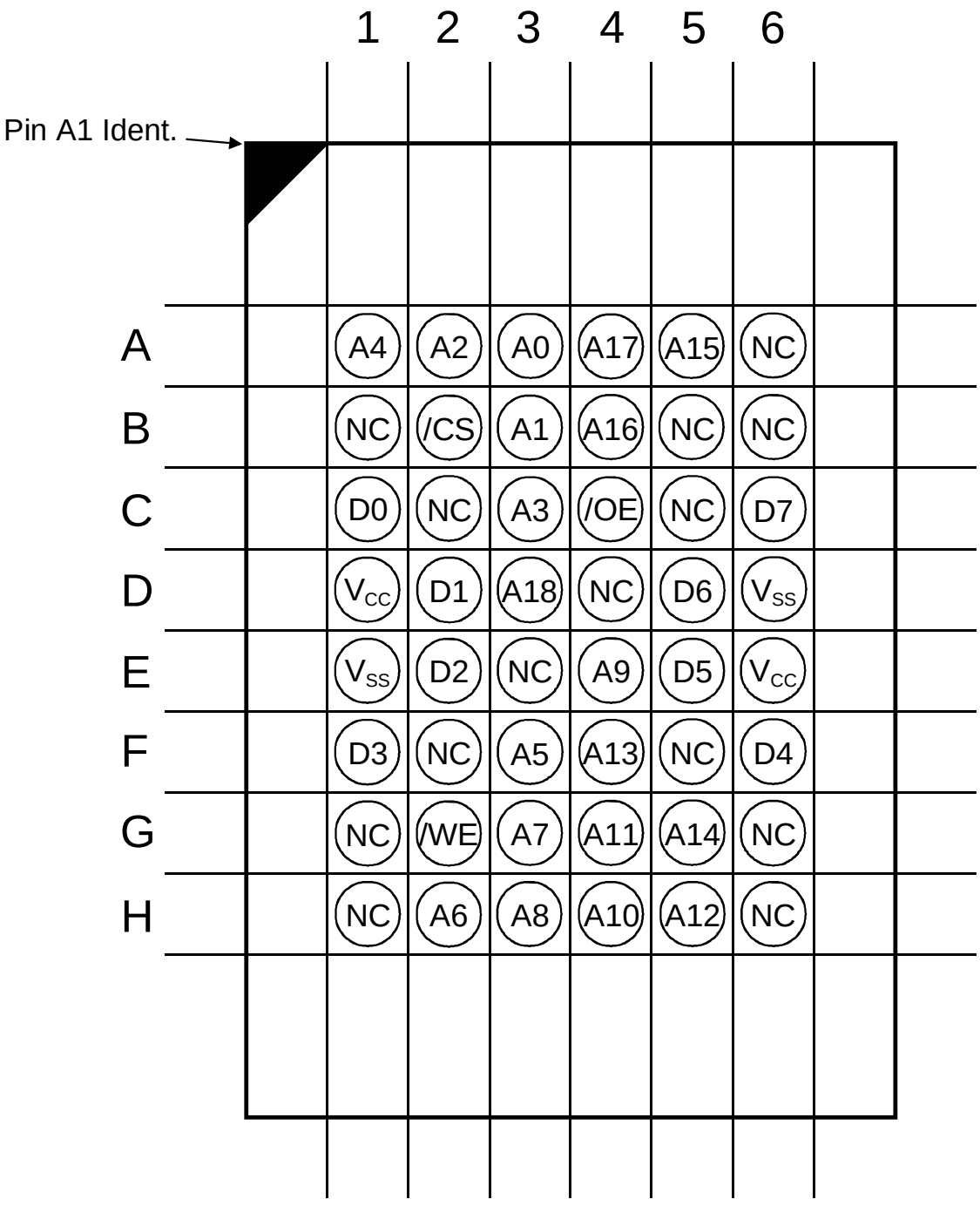
Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A18
Data Input/Output	D0~D7
Chip Select	/CS
Write Enable	/WE
Output Enable	/OE
No Connect	NC
Power	V_{CC}
Ground	GND

Pinout (Top View)



Note : Pinout shows top view,
balls facing down.

Absolute Maximum Ratings(1)

Parameter	Symbol	Min		Max	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5	to	+6.0	V
Power Dissipation	P_T		1		W
Storage Temperature	T_{STG}	-55	to	+150	^{O}C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	6.0	V	
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	^{O}C	
	T_{AI}	-40	-	85	^{O}C	(I Suffix)

DC Electrical Characteristics

(V_{CC}=5V±10%, T_A= -40^{O}C to 85^{O}C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-2	-	2	µA
Output Leakage Current	I_{LO}	/CS=V_{IH} or /OE=V_{IH} or /WE=V_{IL}, V_{OUT}=V_{SS} to V_{CC}	-2	-	2	µA
Operating Supply Current	I_{CC1}	Min. Cycle, 100% Duty /CS=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	-	-	180	mA
Standby Supply Current	I_{SB}	Min. Cycle, /CS=V_{IH}	-	-	60	mA
	I_{SB1}	f=0MHz, CS≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V	-	-	12	mA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Capacitance

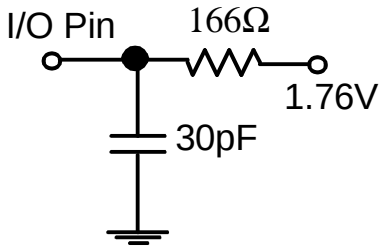
(V_{CC} = 5.0V±10% T_A = 0°C to 70°C)

Parameter	Symbol	Test Condition	Typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 3ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- V_{CC} = 5V±10%

Output Load



Functional Description

/CS	/WE	/OE	Mode	I/O Pin	Supply Current
H	X	X	Not Select	High-Z	I_{SB},I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X = Don't Care

Read Cycle

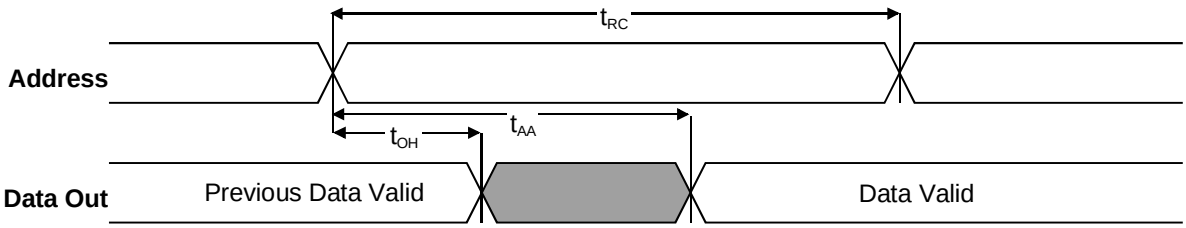
		20		
Parameter	Symbol	Min	Max	Units
Read Cycle Time	t_{RC}	20	-	ns
Address Access Time	t_{AA}	-	20	ns
Chip Select to Output	t_{CO}	-	20	ns
Output Enable to Valid Output	t_{OE}	-	9	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	ns

Write Cycle

		20		
Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	20	-	ns
Chip Select to End of Write	t_{CW}	14	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Address Valid to End of Write	t_{AW}	14	-	ns
Write Pulse Width (/OE High)	t_{WP}	14	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Write to Output High-Z	t_{WHZ}	0	9	ns
Data to Write Time Overlap	t_{DW}	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	ns

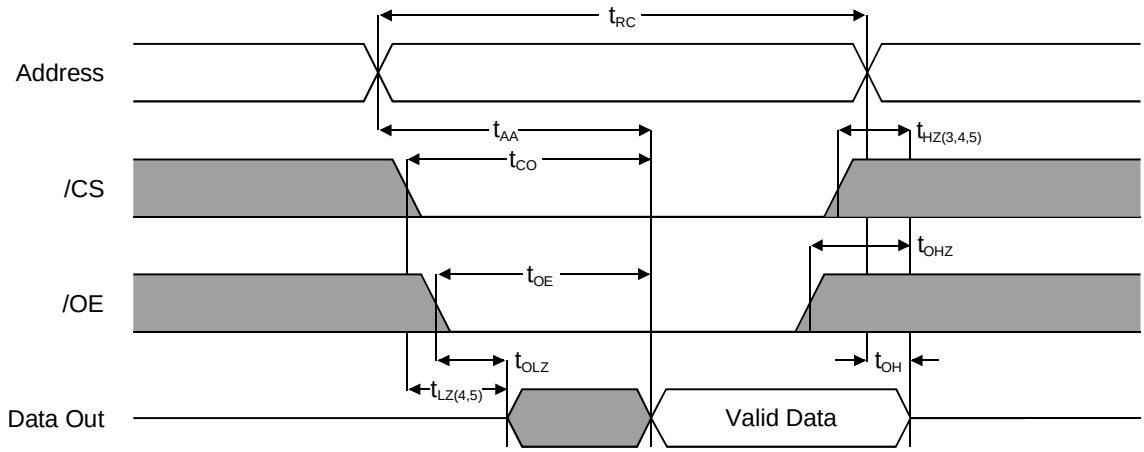
Read Cycle 1

(Address Controlled, /CS=/OE=V_{IL}, /WE=V_{IH})



Read Cycle 2

(/WE = V_{IH})

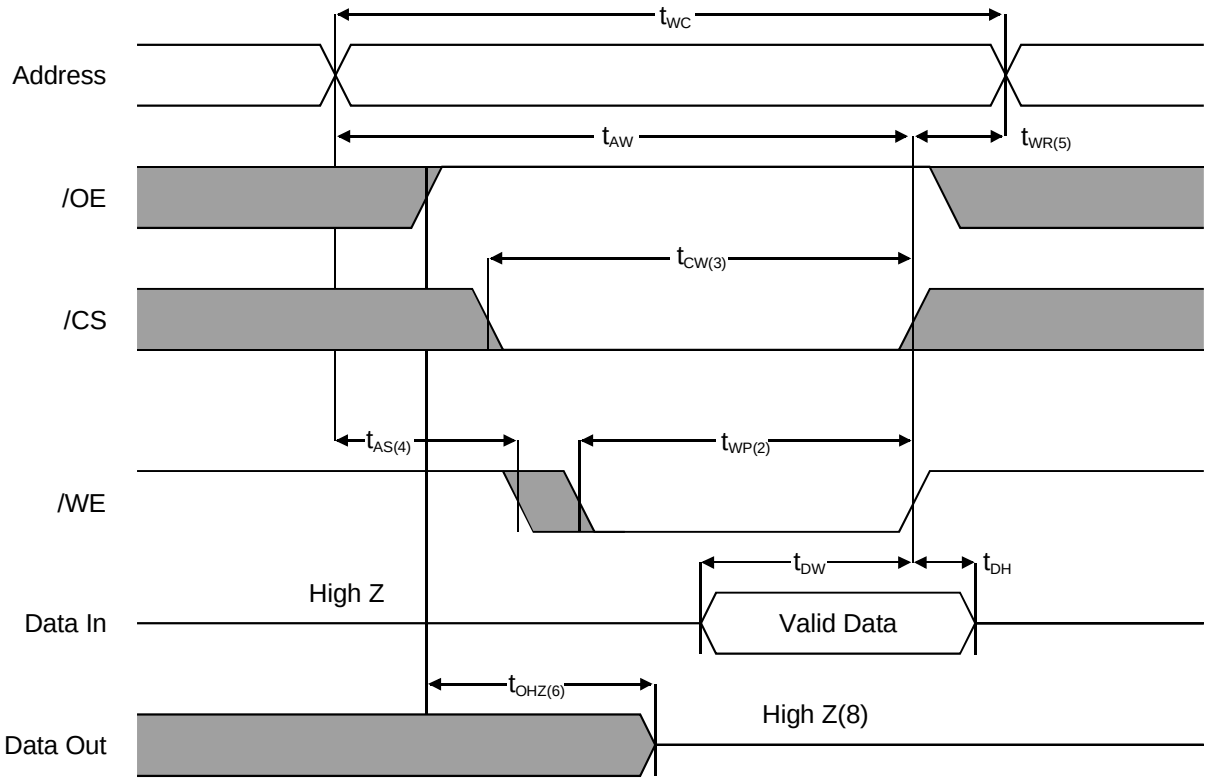


NOTES(READ CYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS=V_{IL}.
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

Write Cycle 1

(/OE = Clock)

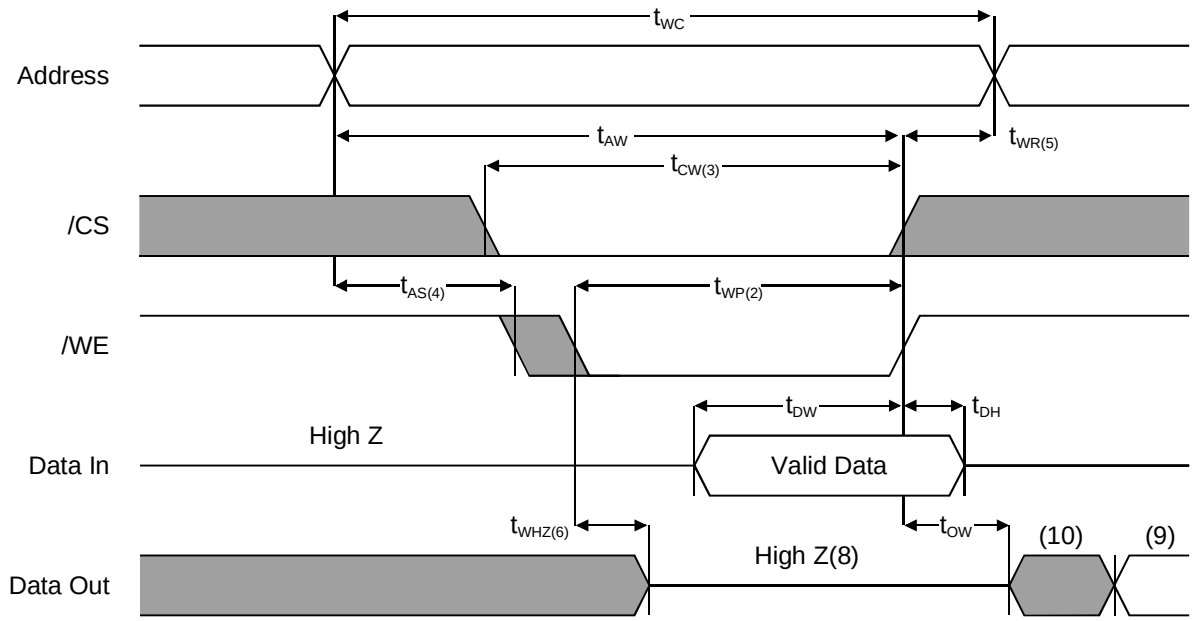


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 2

(/OE = Low Fixed)

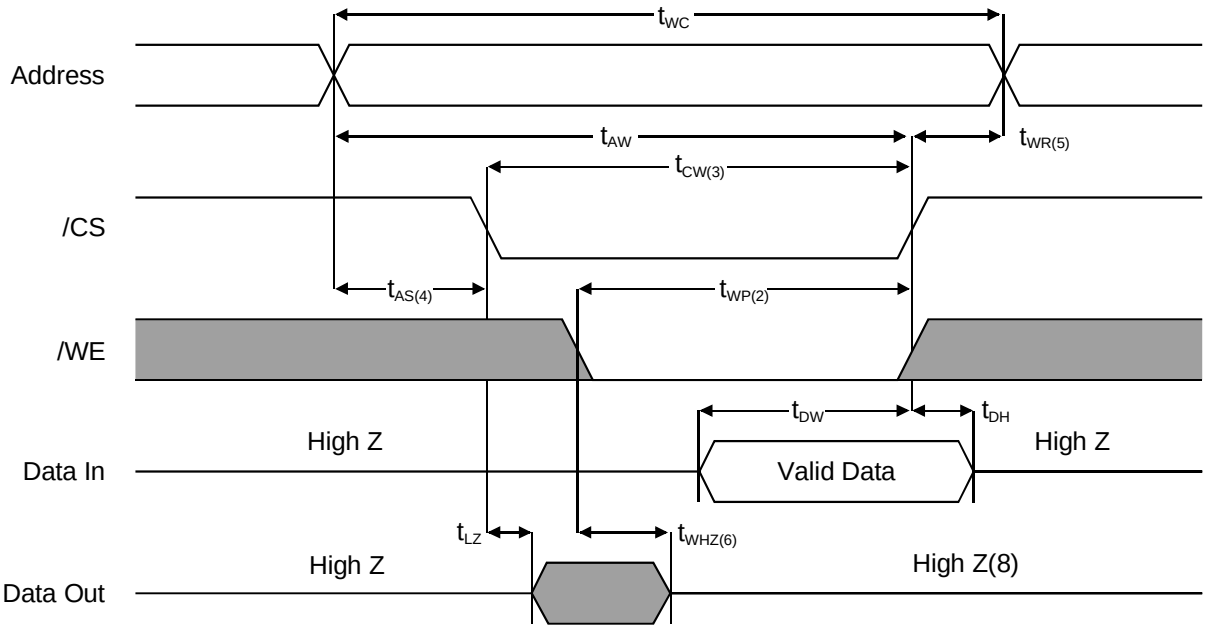


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 3

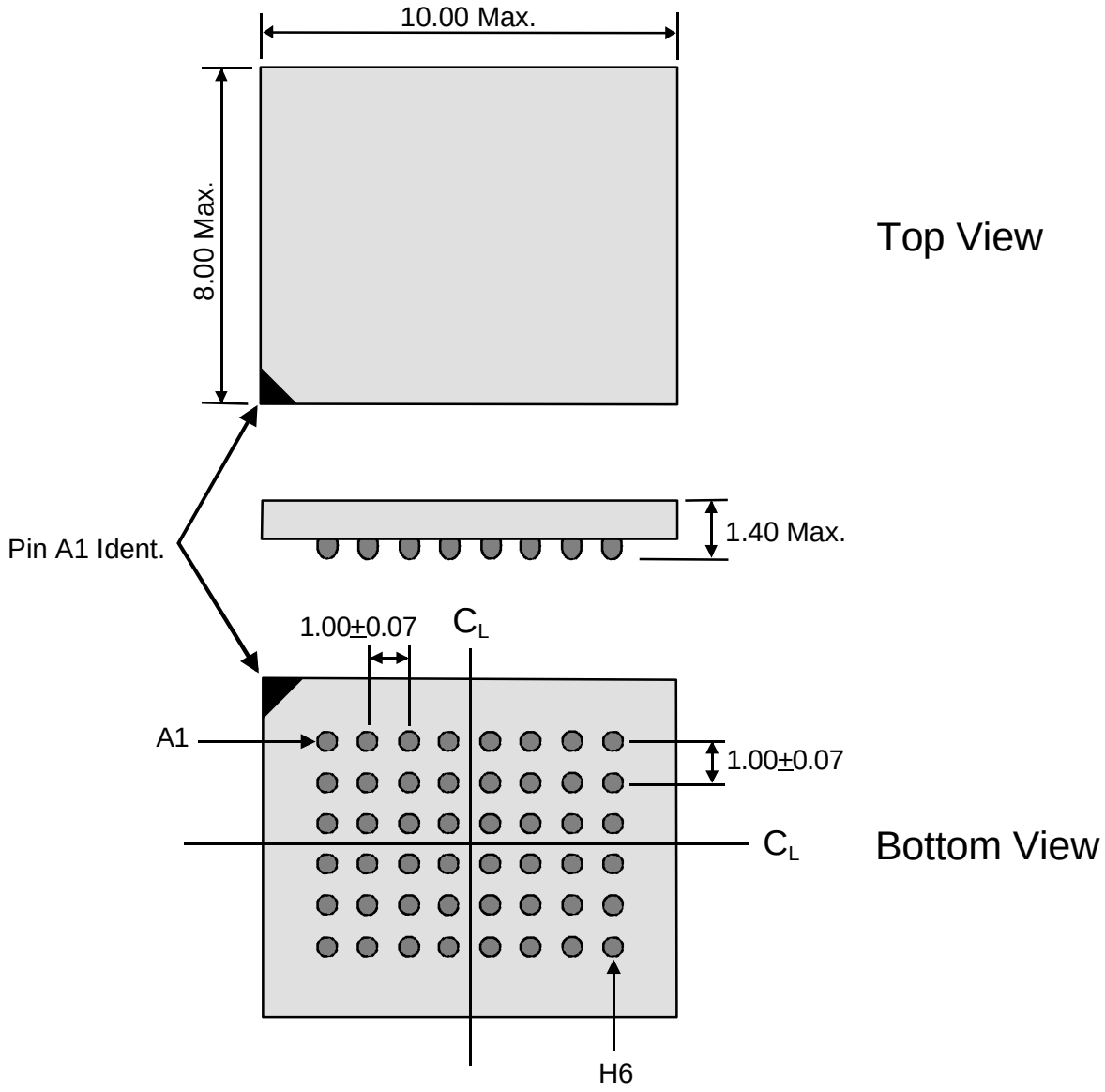
(/CS = Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Chip Size BGA - 48 pad



General Reliability Data	
High Temperature Operating Life	125^{O}C / 6V / 1000hrs
High Temperature Storage Life	150^{O}C / 1000hrs
Autoclave	121^{O}C / 100% RH / 168hrs
Temperature Cycling	-55 ~ 125^{O}C / 1000 cycles
Moisture Sensitivity	JEDEC Level 3 30^{O}C / 60% RH / 192hrs
^{O}JA Thermal Performance	30 ~ 45^{O}C/Watt

Ordering Information

MSM8512CB I - 020/48D

48D	48D	=	48 Pad package, 1mm Pitch
Speed	020	=	20ns
Temp. Range/Screening	Blank	=	Commercial
	I	=	Industrial
Power Consumption	Blank	=	Standard Power
Package	B	=	Chip Size BGA
Die Revision	C	=	'C' Rev die.
Memory Organisation	8512	=	512K x 8
Family	M	=	Monolithic
Technology	S	=	SRAM

Note :
Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.
Our products are subject to a constant process of development. Data may be changed without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.