

Features

- n High-speed – 15/20/25/35 ns
- n Low Power dissipation:
MS62256HL
1.1W (Max.) Operating
1mW (Max.) Power down
- n Fully static operation
- n All inputs and outputs directly TTL compatible
- n Three state outputs
- n Ultra low data retention supply current at
 $V_{CC} = 2V$

Description

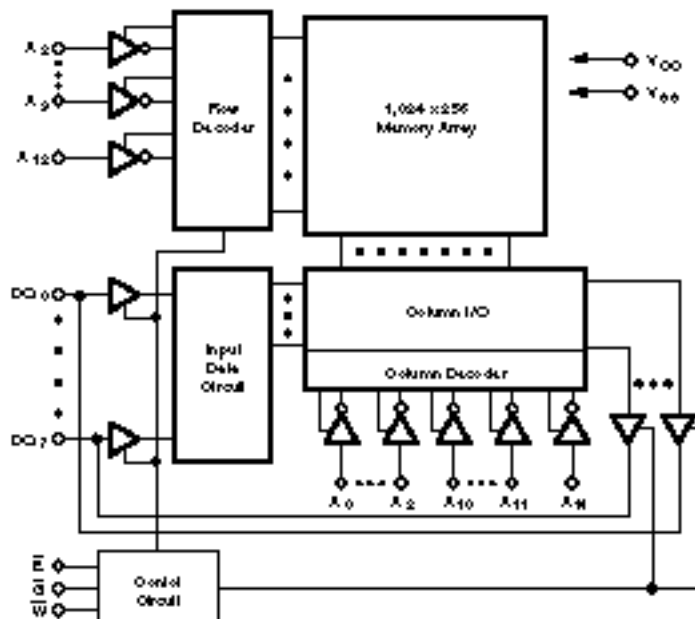
The MS62256H is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL-VITELIC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256H is available in the following standard 28-pin packages:

- 600 MIL Plastic DIP
- 300 MIL Plastic DIP
- 300 MIL Small Outline J-Bend (SOJ)

Pin Configurations



Functional Block Diagram



Pin Descriptions**A₀ - A₁₄ Address Inputs**

These 15 address inputs select one of the 32768 8-bit words in the RAM.

E Chip Enable Input

E is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

G Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when G is inactive.

W Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when W is HIGH and G is LOW, output data will be present at the DQ pins; when W is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ₀ - DQ₇ Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply**V_{SS} Ground****Truth Table**

Mode	<u>E</u>	<u>G</u>	<u>W</u>	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D _{OUT}
Output Disabled	L	H	H	High Z
Write	L	X	L	D _{IN}

Operating Range

Range	Ambient Temperature	V _{cc}
Commercial	0°C to +70°C	5V ± 10%

Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Rating	Units
V _{CC}	Supply Voltage	-0.3 to 7	V
V _{IN}	Input Voltage	-0.3 to 7	
V _{DO}	Input/Output Voltage Applied	-0.3 to 6	
T _{BIAS}	Temperature Under Bias	Plastic -10 to +125	°C
T _{STG}	Storage Temperature	Plastic -40 to +150	°C
P _D	Power Dissipation	1.2	W
I _{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability and degrade performance characteristics.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS62256H			Units
			Min.	Typ. ⁽¹⁾	Max.	
V_{IL}	Guaranteed Input Low Voltage ^(2,3)		-0.3	-	0.8	V
V_{IH}	Guaranteed Input High Voltage ⁽²⁾		2.2	-	6.0	V
I_{IL}	Input Leakage Current	$V_{CC} = \text{Max}, V_{IN} = 0V \text{ to } V_{CC}$	-2	-	2	μA
I_{OL}	Output Leakage Current	$V_{CC} = \text{Max}, E = V_{IH} \text{ or } G = V_{IH}, V_{IN} = 0V \text{ to } V_{CC}$	-2	-	2	μA
V_{OL}	Output Low Voltage	$V_{CC} = \text{Min}, I_{OL} = 8mA$	-	-	0.4	V
V_{OH}	Output High Voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0mA$	2.4	-	-	V
I_{CC}	Operating Power Supply Current	$V_{CC} = \text{Max}, E = V_{IL}, I_{DQ} = 0mA, F = F_{max}^{(4)}$	-	-	200	mA
I_{CCSB}	Standby Power Supply Current	$V_{CC} = \text{Max}, E = V_{IH}, I_{DQ} = 0mA$	-	-	40	mA
I_{CCSB1}	Power Down Power Supply	$V_{CC} = \text{Max}, E \geq V_{CC} - 0.2V$	-	-	2	mA
	Current	$V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V$	-	-	130 ⁽⁵⁾	μA

1. Typical characteristics are at $V_{CC} = 5V, T_A = 25^\circ C$.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $V_{IL} (\text{Min.}) = -3.0V$ for pulse width $\leq 20ns$
4. $F_{MAX} = 1/t_{RC}$.
5. L version only.

Capacitance⁽¹⁾ $T_A = 25^\circ C, f = 1.0MHz$

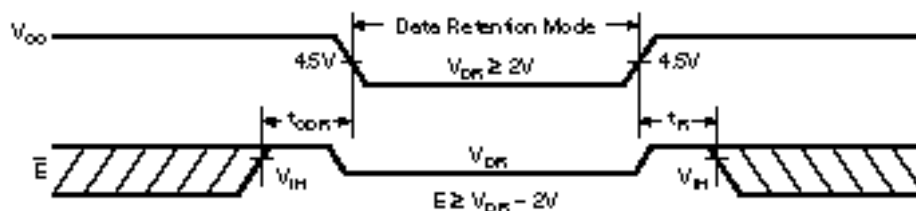
Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0V$	10	pF

1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max. ⁽²⁾	Units
V_{DR}	V_{CC} for Data Retention	$E \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V$	2.0 ⁽¹⁾	-	-	V
I_{CCDR}	Data Retention Current	$E \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V$	-	2	50 ⁽⁴⁾	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		$t_{RC}^{(3)}$	-	-	ns

1. $V_{CC} = 2V, T_A = +25^\circ C$
2. $V_{CC} = 3V$
3. t_{RC} = Read Cycle Time

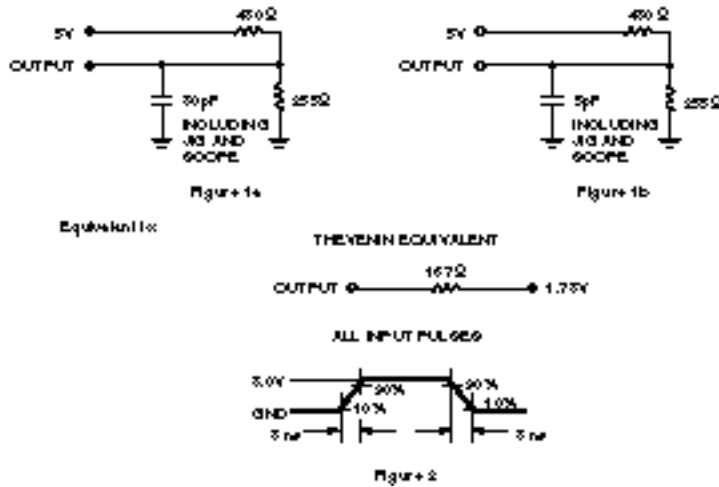
Timing Waveform Low V_{CC} Data Retention Waveform

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

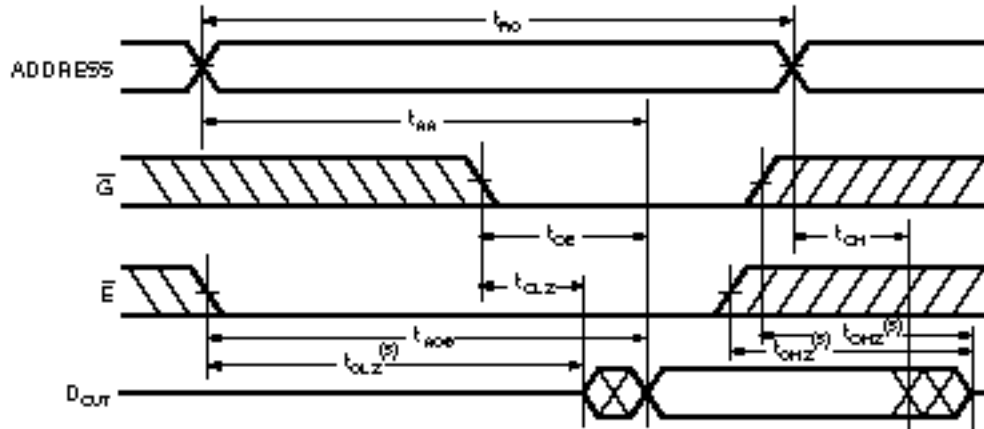
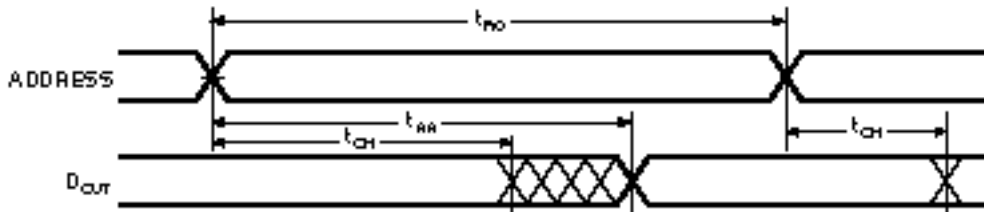
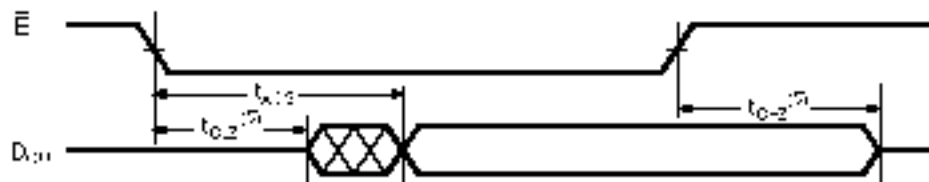
Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE 0V TO 0V	WILL BE 0V TO 0V
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DCE & NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms**AC Electrical Characteristics (over the commercial operating range)****Read Cycle**

Jedec Parameter Name	Parameter Name	Parameter	MS62256H-15 Min.	MS62256H-15 Max.	MS62256H-20 Min.	MS62256H-20 Max.	MS62256H-25 Min.	MS62256H-25 Max.	MS62256H-35 Min.	MS62256H-35 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	15	-	20	-	25	-	35	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	15	-	20	-	25	-	35	ns
t_{ELOV}	t_{ACS}	Chip Enable Access Time	-	15	-	20	-	25	-	35	ns
t_{GLOX}	t_{OE}	Output Enable to Output Valid	-	8	-	10	-	12	-	15	ns
t_{EHOZ}	t_{CLZ}	Chip Enable to Output Low Z	5	-	5	-	5	-	5	-	ns
t_{GLOX}	t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	0	-	ns
t_{EHOZ}	t_{CHZ}	Chip Disable to Output in High Z	-	8	-	8	-	10	-	15	ns
t_{GHOZ}	t_{OHZ}	Output Disable to Output in High Z	-	8	-	8	-	10	-	15	ns
t_{AXOX}	t_{OH}	Output Hold from Address Change	3	-	5	-	5	-	5	-	ns

Switching Waveforms (Read Cycle)

READ CYCLE 1⁽¹⁾READ CYCLE 2^(1, 2, 4)READ CYCLE 3^(1, 3, 4)

NOTES:

1. $\bar{W}$ is High for READ Cycle.
2. Device is continuously selected $\bar{E} = V_{IL}$.
3. Address valid prior to or coincident with $\bar{E}$ transition low.
4. $\bar{G} = V_{IL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

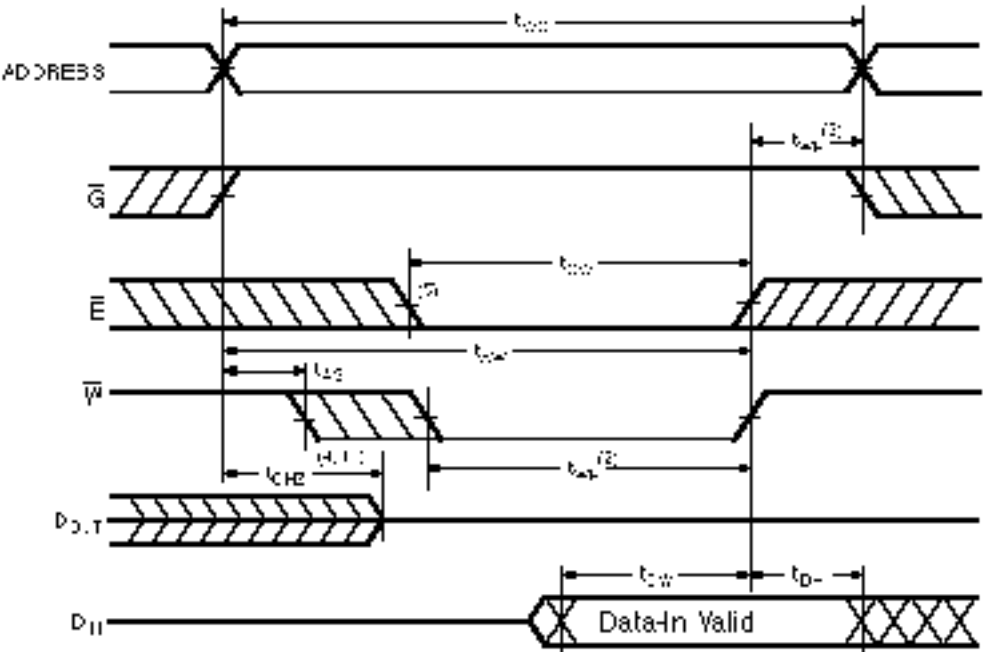
AC Electrical Characteristics (over the commercial operating range)

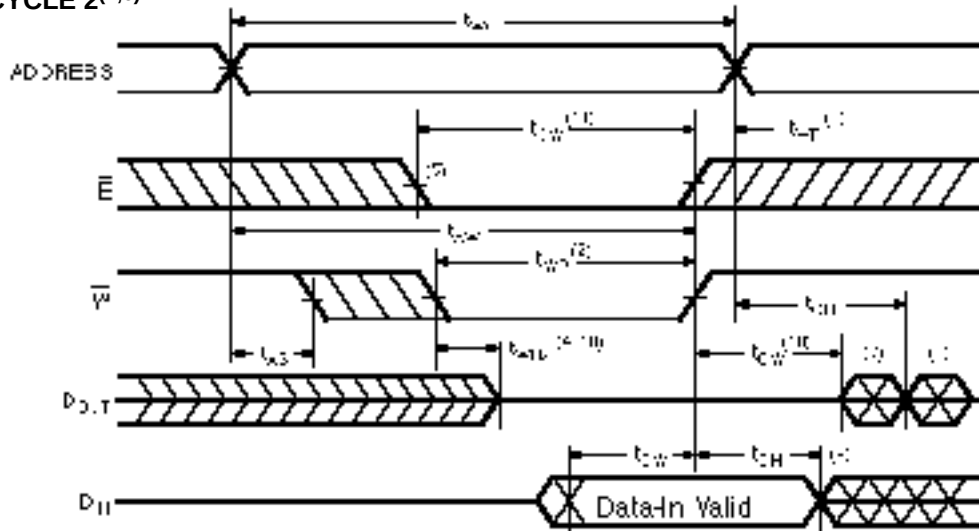
Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256H-15		MS62256H-20		MS62256H-25		MS62256H-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	15	-	20	-	25	-	35	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	10	-	15	-	20	-	25	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	10	-	15	-	20	-	25	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	12	-	12	-	15	-	20	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	ns
t_{WLOZ}	t_{WHZ}	Write to Output in High Z	0	10	0	10	0	13	0	15	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	8	-	10	-	13	-	15	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
t_{GHOZ}	t_{OHZ}	Output Disable to Output in High Z	0	8	0	8	0	10	0	-	ns
t_{WHOX}	t_{OW}	Output Active from End of Write	3	-	3	-	3	-	0	-	ns

Switching Waveforms (Write Cycle)

WRITE CYCLE 1⁽¹⁾

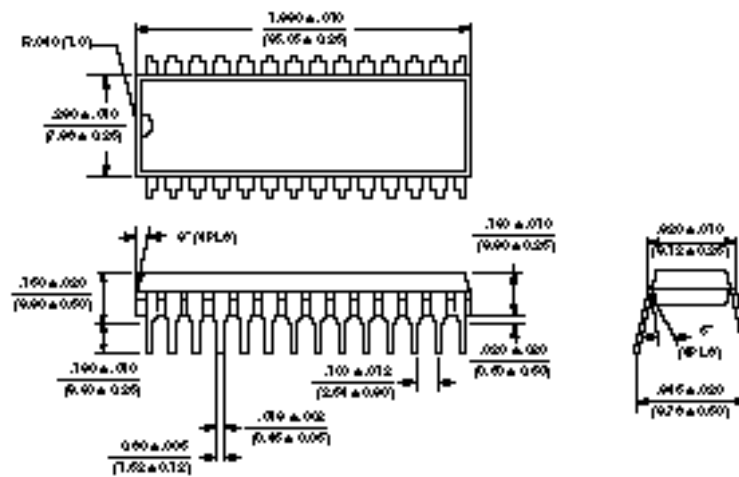
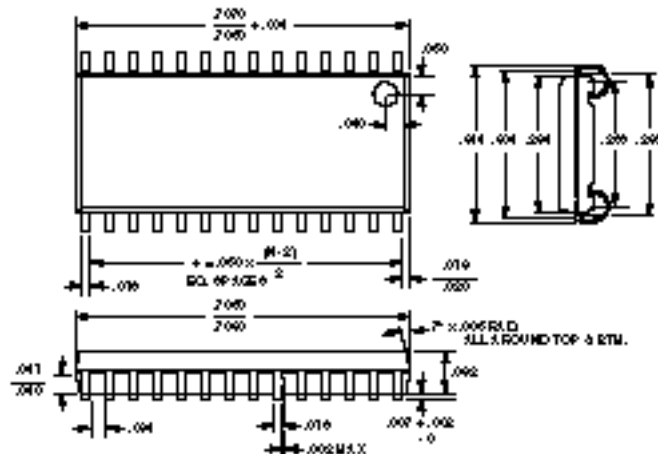


Switching Waveforms (Write Cycle)**WRITE CYCLE 2^(1,6)****NOTES:**

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speeds	Ordering Part Number	Package	Temperature Range
15	MS62256H-15NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
15	MS62256H-15RC	28 Pin Small Outline J Bend	0°C to +70°C
20	MS62256H-20NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
20	MS62256H-20RC	28 Pin Small Outline J Bend	0°C to +70°C
25	MS62256H-25NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
25	MS62256H-25RC	28 Pin Small Outline J Bend	0°C to +70°C
35	MS62256H-35NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
35	MS62256H-35RC	28 Pin Small Outline J Bend	0°C to +70°C

Package Dimensions**28 Pin 300 mil Plastic DIP****28 Pin 300 mil SOJ**

U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-00952

TAIWAN

5F, NO.. 102
MIN CHUAN E. ROAD, SEC.3
TAIPEI
PHONE: 011-886-2-545-1213
FAX: 011-886-2-545-1214

JAPAN

RM.302 ANNEX-G
HIGASHI-NAKANO
NAKANO-KU, TOKYO 164
PHONE: 011-81-03-3365-2851
FAX: 011-81-03-3365-2836

KOREA

RM. 309, BEUK-EUN BLDG.
1339-1 SEOCHO-DONG,
SEOCHO-KU
SEOUL, KOREA
PHONE: 011-82-2-553-3385
FAX: 011-82-2-553-3675

HONG KONG

19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 011-852-665-4883
FAX: 011-852-664-7535

1 R&D ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 011-886-35-770055
FAX: 011-886-35-776520

KSP R&D C-4F, SSAKADO 3-2-1
TAKATSU-KU, KAWASAKI-SHI
KANAGAWA PREF 213
PHONE: 011-81-04-4812-4397
FAX: 011-81-04-4812-4074

U.S. SALES OFFICES**NORTHWESTERN**

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

SOUTHWESTERN

SUITE 200
5150 E. PACIFIC COAST HWY.
LONG BEACH, CA 90804
PHONE: 310-498-3314
FAX: 310-597-2174

CENTRAL & SOUTHEASTERN

604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 214-690-1402
FAX: 214-690-0341

NORTHEASTERN

SUITE 306
71 SPITBROOK ROAD
NASHUA, NH 03062
PHONE: 603-891-2007
FAX: 603-891-3597

The information in this document is subject to change without notice.

MOSEL-VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL-VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL-VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.