MPQ2456

0.5A, 50V, 1.2MHz
Step-Down Converter in a TSOT23-6

The Future of Analog IC Technology

DESCRIPTION

The MPQ2456 is a monolithic, step-down, switch-mode converter with a built-in power MOSFET. It achieves 0.5A of peak output current over a wide input supply range with excellent load and line regulation.

Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2456 requires a minimal number of readily available, external components and is available in a TSOT23-6 package.

FEATURES

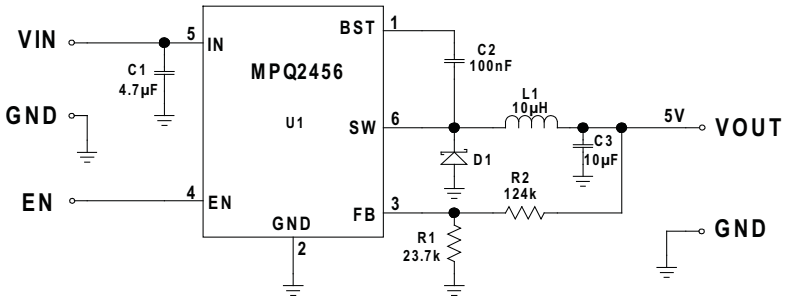
- 0.5A Peak Output Current
- 1Ω Internal Power MOSFET
- Capable of Starting Up with a Large Output Capacitor
- Stable with Low ESR Ceramic Output Capacitors
- Up to 90% Efficiency
- 0.1μA Shutdown Mode
- Fixed 1.2MHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over-Current Protection (OCP)
- Wide 4.5V to 50V Operating Input Range
- Output Adjustable from 0.81V to 0.9 x V_{IN}
- Available in a TSOT23-6 Package

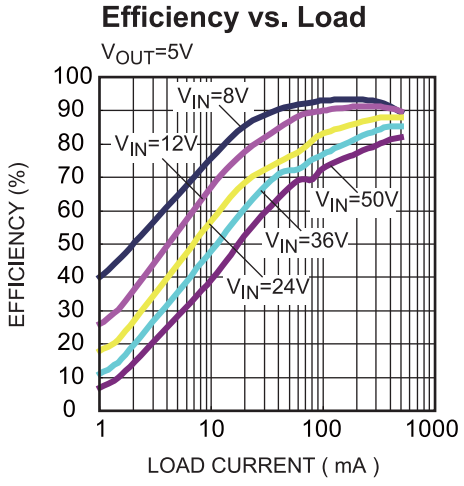
APPLICATIONS

- Power Meters
- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- WLED Drivers

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ2456GJ	TSOT23-6	*See Below*

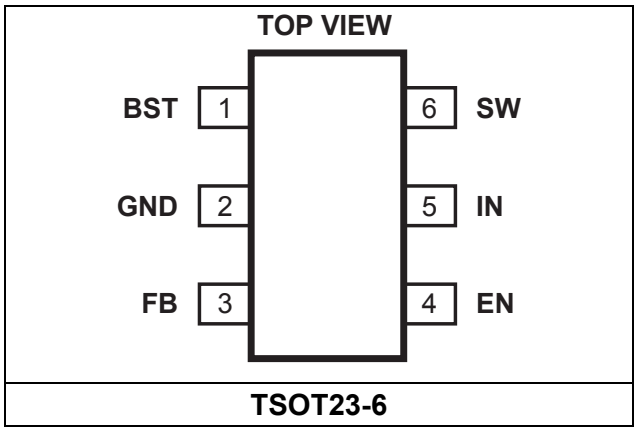
* For Tape & Reel, add suffix –Z (e.g. MPQ2456GJ–Z)

TOP MARKING

| AGVY

AGV: Product code of MPQ2456GJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... …-0.3V to 52V
V_{SW} ..... −0.3V to V_{IN} + 0.3V
V_{BS} ..... V_{SW} + 6V
All other pins .....-0.3V to +6V
EN sink current 100µA
Continuous power dissipation (T_A = +25°C) (2)
TSOT23-6 ..... 0.568W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 50V
Output voltage (V_{OUT}).....0.81V to 0.9 x V_{IN}
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6	220	110 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are T_J = +25°C.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Feedback voltage	V_{FB}		T_J = +25°C	0.792	0.812	0.832	V
			T_J = -40°C to +125°C	0.787		0.837	
Feedback current	I_{FB}	V_{FB} = 0.85V				0.1	µA
Switch-on resistance	$R_{DS(ON)}$				1		Ω
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V				1	µA
Current limit	I_{LIM}		T_J = +25°C	1.0	1.25	1.5	A
			T_J = -40°C to +125°C	0.9		1.7	
Oscillator frequency	f_{SW}	V_{FB} = 0.6V	T_J = +25°C	0.95	1.2	1.45	MHz
			T_J = -40°C to +125°C	0.85		1.45	
Foldback frequency	f_{SW_F}	V_{FB} = 0V			200		kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 0.4V		89	91		%
Minimum on time(5)	τ_{ON}				50		ns
Under-voltage lockout threshold rising	V_{UVLO_R}			2.9	3.3	3.7	V
Under-voltage lockout threshold falling	V_{UVLO_F}			2.65	3.05	3.45	V
Under-voltage lockout threshold hysteresis	V_{UVLO_HYS}				250		mV
EN threshold rising	V_{EN_R}			1.2	1.35	1.5	V
EN threshold falling	V_{EN_F}			1	1.17	1.35	V
EN threshold hysteresis	V_{EN_HYS}				180		mV
EN input current	I_{EN}	V_{EN} = 2V			3.1		µA
		V_{EN} = 0V			0.1		
Supply current (shutdown)	I_S	V_{EN} = 0V			0.1	1.0	µA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V	T_J = +25°C		0.73	0.85	mA
			T_J = -40°C to +125°C			1.0	
Thermal shutdown(5)	T_{SD}				165		°C
Thermal shutdown hysteresis(5)	T_{SD_HYS}				20		°C

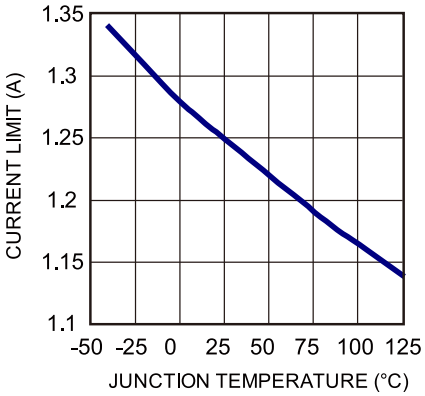
NOTE:
5) Derived from bench characterization. Not tested in production.

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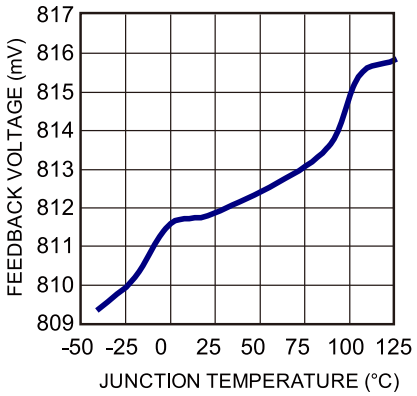
TYPICAL CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

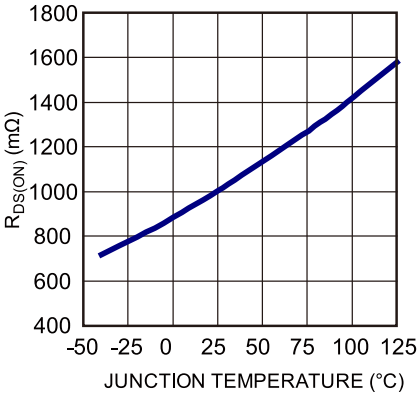
Current Limit vs. T_J



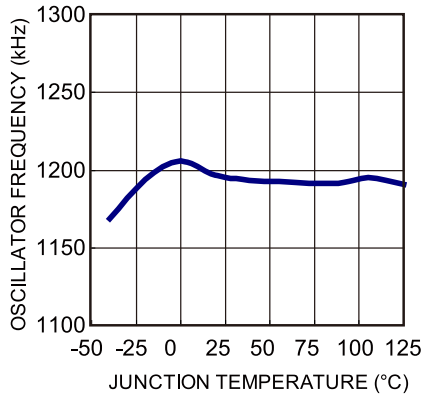
Feedback Voltage vs. T_J



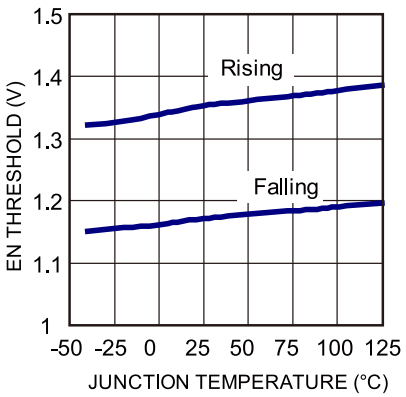
$R_{DS(ON)}$ vs. T_J



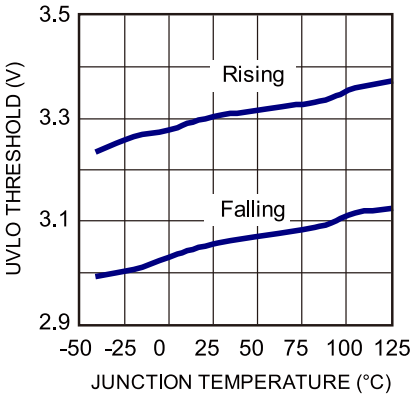
Oscillator Frequency vs. T_J



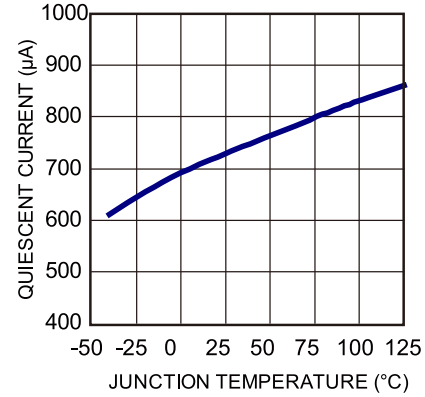
EN Threshold vs. T_J



UVLO Threshold vs. T_J



Quiescent Current vs. T_J

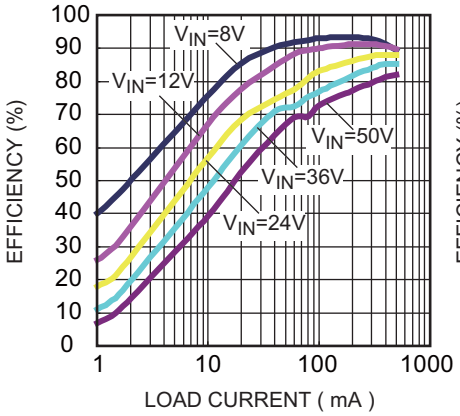


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TYPICAL PERFORMANCE CHARACTERISTICS

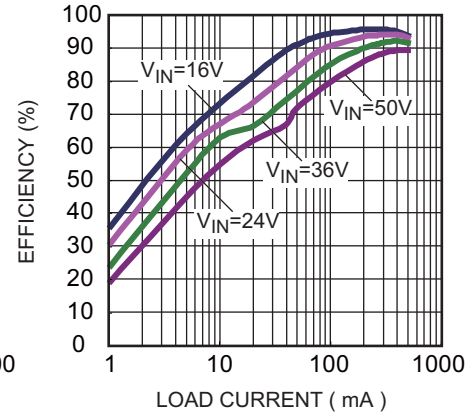
V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load



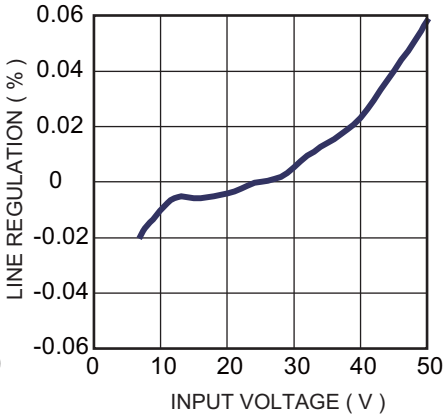
Efficiency vs. Load

V_{OUT}=12V, L=33µH

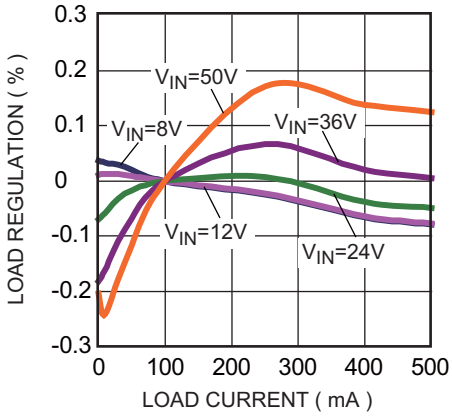


Line Regulation

I_{OUT}=500mA



Load Regulation

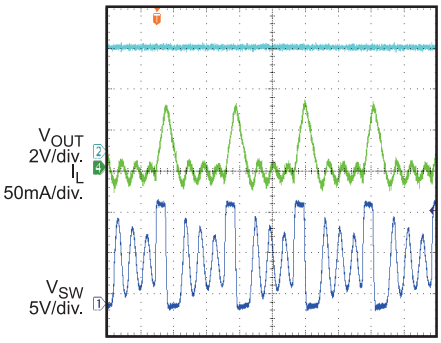


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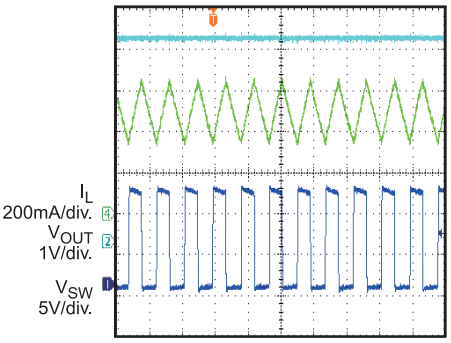
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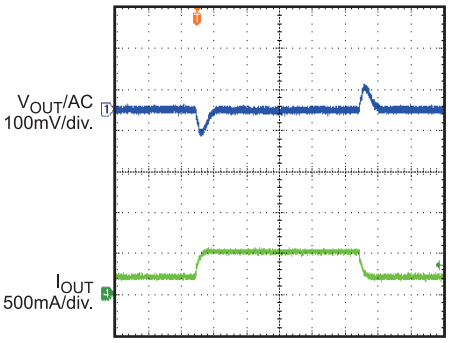
Steady State
I_{OUT}=10mA



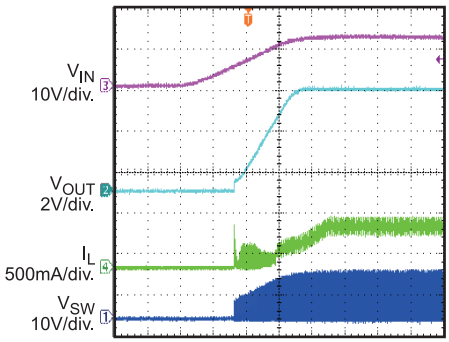
Steady State
I_{OUT}=500mA



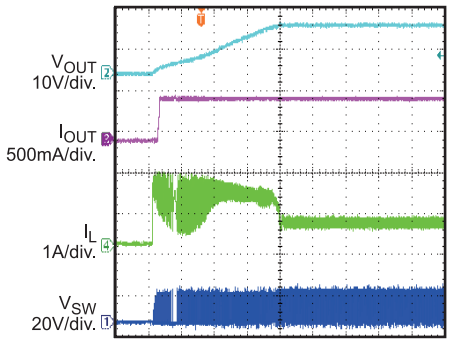
Load Transient
I_{OUT}=200mA<->500mA@1.6A/µs



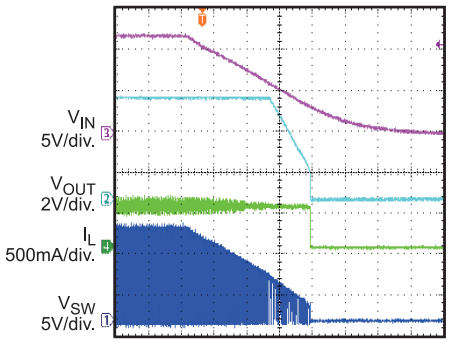
Power On
I_{OUT}=500mA



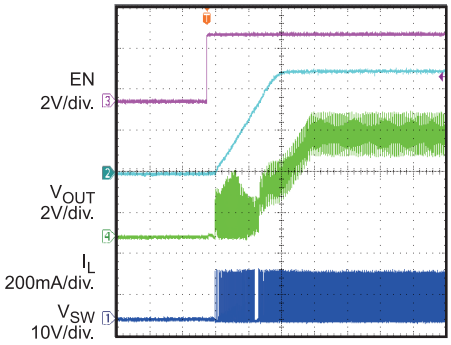
Power On
V_{IN}=16V, V_{OUT}=12V,
C_{OUT}=2200µF, I_{OUT}=500mA



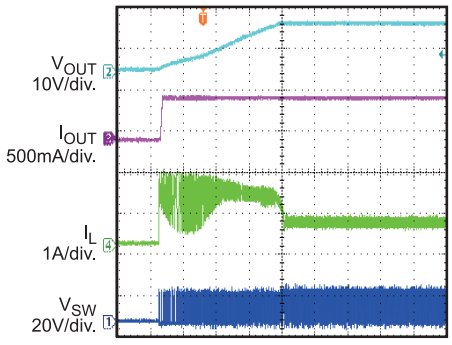
Power Off
I_{OUT}=500mA



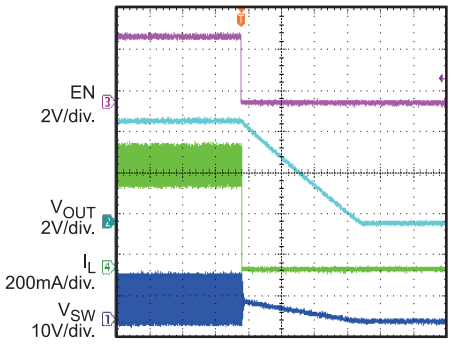
EN On
I_{OUT}=500mA



EN On
V_{IN}=16V, V_{OUT}=12V,
C_{OUT}=2200µF, I_{OUT}=500mA



EN Off
I_{OUT}=500mA

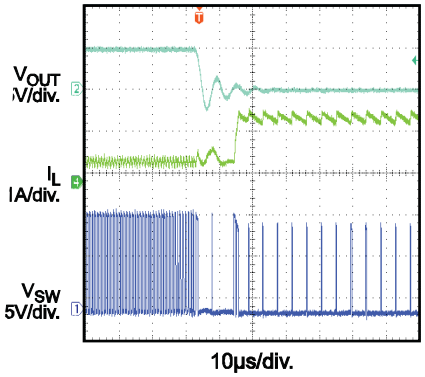


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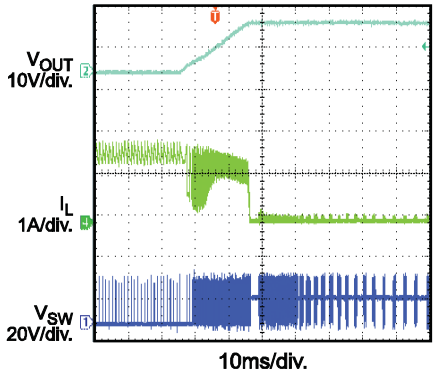
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

Short-Circuit Entry
I_{OUT}=500mA



Short-Circuit Recovery
V_{IN}=16V, V_{OUT}=12V,
C_{OUT}=2200µF, I_{OUT}=500mA



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PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between SW and BS to form a floating supply across the power switch driver. This capacitor drives the power switch's gate above the supply voltage.
2	GND	**Ground.** GND is the voltage reference for the regulated output voltage. GND requires special consideration during layout. Isolate GND from the D1 to C1 ground path to prevent inducing switching current spikes.
3	FB	**Feedback.** FB sets the output voltage. Connect FB to the tap of an external resistor divider from output to GND. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV to prevent current-limit runaway during a short-circuit fault.
4	EN	**On/off.** Pull EN above 1.35V to turn the device on. For automatic enable, connect EN to VIN using a resistor. Ensure that the sink current of EN does not exceed 100μA.
5	IN	**Supply voltage.** The MPQ2456 operates from a 4.5V to 50V unregulated input. Requires C1 to prevent large voltage spikes from appearing at the input.
6	SW	**Switch output.**

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OPERATION

The MPQ2456 is a current mode buck regulator, meaning the EA output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 1.2MHz CLK signal sets the RS flip-flop. Its output turns on M1, connecting SW and the inductor to the input supply.

The increasing inductor current is sensed and amplified by the current sense amplifier. Ramp compensation is summed to the current sense amplifier output and compared to the error amplifier output by the PWM comparator. When the sum of the current sense amplifier output and the slope compensation signal exceed the EA output voltage, the RS flip-flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the current sense amplifier output and the slope compensation signal do not exceed the EA output for an entire cycle, then the falling edge of the CLK resets the flip-flop.

The output of the error amplifier integrates the voltage difference between the feedback and the 0.81V bandgap reference. The polarity is such that a FB voltage lower than 0.81V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases the current delivered to the output.

The MPQ2456 has a 0.6ms internal soft start. The soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuit generates a soft-start voltage (SS) that ramps up with a fixed rising rate. When the SS voltage is below the internal reference (REF), SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, REF regains control.

When there is an extremely large capacitor at the output (e.g. 2200μF or larger), the output voltage rises slower than SS because the current needed to charge up the large output capacitor is higher than the chip's max output current ability. The current limit is kicked during the entire start-up period until V_{OUT} rises to its regulated value.

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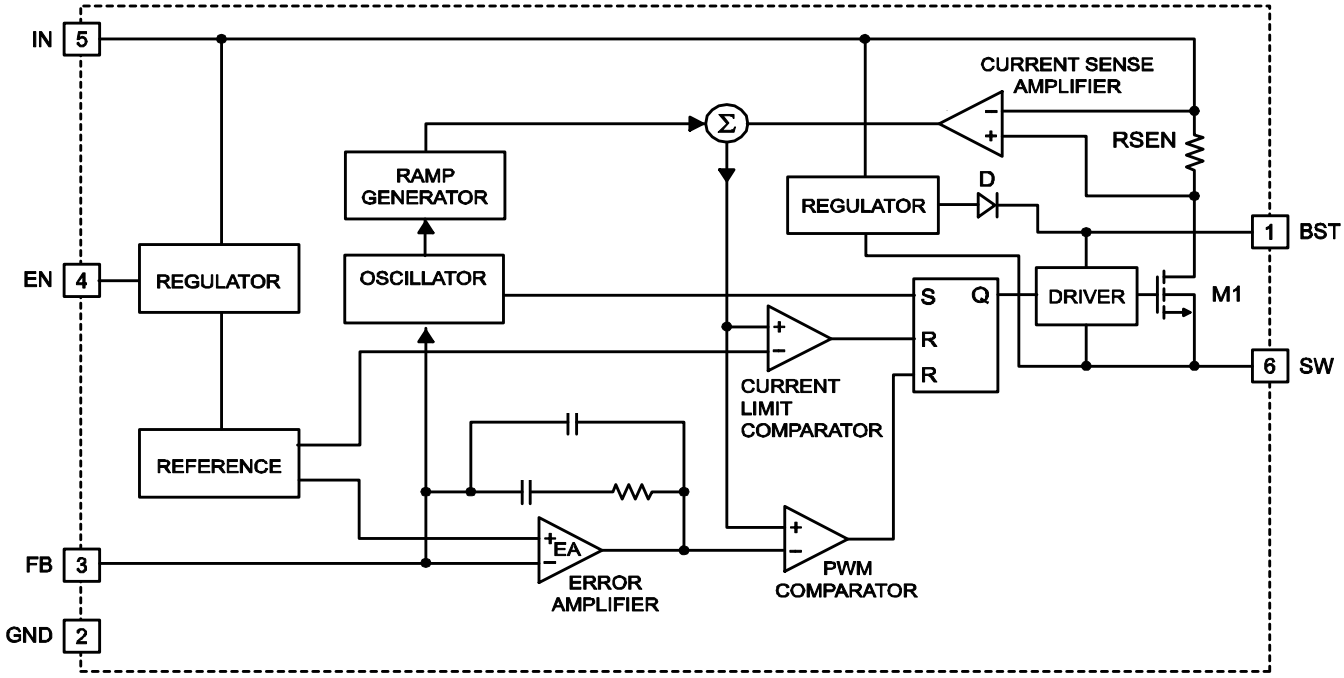


Figure 1: Functional Block Diagram

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic). Table 1 lists resistors for common output voltages. The feedback resistor (R2) sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). R1 can be calculated with Equation (1):

$$R1 = \frac{R2}{\frac{V_{OUT}}{0.812V} - 1} \quad (1)$$

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	102 (1%)	124 (1%)
2.5	59 (1%)	124 (1%)
3.3	40.2 (1%)	124 (1%)
5	23.7 (1%)	124 (1%)
12	8.2 (1%)	113 (1%)

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. For best efficiency, the inductor's DC resistance should be less than 200mΩ. For most designs, the required inductance value can be derived from Equation (2):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions (below 100mA), use a larger inductance to improve efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 22μF ceramic capacitor is sufficient.

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PCB Layout Guide

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 2 and follow the guidelines below.

1) Keep the path of the switching current short and minimize the loop area formed by the input capacitor, high-side MOSFET, and Schottky diode.
2) Keep the connection from the power ground to the Schottky diode to SW as short and wide as possible.
3) Ensure that all feedback connections are short and direct.
4) Place the feedback resistors and compensation components as close to the chip as possible.
5) Route SW away from sensitive analog areas, such as FB.
6) Connect IN, SW, and especially GND to large copper areas to cool the chip for improved thermal performance and long-term reliability. For single layer PCBs, avoid soldering the exposed pad.

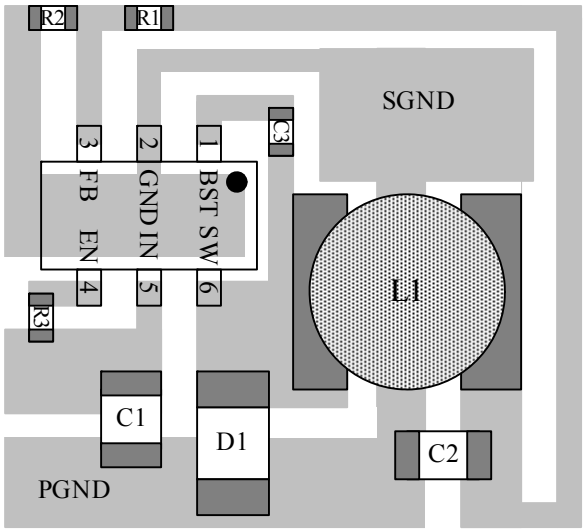


Figure 2: PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance regulator efficiency under the following conditions:

- V_{OUT} = 5V or 3.3V
- High duty cycle: D = $\frac{V_{OUT}}{V_{IN}}$ > 65%

In these cases, add an external BST diode from the output of the voltage regulator to BST (see Figure 3).

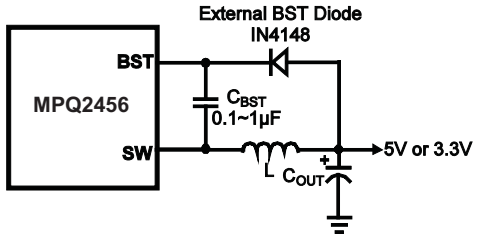


Figure 3: Optional Bootstrap Diode for Enhanced Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor is 0.1μF - 1μF.

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TYPICAL APPLICATION CIRCUIT

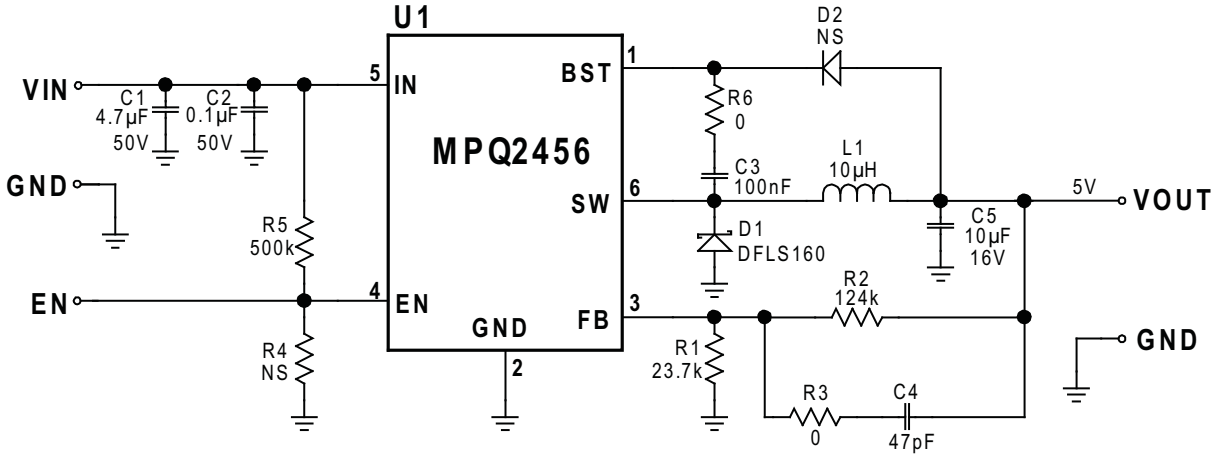


Figure 4: 5V Output Typical Application Circuit

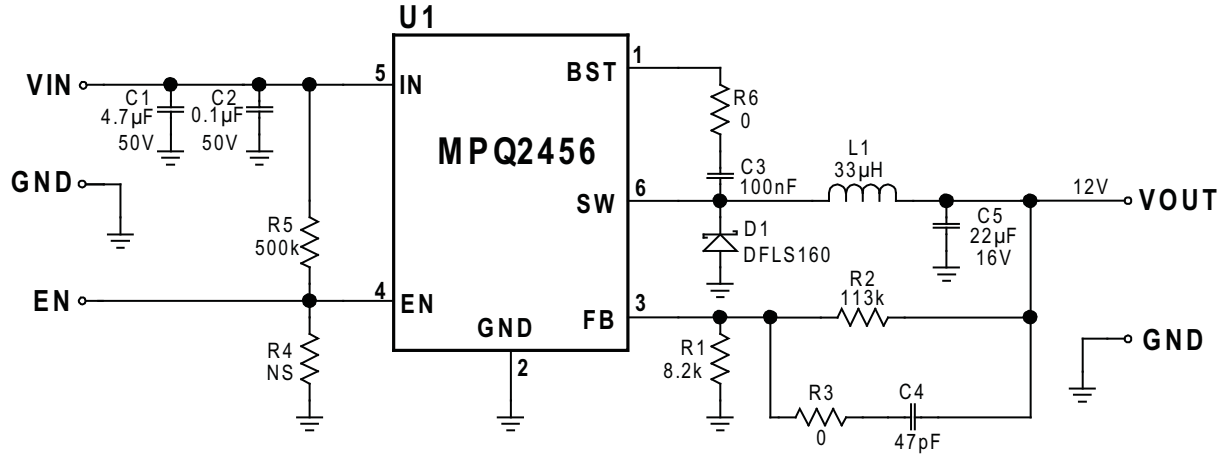
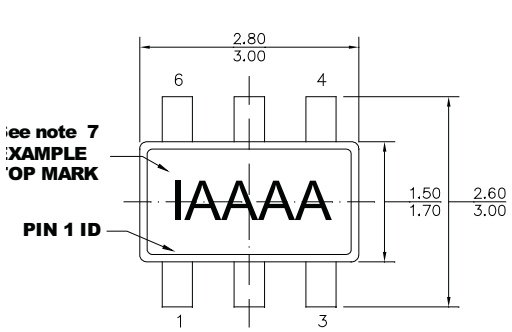


Figure 5: 12V Output Typical Application Circuit

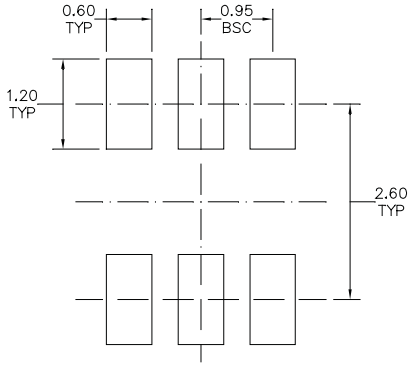
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PACKAGE INFORMATION

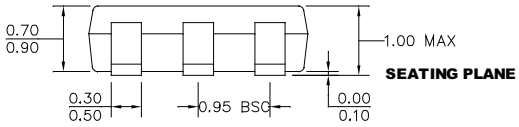
TSOT23-6



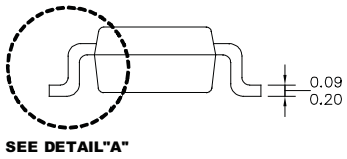
TOP VIEW



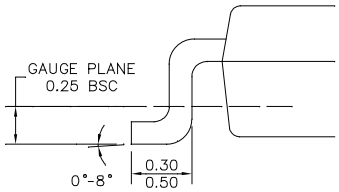
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO193, VARIATION AB.
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK)

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