MPM3606

21V Input, 0.6A Module Synchronous Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology

DESCRIPTION

The MPM3606 is a synchronous rectified, step-down converter module with built-in power MOSFETs, inductor and two capacitors. It offers a very compact solution with only 5 external components to achieve a 0.6A continuous output current with excellent load and line regulation over a wide input supply range. The MPM3606 operates at 2MHz switching frequency, which provides fast load transient response. External AAM pin provides selectable power save mode or forced PWM mode.

Full protection features include over-current protection and thermal shut down.

MPM3606 eliminates design and manufacturing risks while dramatically improving time to market.

The MPM3606 is available in a space-saving QFN-20 (3mmx5mmx1.6mm) package.

FEATURES

- 4.5V-to-21V Operating Input Range
- 0.6A Continuous Load Current
- 200μA Low Quiescent Current
- 100mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Integrated Inductor
- Integrated VCC and Bootstrap Capacitors
- External AAM pin for Power-Save Mode Programming
- OCP Protection with Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in QFN-20 (3mmx5mmx1.6mm) Package
- Total Solution Size 6.7mm x 6.3mm

APPLICATIONS

- Industrial Controls
- Medical and Imaging Equipment
- Telecom and Networking Applications
- LDO Replacement
- Space and Resource-limited Applications

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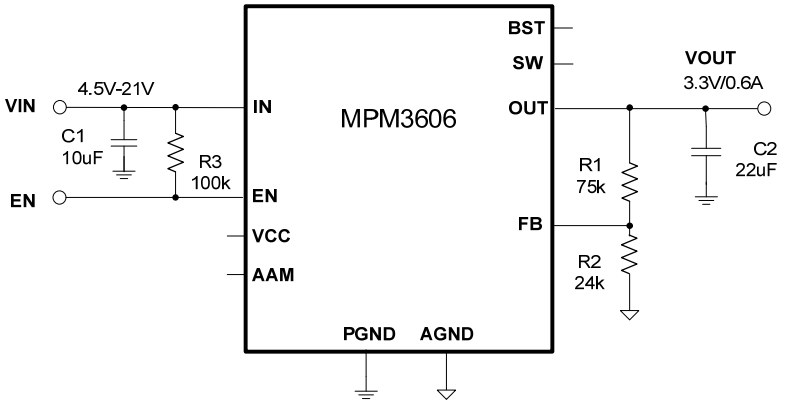
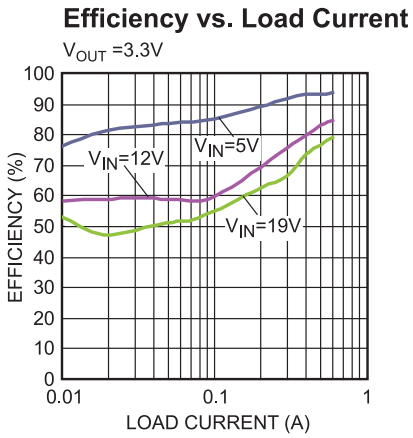
TYPICAL APPLICATION





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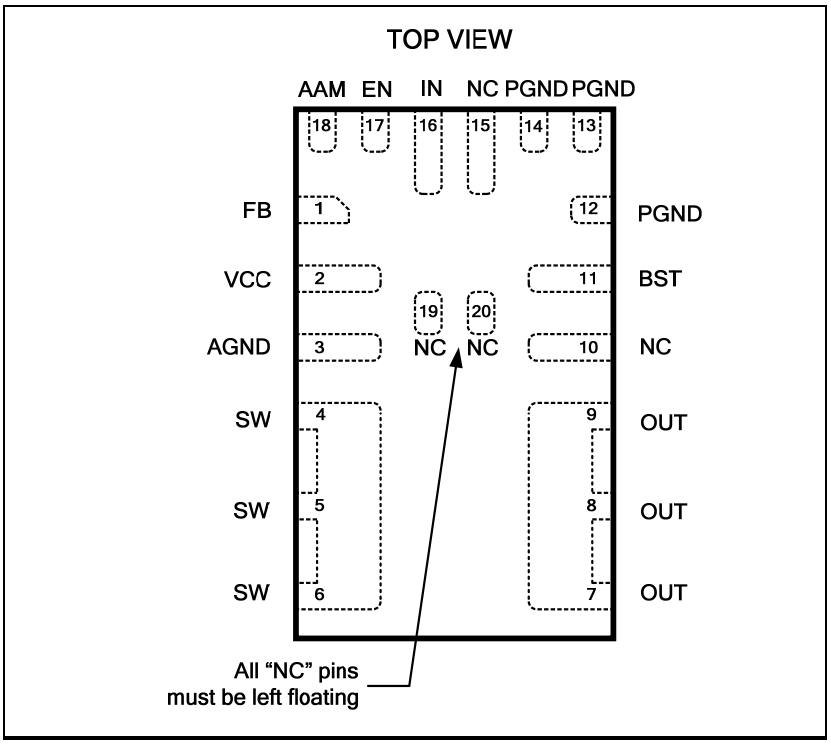
ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3606GQV	QFN-20 (3mmx5mmx1.6mm)	MP3606 M

* For Tape & Reel, add suffix –Z (e.g. MPM3606GQV–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 28V
V_{SW} .....
-0.3V (-5V for <10ns) to 28V (30V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins .....-0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
..... 2.7W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} .....4.5V to 21V
Output Voltage V_{OUT}..... 0.8V to 5.5V(5)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (6)

	θ_{JA}	θ_{JC}
QFN-20 (3mmx5mmx1.6mm)	46	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to page 11, Enable control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) For output voltage setting above 5.5V, please refer to the application information on page 13.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C to +125°C[7], typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V,T_J=25°C			1	μA
Supply Current (Quiescent)	I_q	V_{FB} = 1V, V_{AAM}=0.5V		0.2		mA
		V_{FB} = 1V, V_{AAM}=5V		0.7		
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		100		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		50		mΩ
Inductor DC Resistance	L_{DCR}			60		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit [8]	I_{LIMIT}	Under 40% Duty Cycle	1.8	2.4		A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V, T_J=+25°C	1700	2000	2400	kHz
		V_{FB}=0.75V,T_J=-40°C to +125°C	1500	2000	2500	kHz
Fold-Back Frequency	f_{FB}	V_{FB}<400mV		0.3		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV	80	85		%
Minimum On Time[8]	T_{ON_MIN}			35		ns
Feedback Voltage	V_{FB}	T_J=+25°C	786	798	810	mV
		T_J=-40°C to +125°C	782	798	814	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
AAM Source Current	I_{AAM}	T_J=+25°C	5.6	6.2	6.8	μA
		T_J=-40°C to +125°C	4.3	6.2	7.9	μA
EN Rising Threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN Falling Threshold	$V_{EN_FALLING}$		1.05	1.25	1.45	V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
VIN Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$		3.65	3.9	4.15	V
VIN Under-Voltage Lockout Threshold—Hysteresis	$INUV_{HYS}$			650		mV
VCC Regulator	V_{CC}			4.9		V
VCC Load Regulation		I_{CC}=5mA		1.5		%
Soft-Start Time	t_{SS}	V_{OUT} from 10% to 90%		1.5		ms
Thermal Shutdown [8]				150		°C
Thermal Hysteresis [8]				20		°C

Notes:

7) Not tested in production; guaranteed by over-temperature correlation.
8) Guaranteed by design.

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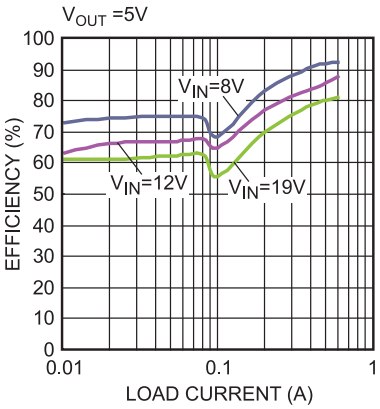
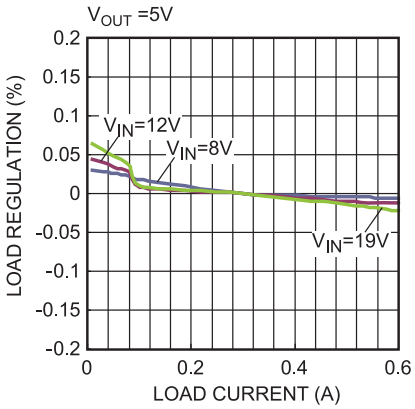
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

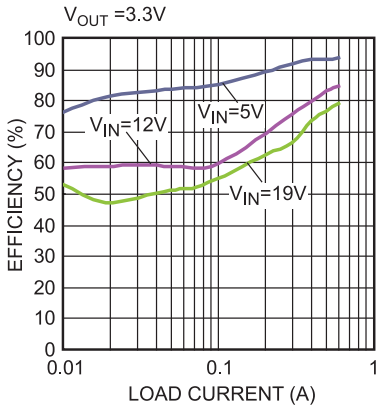
Efficiency vs. Load Current



Load Regulation



Efficiency vs. Load Current



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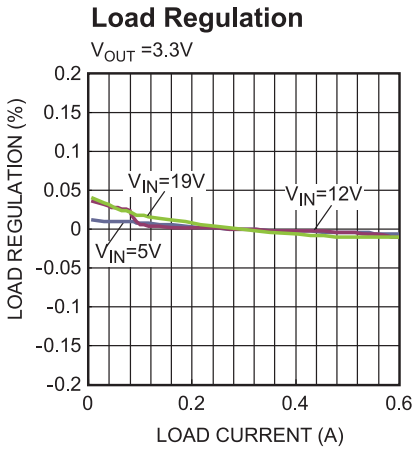
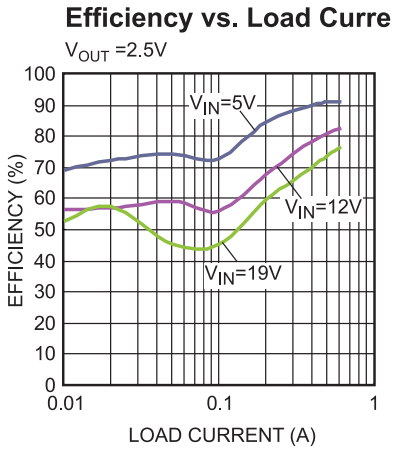


Efficiency vs. Load Current



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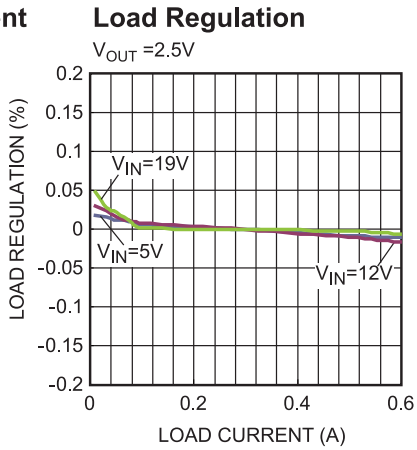
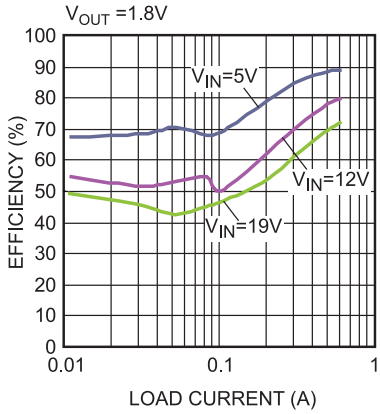


Efficiency vs. Load Current



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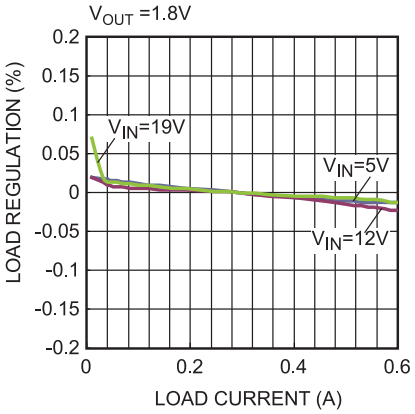
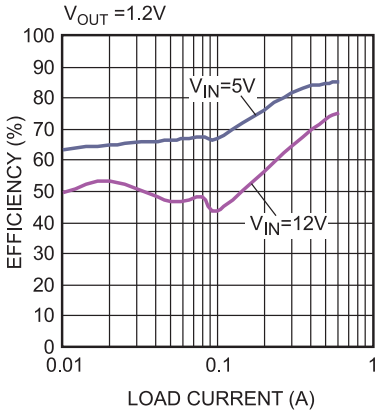


Efficiency vs. Load Current



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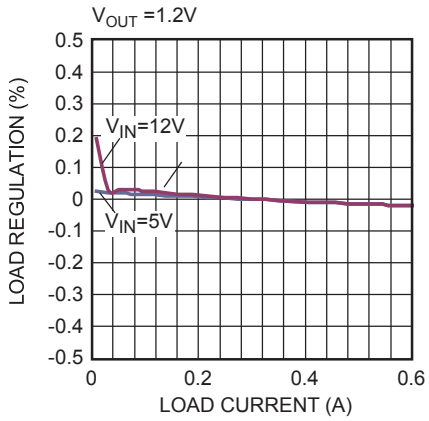
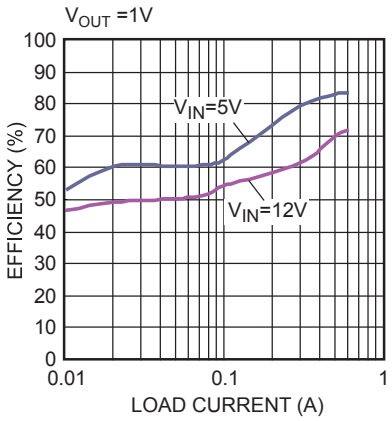
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Load Regulation



Efficiency vs. Load Current



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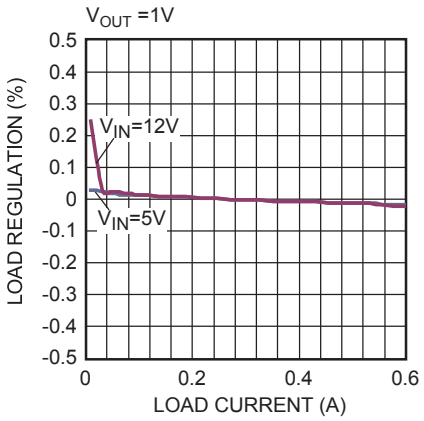
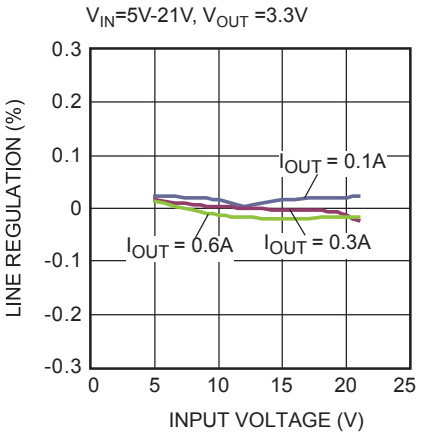
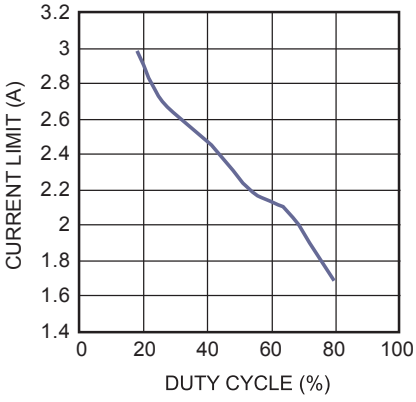


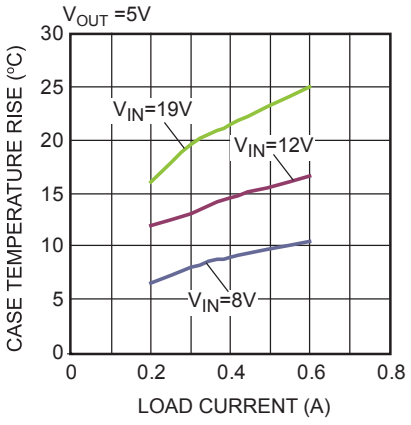
Line Regulation



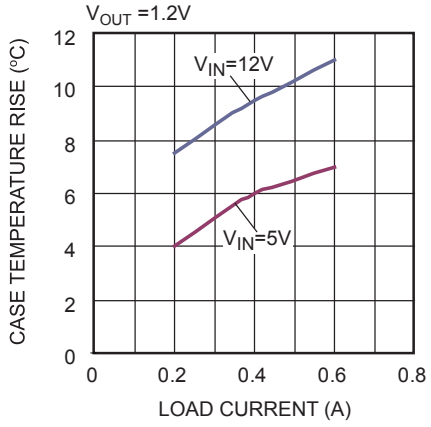
Current Limit vs. Duty Cycle



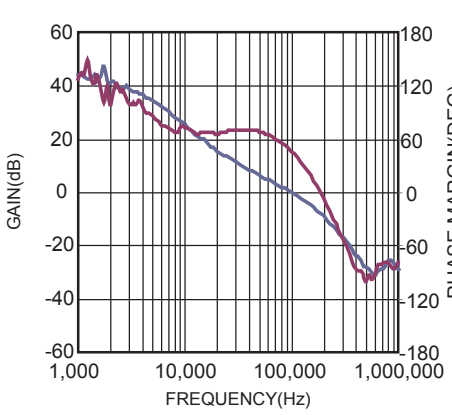
Case Temperature Rise vs. Output Current



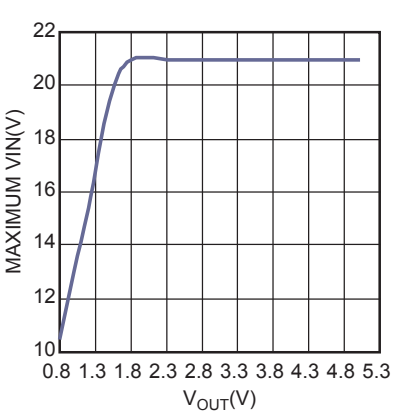
Case Temperature Rise vs. Output Current



Bode Plot



Maximum VIN vs. VOUT



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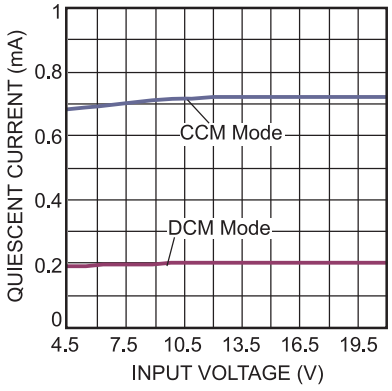
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

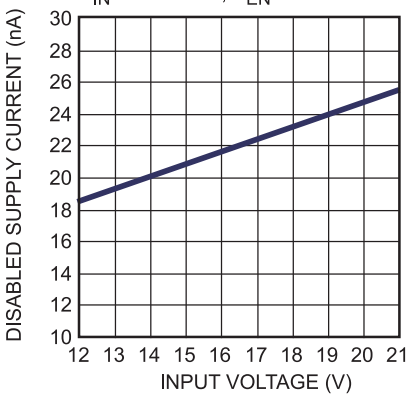
Quiescent Current vs. Input Voltage

V_{IN}=4.5V to 21V, V_{FB}=1V



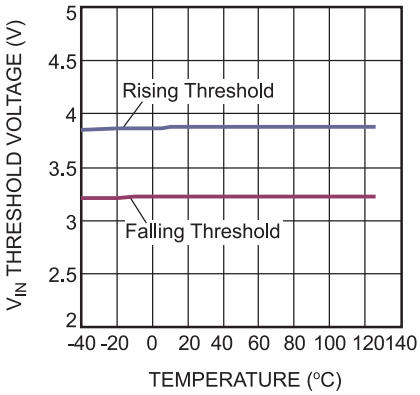
Disabled Supply Current vs. Input Voltage

V_{IN}=12V to 21V, V_{EN}=0V



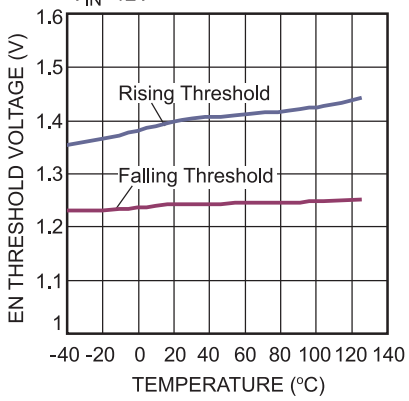
V_{IN} Threshold vs. Temperature

V_{EN}=5V

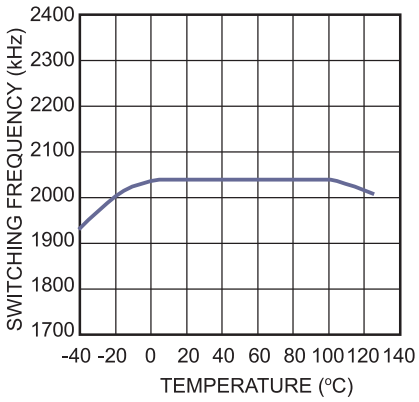


EN Threshold vs. Temperature

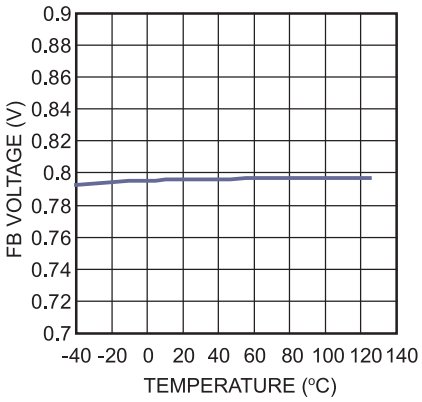
V_{IN}=12V



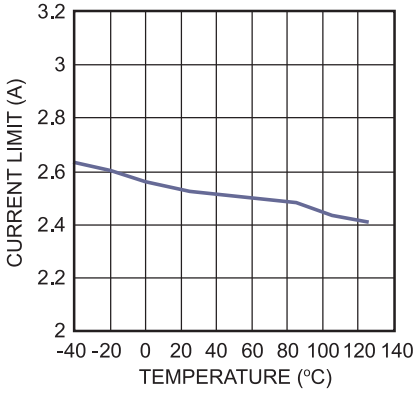
Switching Frequency vs. Temperature



FB Voltage vs. Temperature

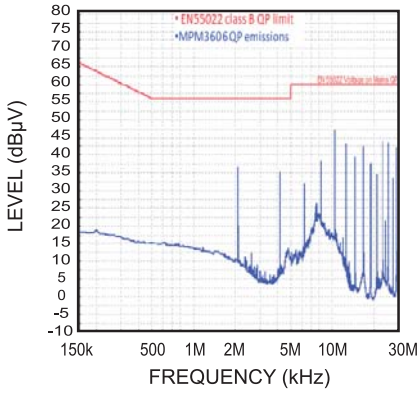


Current Limit vs. Temperature



Conduction-EMI

I_{OUT}=0.6A



Radiation-EMI

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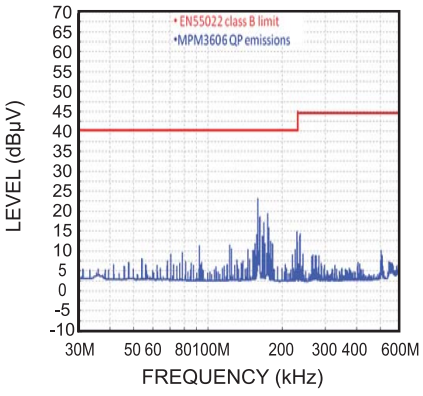

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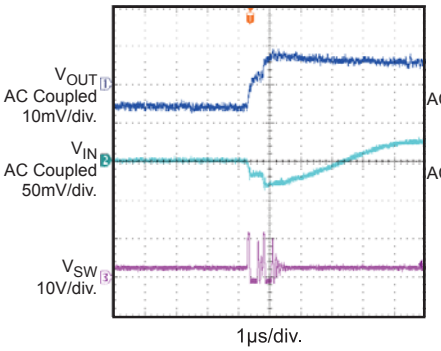
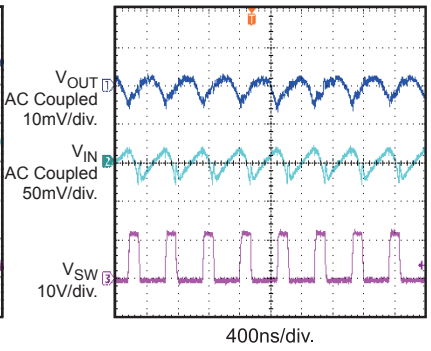
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

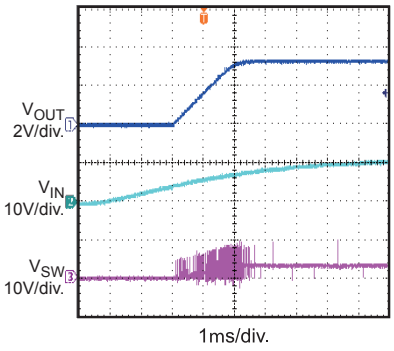
Input/Output Ripple
I_{OUT} = 0A



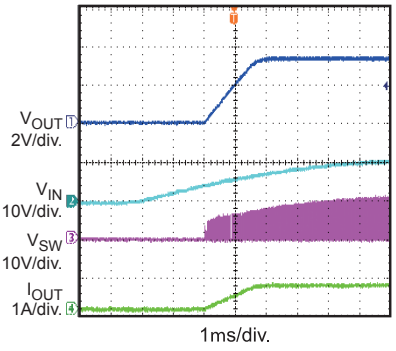
Input/Output Ripple
I_{OUT} = 0.6A



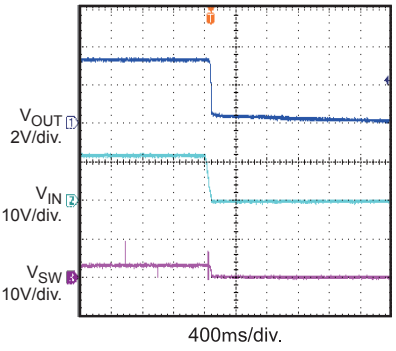
VIN Startup
I_{OUT} = 0A



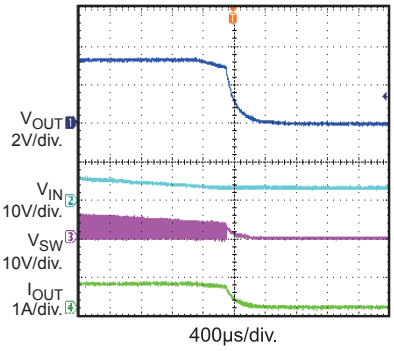
VIN Startup
I_{OUT} = 0.6A



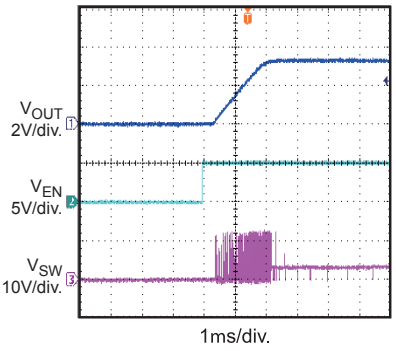
VIN Shutdown
I_{OUT} = 0A



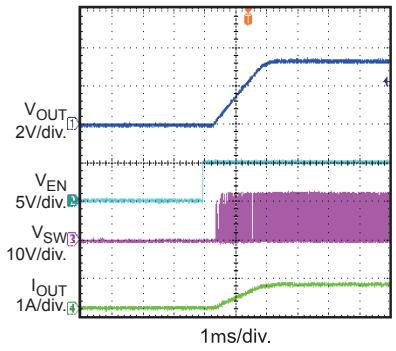
VIN Shutdown
I_{OUT} = 0.6A



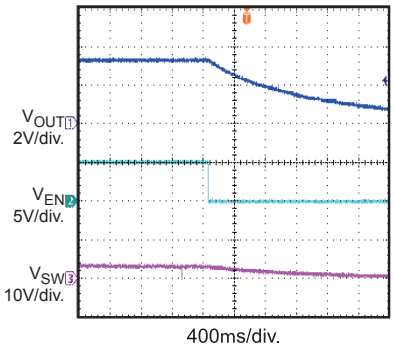
EN Startup
I_{OUT} = 0A



EN Startup
I_{OUT} = 0.6A



EN Shutdown
I_{OUT} = 0A



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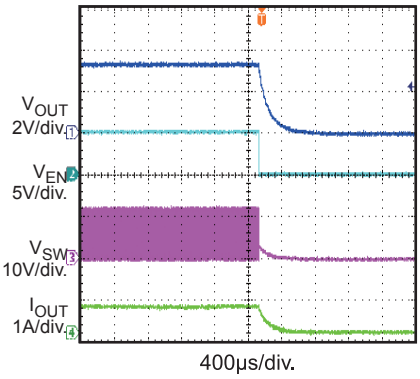
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

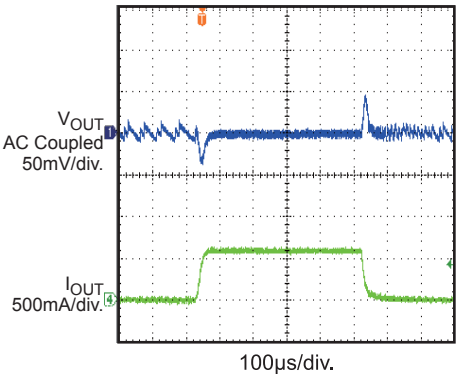
EN Shutdown

I_{OUT} = 0.6A

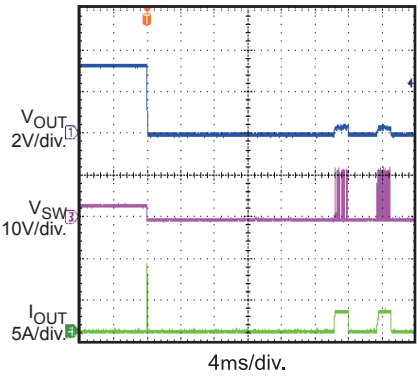


Transient Response

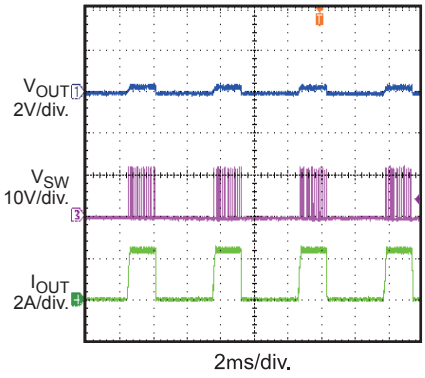
I_{OUT} = 0A to 0.6A



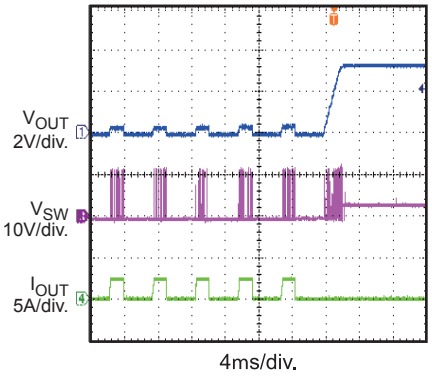
Short Circuit Entry



Short Circuit Steady State



Short Circuit Recovery



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PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	Feedback. Connect to the tap of an external resistor divider from the output to AGND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short circuit fault. Place the resistor divider as close to the FB pin as possible. Avoid placing vias on the FB traces.
2	VCC	Internal 5V LDO output. Internal circuit integrates LDO output capacitor, so there is no need to add external capacitor.
3	AGND	Analog Ground. Reference ground of logic circuit. AGND is internally connected to PGND. No need add external connections to PGND.
4, 5, 6	SW	Switch Output. Large copper plane is recommended on pin 4, 5 and 6 for better heat sink.
7, 8, 9	OUT	Power Output. Connect load to this pin. Output capacitor is needed.
10, 15, 19, 20	NC	DO NOT CONNECT. Pin must be left floating.
11	BST	Bootstrap. Bootstrap capacitor is integrated internally. External connection is not needed.
12, 13, 14	PGND	Power Ground. Reference ground of the power device. PCB layout requires extra care. For best results, connect to PGND with copper and vias.
16	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MPM3606 operates from a +4.5V to +21V input rail. Requires a low-ESR, and low-inductance capacitor to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
17	EN	EN=high to enable the module. Float EN pin or connect it to ground will disable the converter.
18	AAM	Advanced Asynchronous Modulation. AAM pin sources a 6.2μA current from internal 5V supply. Float AAM pin or drive AAM pin high (>2.5V) to force the MPM3606 to always operate in CCM. Connect a resistor to ground to program AAM voltage in the range of 0 to1V if non-synchronous mode is required under light load.

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FUNCTIONAL BLOCK DIAGRAM

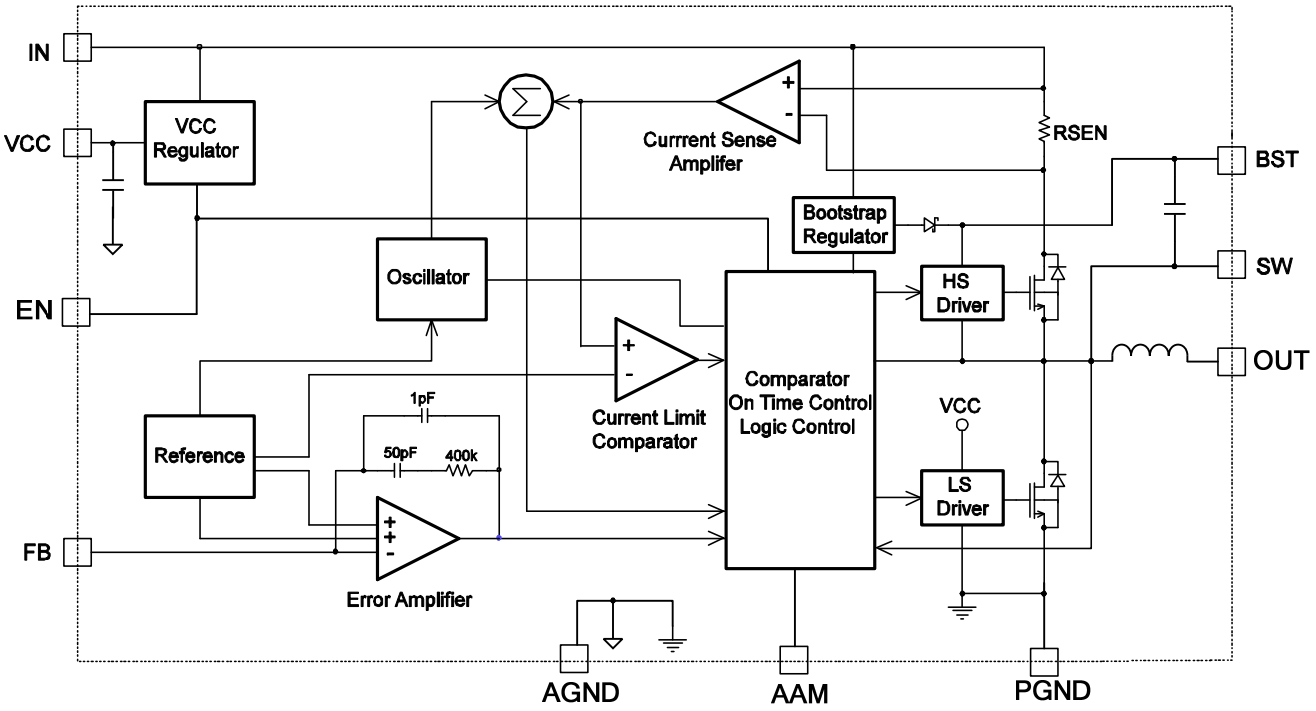

Figure 1: Functional Block Diagram

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OPERATION

The MPM3606 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, integrated inductor and two capacitors. It offers a very compact solution that achieves a 0.6A continuous output current with excellent load and line regulation over 4.5V to 21V input supply range.

The MPM3606 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until the current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, within 80% of one PWM period, the current in the power MOSFET does not reach the value set by the COMP value, the power MOSFET is forced off.

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. When V_{IN} is less than 5.0V, the output decreases, and the part integrates internal decoupling capacitor. No need add external VCC output capacitor.

AAM Operation

The MPM3606 has AAM (Advanced Asynchronous Modulation) power-save mode for light load. Connect a resistor from AAM pin to GND to set AAM voltage. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} is higher than V_{AAM}.

Under the light load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, thus the MPM3606 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

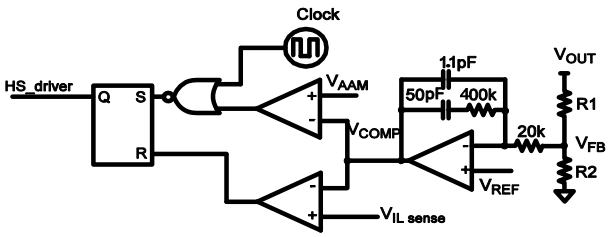

Figure 2: Simplified AAM Control Logic

Error Amplifier

The error amplifier compares the FB pin voltage to the internal 0.8V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. The MPM3606 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.9V while its falling threshold is 3.25V.

Enable Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 3. Connecting the EN input pin through a pullup resistor to the voltage on the V_{IN} pin limits the EN input current to less than 100μA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V – 6.5V) \div 100\mu A = 55k\Omega$.

Connecting the EN pin is directly to a voltage source without any pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

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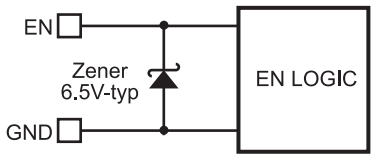

Figure 3: 6.5V Zener Diode Connection

Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.5ms.

Over-Current-Protection and Hiccup

The MPM3606 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until V_{FB} is below the Under-Voltage (UV) threshold—typically 50% below the reference. Once UV is triggered, the MPM3606 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground, and greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator. The MPM3606 exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 150°C, it shuts down the whole chip. When the temperature drops below its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (Figure 4). If (V_{IN}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4.

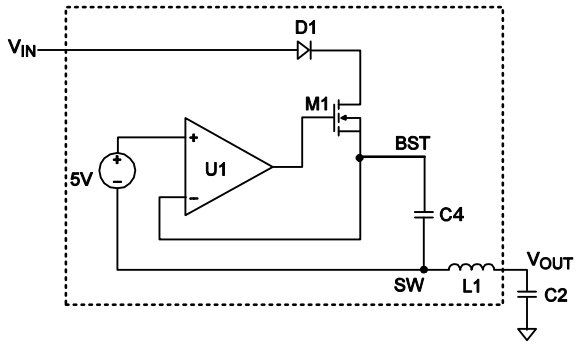

Figure 4: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and EN exceed their thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{IN} low, EN low and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 refer to Table 1, R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.798V} - 1}$$

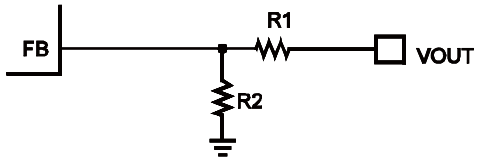

Figure 5: Feedback Network

Table 1 lists the recommended resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_{AAM}(kΩ)(9)
1.0	221	887	9.09
1.2	191	383	11.3
1.5	158	180	13
1.8	102	82	18.2
2.5	75	34.8	25.5
3.3	75	24	33
5	100	19.1	45.3

Notes:

9) The recommended R_{AAM} value is based on 12V input voltage, please refer to Figure 7 for full input and output voltage range's R_{AAM} value.

Normally output voltage is recommended to be set from 0.8V to 5.5V. Actually it can be set larger than 5.5V. Output voltage ripple will be larger in this case. Additional output capacitor may be needed to reduce the output voltage ripple.

When output voltage is high, the chip's heat dissipation become more important, please refer to PC Board layout guidelines on page 14-15 to achieve better thermal effect.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 10μF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Setting the AAM Voltage

The AAM voltage is used to set the transition point from AAM to CCM. It should be chosen to provide the best combination of efficiency, stability, ripple, and transient.

If the AAM voltage is set lower, then stability and ripple improves, but efficiency during AAM mode and transient degrades. Likewise, if the AAM voltage is set higher, then the efficiency during AAM and transient improves, but stability

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and ripple degrades. So the optimal balance point of AAM voltage for good efficiency, stability, ripple and transient should be found out.

Adjust the AAM threshold by connecting a resistor from AAM pin to ground. Take Figure 6 as reference. An internal 6.2μA current source charges the external resistor.

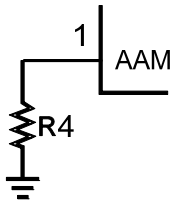

Figure 6: AAM Network

Generally, R4 is then given by:

$$V_{AAM}=R4 \times 6.2\mu A$$

Please consult the Figure 7 below when setting the AAM resistor.

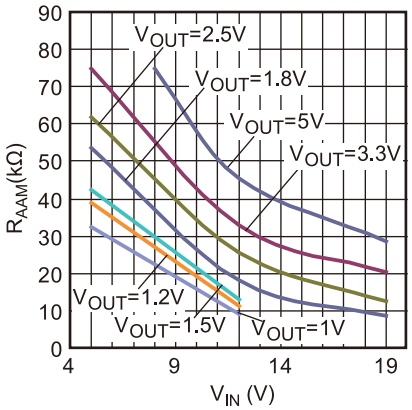

Figure 7: AAM Resistor Selection

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_S \times L_1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_S^{\,2}\times L_1\times C2}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_S \times L_1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3606 can be optimized for a wide range of capacitance and ESR values.

PC Board Layout [10]

PCB layout is very important to achieve stable operation especially for input capacitor placement. For best results, follow these guidelines:

1. Use large ground plane directly connect to PGND pin. Add vias near the PGND pin if bottom layer is ground plane.
2. The high current paths at GND, IN. Place the ceramic input capacitor close to IN and PGND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.
3. The external feedback resistors should be placed next to the FB pin.
4. Keep the feedback network away from the switching node.

Notes:

10) The recommended layout is based on the Figure 8 Typical Application circuit on page 16.

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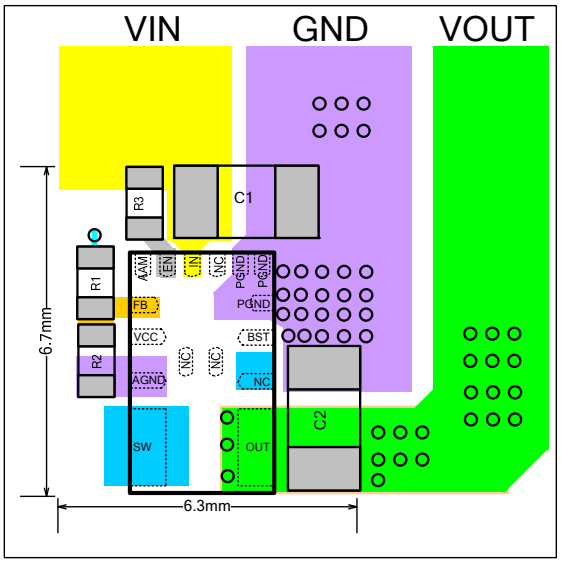
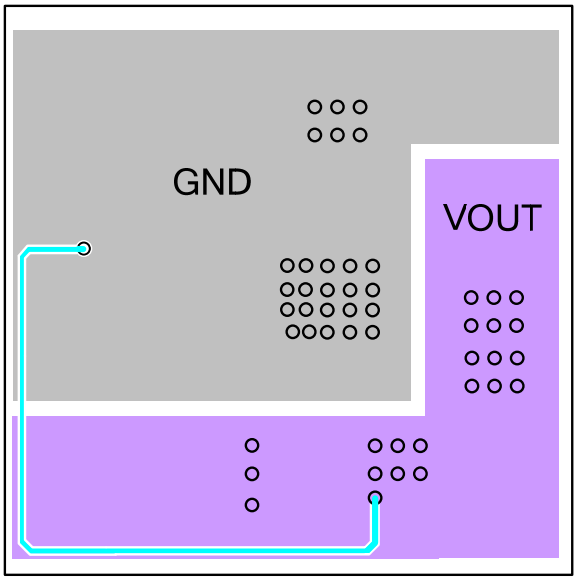


Top Layer



Bottom Layer

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	0.6A

The detailed application schematic is shown in Figure 8 through 13. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

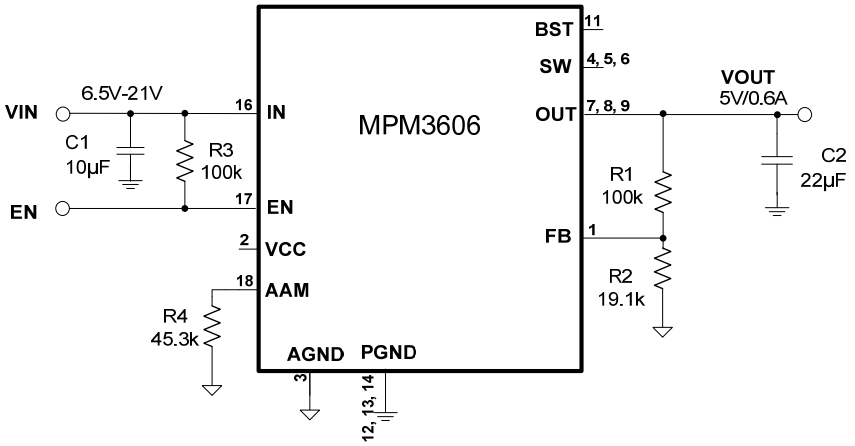

Figure 8: V_{OUT}=5V, I_{OUT}=0.6A

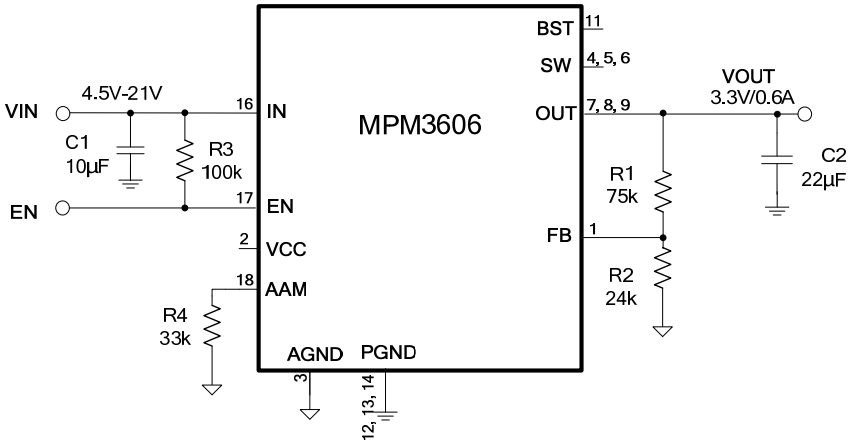

Figure 9: V_{OUT}=3.3V, I_{OUT}=0.6A

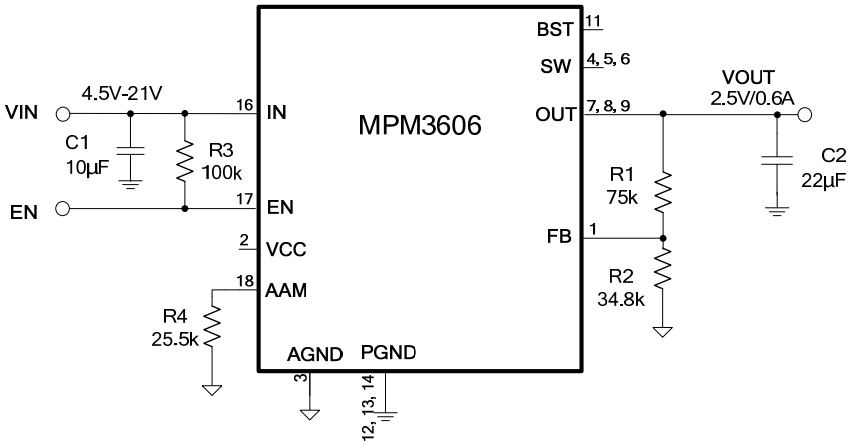

Figure 10: V_{OUT}=2.5V, I_{OUT}=0.6A

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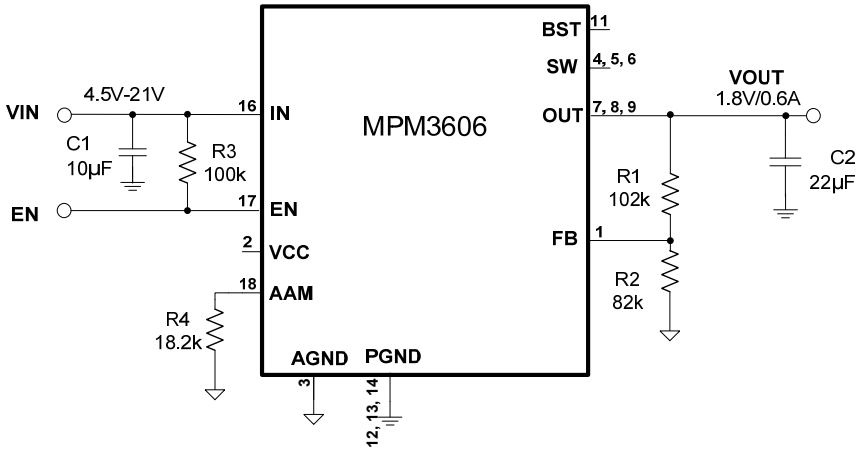

Figure 11: V_{OUT}=1.8V, I_{OUT}=0.6A

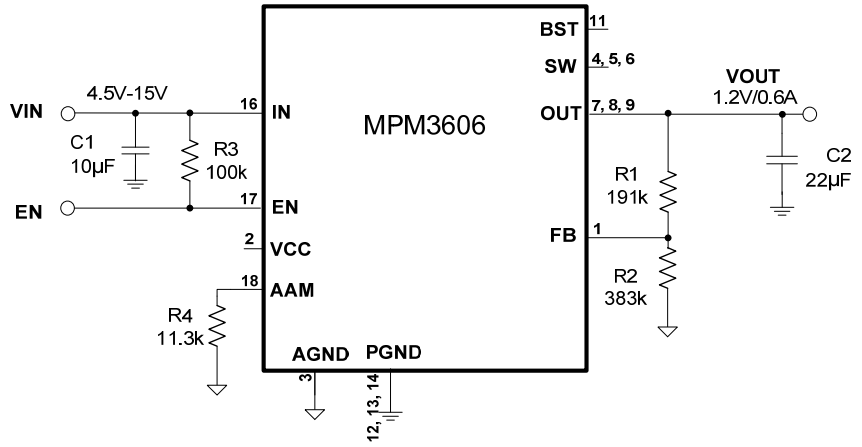

Figure 12: V_{OUT}=1.2V, I_{OUT}=0.6A

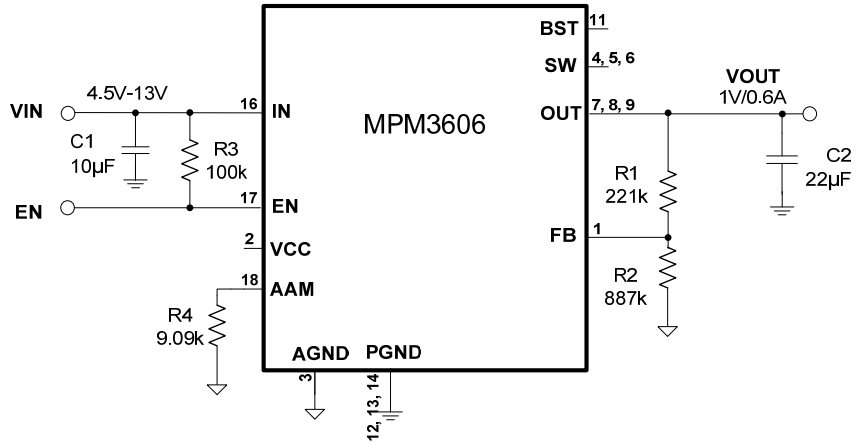

Figure 13: V_{OUT}=1V, I_{OUT}=0.6A

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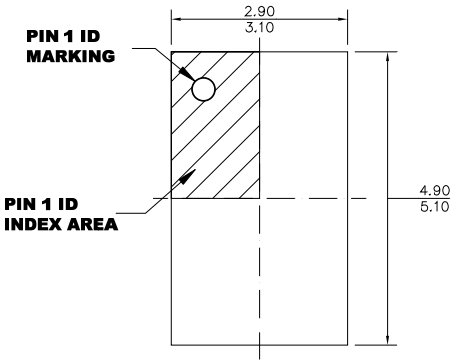
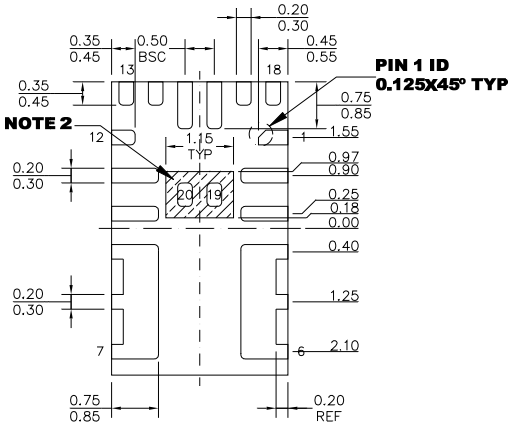
PACKAGE INFORMATION

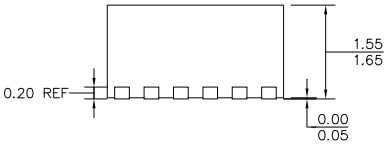
QFN-20 (3mmx5mmx1.6mm)



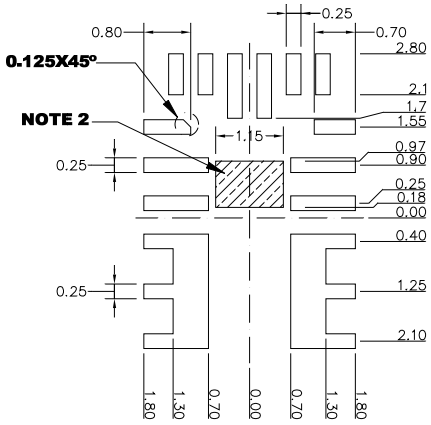
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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