3.3 V 1:6 LVCMOS PLL Clock Generator

MPC9331

**LOW VOLTAGE
3.3 V LVCMOS 1:6
CLOCK GENERATOR**



**FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03**



**AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03**

The MPC9331 is a 3.3 V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking, and computing applications. With output frequencies up to 240 MHz and output skews less than 150 ps, the device meets the needs of most the demanding clock applications. The MPC9331 is specified for the temperature range of 0°C to +70°C.

Features

- 1:6 PLL based low-voltage clock generator
- 3.3 V power supply
- Generates clock signals up to 240 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- Supports zero-delay operation in external feedback mode
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free Package Available
- Ambient temperature range 0°C to +70°C
- Internal Power-Up Reset
- Pin and function compatible to the MPC931

Functional Description

The MPC9331 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9331 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4, and divide-by-6), the internal VCO of the MPC9331 is running at either 2x, 4x, 6x, 8x, or 12x of the reference clock frequency. In internal feedback configuration (divide-by-8) the internal VCO is running 8x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB, and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4.

The REF_SEL pin selects the differential LVPECL or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) by deasserting the OE/$\overline{\text{MR}}$ pin. In the PLL configuration with external feedback selected, deasserting OE/$\overline{\text{MR}}$ causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/$\overline{\text{MR}}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9331 output clock stop control allows the outputs to start and stop synchronously in logic low state, without the potential generation of runt pulses.

The MPC9331 is fully 3.3 V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9331 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

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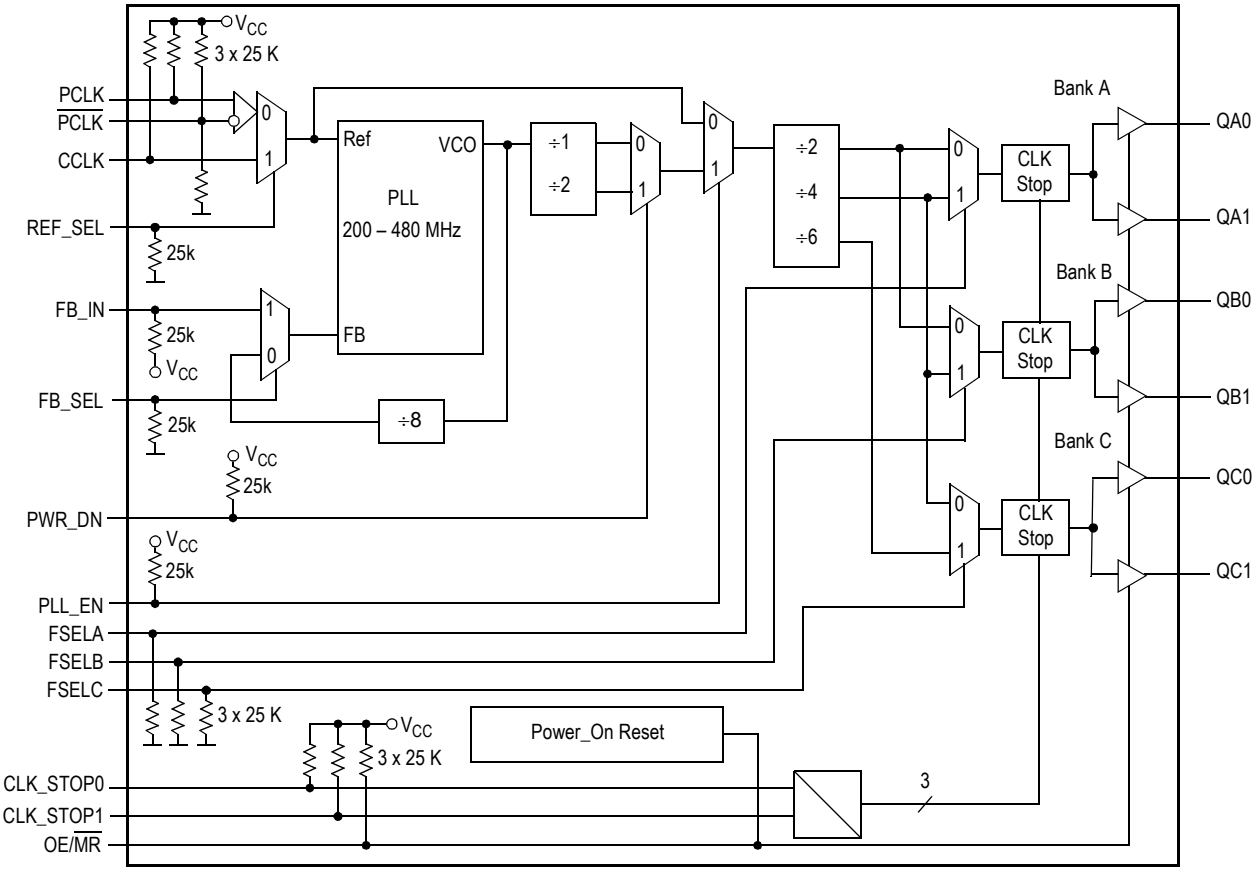
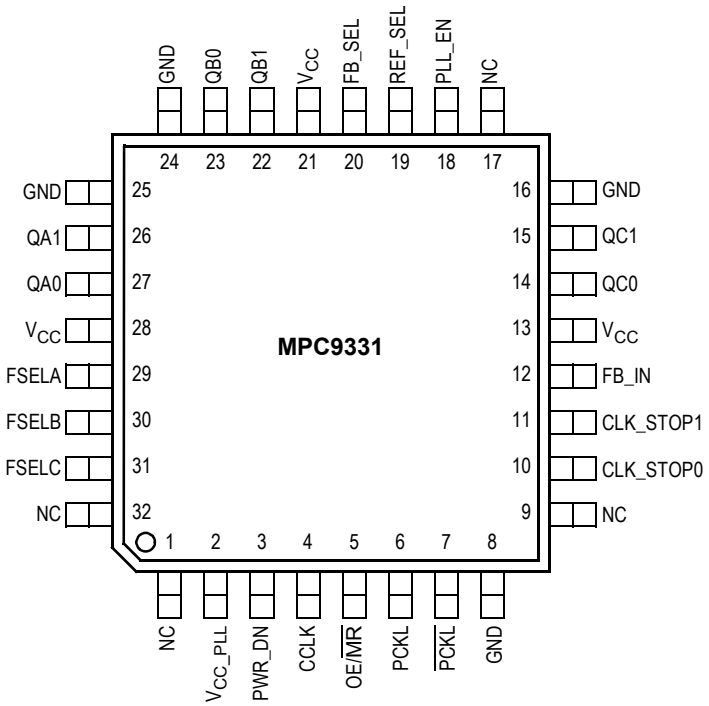


Figure 1. MPC9331 Logic Diagram



It is recommended to use an external RC filter for the analog V_{CC_PLL} power supply pin. Please see application section for details.

Figure 2. MPC9331 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
PCLK, $\overline{PCLK}$	Input	LVPECL	Differential PECL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
FB_SEL	Input	LVCMOS	Feedback select
REF_SEL	Input	LVCMOS	Reference clock select
PWR_DN	Input	LVCMOS	Output frequency and power down select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVCMOS	PLL enable/disable
CLK_STOP0-1	Input	LVCMOS	Clock output enable/disable
OE/$\overline{MR}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0-1, QB0-1, QC0-1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use external RC filter for the analog power supply pin $V_{CC_PLL.}$ Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	PCLK is the PLL reference clock	CCLK is the PLL reference clock
FB_SEL	1	Internal PLL feedback of 8. $f_{VCO} = 8 * f_{ref}$	External feedback. Zero-delay operation enabled for CCLK or PCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9331 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
PWR_DN	1	VCO ÷ 1 (High output frequency range)	VCO ÷ 2 (Low output frequency range)
FSELA	0	Output divider ÷ 2	Output divider ÷ 4
FSELB	0	Output divider ÷ 2	Output divider ÷ 4
FSELC	0	Output divider ÷ 4	Output divider ÷ 6
OE/$\overline{MR}$	1	Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9331 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK or PCLK). Reset does not affect PLL lock in internal feedback configuration.	Outputs enabled (active)
CLK_STOP[0:1]	11	See Table 3	

PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 8 through Table 10 for supported frequency ranges and output to input frequency ratios.

Table 3. Clock Output Synchronous Disable (CLK_STOP) Function Table(1)

CLK_STOP0	CLK_STOP1	QA[0:1]	QB[0:1]	QC[0:1]
0	0	Active	Stopped in logic L state	Stopped in logic L state
0	1	Active	Stopped in logic L state	Active
1	0	Stopped in logic L state	Stopped in logic L state	Active
1	1	Active	Active	Active

1. Output operation for OE/$\overline{MR}$=1 (outputs enabled). OE/$\overline{MR}$=0 will disable (high-impedance state) all outputs independent on CLK_STOP[0:1].

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}(1)	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA(2)
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output impedance			14 – 17		Ω	
I_{IN}	Input Current(3)				±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			8.0	12	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current(4)				26	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9331 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
3. Inputs have pull-down or pull-up resistors affecting the input current.
4. OE/$\overline{MR}$=0 (outputs in high-impedance state).

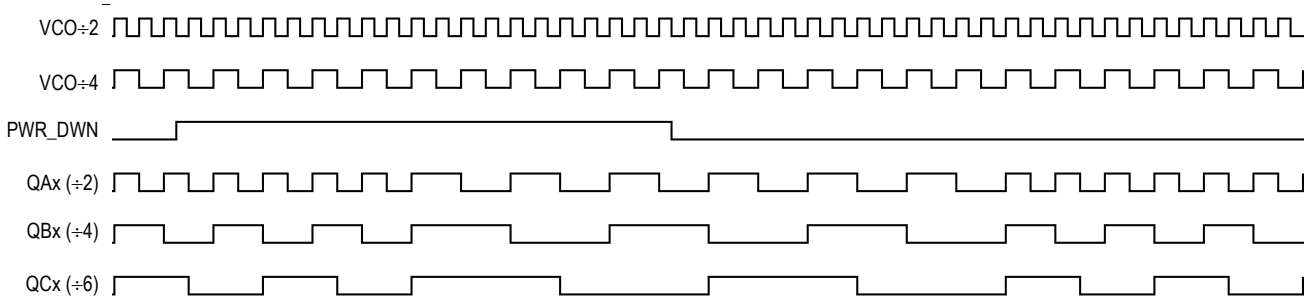
Table 7. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency	÷2 feedback	100.0		240.0	MHz	PLL locked
	PLL mode, external feedback	÷4 feedback	50.0		120.0	MHz	
		÷6 feedback	33.3		80.0	MHz	
		÷8 feedback	25.0		60.0	MHz	
		÷12 feedback	16.67		40.0	MHz	
	PLL mode, internal feedback	(÷8 feedback)	25.0		60.0	MHz	
	Input reference frequency in PLL bypass mode[2]				240	MHz	
f_{VCO}	VCO lock frequency range[3]		200		480	MHz	
f_{MAX}	Output Frequency	÷2 output	100.0		240.0	MHz	PLL locked
		÷4 output	50.0		120.0	MHz	
		÷6 output	33.3		80.0	MHz	
		÷8 output	25.0		60.0	MHz	
		÷12 output	16.67		40.0	MHz	
V_{PP}	Peak-to-peak input voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[4]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC} – 0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[5]		2.0			ns	
t_R, t_F	CCLK Input Rise/Fall Time[6]				1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay	CCLK to FB_IN[7]	–250	–130	–50	ps	FB_SEL = 1
	(static phase offset)	PCLK to FB_IN[7]	–180	–30	+120	ps	and PLL locked
		CCLK or PCLK to FB_IN[8]	–3.0		+3.0	°	
$t_{sk(O)}$	Output-to-output Skew				150	ps	
DC	Output duty cycle[9]		(T÷2)–500	T÷2	(T÷2)+500	ps	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				8.0	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter[10]				200	ps	
$t_{JIT(PER)}$	Period Jitter				125	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1 σ)			25	ps	
BW	PLL closed loop bandwidth[11]	÷ 4 feedback		2.0–8.0		MHz	
	PLL mode, external feedback	÷ 6 feedback		1.2–4.0		MHz	
		÷ 8 feedback		1.0–3.0		MHz	
		÷12 feedback		0.7–2.0		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

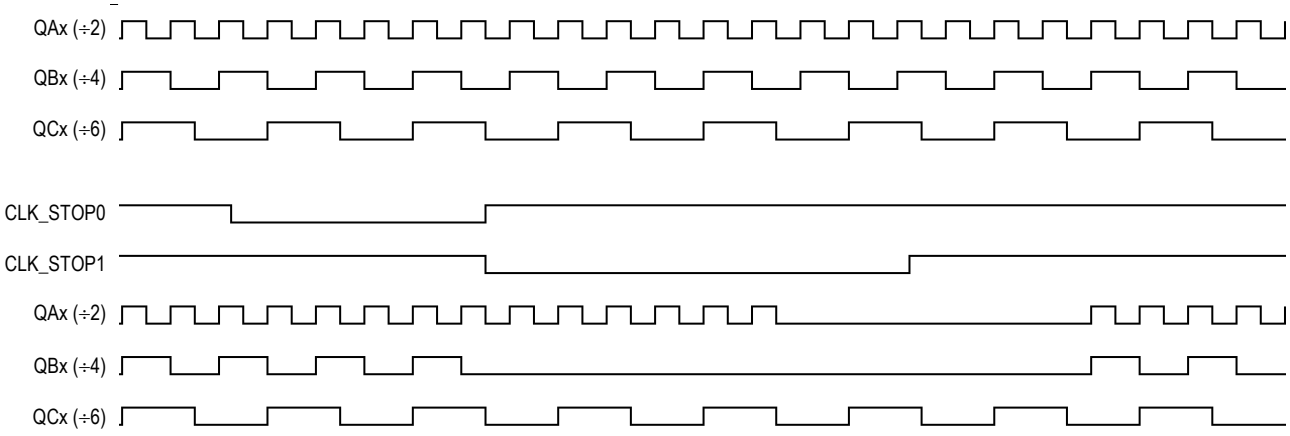
1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. In bypass mode, the MPC9331 divides the input reference clock.
3. The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
4. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
5. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$.
6. The MPC9331 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.
7. Data valid for f_{REF} = 50 MHz and a PLL feedback of ÷8 (e.g. QAx connected to FB_IN and FSELA=1, PWR_DN=1).
8. Data valid for 16.67 MHz < f_{REF} < 100 MHz and any feedback divider. $t_{sk(O)}$ [s] = $t_{sk(O)}$ [°] ÷ ($f_{REF} \cdot 360°$).
9. Output duty cycle is DC = (0.5 ± 500 ps · f_{OUT}) · 100%. (e.g. the DC range at f_{OUT} = 100 MHz is 45% < DC < 55%).
10. All outputs in ÷4 divider configuration.
11. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Output Power Down (PWR_DN) Timing Diagram



Output Clock Stop (CLK_STOP) Timing Diagram



Programming the MPC9331

The MPC9331 supports output clock frequencies from 16.67 to 240 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 4:1, 3:1, 2:1, 1:1, 1:2, 2:3 and 3:2. Table 8 illustrates the various output configurations and frequency ratios supported by the MPC9331. See also Table 9 and Table 10 for further reference.

Table 8. MPC9331 Example Configurations (Internal Feedback: FB_SEL = 0)

fref[1] [MHz]	PWR_DN	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
25.0 – 60.0	0	0	0	0	fref · 4 (100-240 MHz)	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)
	0	0	0	1	fref · 4 (100-240 MHz)	fref · 4 (100-240 MHz)	fref ·4÷3 (33.3-80 MHz)
	0	0	1	0	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)
	0	0	1	1	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)	fref ·4÷3 (33.3-80 MHz)
	0	1	0	0	fref · 2 (50-120 MHz)	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)
	0	1	0	1	fref · 2 (50-120 MHz)	fref · 4 (100-240 MHz)	fref ·4÷3 (33.3-80 MHz)
	0	1	1	0	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)
	0	1	1	1	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref ·4÷3 (33.3-80 MHz)
	1	0	0	0	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)
	1	0	0	1	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref ·2÷3 (16.67-40 MHz)
	1	0	1	0	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)	fref (25.0-60 MHz)
	1	0	1	1	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)	fref ·2÷3 (16.67-40 MHz)
	1	1	0	0	fref (25.0-60 MHz)	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)
	1	1	0	1	fref (25.0-60 MHz)	fref · 2 (50-120 MHz)	fref ·2÷3 (16.67-40 MHz)
	1	1	1	0	fref (25.0-60 MHz)	fref (25.0-60 MHz)	fref (25.0-60 MHz)
	1	1	1	1	fref (25.0-60 MHz)	fref (25.0-60 MHz)	fref ·2÷3 (16.67-40 MHz)

1. fref is the input clock reference frequency (CCLK or PCLK).

Table 9. MPC9331 Example Configurations (External Feedback and PWR_DN = 0)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 2[2]	100 – 240	0	0	0	fref (100-240 MHz)	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)
		0	0	1	fref (100-240 MHz)	fref (100-240 MHz)	fref ÷ 3 (33.3-80 MHz)
		0	1	0	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 2 (50-120 MHz)
		0	1	1	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 3 (33.3-80 MHz)
VCO ÷ 4[3]	50 –120	1	0	0	fref (50-120 MHz)	fref ·2 (100-240 MHz)	fref (50-120 MHz)
		1	0	1	fref (50-120 MHz)	fref ·2 (100-240 MHz)	fref ·2÷3 (33.3-80 MHz)
		1	1	0	fref (50-120 MHz)	fref (100-240 MHz)	fref (50-120 MHz)
		1	1	1	fref (50-120 MHz)	fref (100-240 MHz)	fref ·2 ÷ 3 (33.3-80 MHz)
VCO ÷ 6[4]	33.3 – 80	0	0	1	fref ·3 (100-240 MHz)	fref ·3 (100-240 MHz)	fref (33.3-80 MHz)
		0	1	1	fref ·3 (100-240 MHz)	fref ·3 ÷ 2 (50-120 MHz)	fref (33.3-80 MHz)
		1	0	1	fref ·3 ÷ 2 (50-120 MHz)	fref ·3 (100-240 MHz)	fref (33.3-80 MHz)
		1	1	1	fref ·3 ÷ 2 (50-120 MHz)	fref ·3 ÷ 2 (50-120 MHz)	fref (33.3-80 MHz)

1. fref is the input clock reference frequency (CCLK or PCLK).
2. QAx connected to FB_IN and FSELA=0, PWR_DN=0.
3. QAx connected to FB_IN and FSELA=1, PWR_DN=0.
4. QCx connected to FB_IN and FSELC=1, PWR_DN=0.

Table 10. MPC9331 Example Configurations (External Feedback and PWR_DN = 1**)**

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8[2]	25.0 – 60.0	1	0	0	fref 25-60 MHz)	fref ·2 (50-120 MHz)	fref (2.25-60 MHz)
		1	0	1	fref (25-60 MHz)	fref ·2 (50-120 MHz)	fref ·2÷3 (16.6-40 MHz)
		1	1	0	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	1	1	fref (25-60 MHz)	fref (25-60 MHz)	fref ·2÷3 (16.6-40 MHz)
VCO ÷ 12[3]	16.67 – 40	0	0	1	fref ·3 (50-120 MHz)	fref ·3 (50-120 MHz)	fref (16.67-40 MHz)
		0	1	1	fref ·3 (50-120 MHz)	fref ·3 ÷ 2 (25-60 MHz)	fref (16.67-40 MHz)
		1	0	1	fref ·3 ÷ 2 (25-60 MHz)	fref ·3 (50-120 MHz)	fref (16.67-40 MHz)
		1	1	1	fref ·3 ÷ 2 (25-60 MHz)	fref ·3 ÷ 2 (25-60 MHz)	fref (16.67-40 MHz)

1. fref is the input clock reference frequency (CCLK or PCLK).
2. QAx connected to FB_IN and FSELA=1, PWR_DN=1.
3. QCx connected to FB_IN and FSELC=1, PWR_DN=1.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9331 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance, I/O jitter. The MPC9331 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9331. Figure 3 illustrates a typical power supply filter scheme. The MPC9331 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet, the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 8 mA (12 mA maximum), assuming that a minimum of 3.0 V must be maintained on the V_{CC_PLL} pin.

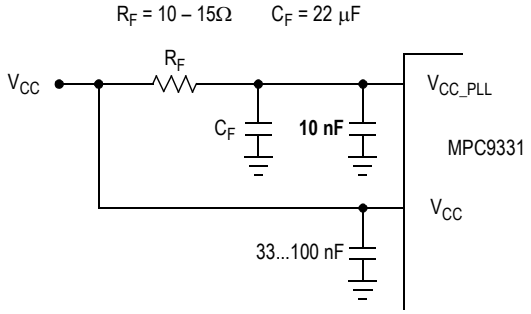


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for RF and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9331 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9331 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9331 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9331 clock driver is effectively doubled due to its capability to drive multiple lines.

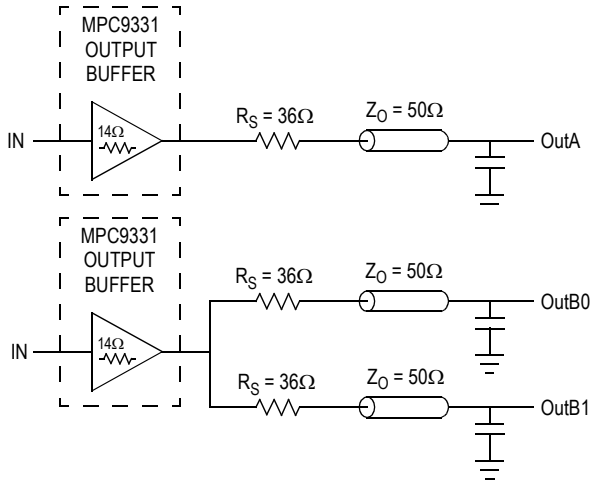


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9331 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9331. The output waveform in Figure 5 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\ \Omega \parallel 50\ \Omega$

$R_S = 36\ \Omega \parallel 36\ \Omega$

$R_0 = 14\ \Omega$

$V_L = 3.0\ (25 \div (18+14+25)$

$= 1.31\ V$

At the load end, the voltage will double due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Final skew data pending specification.

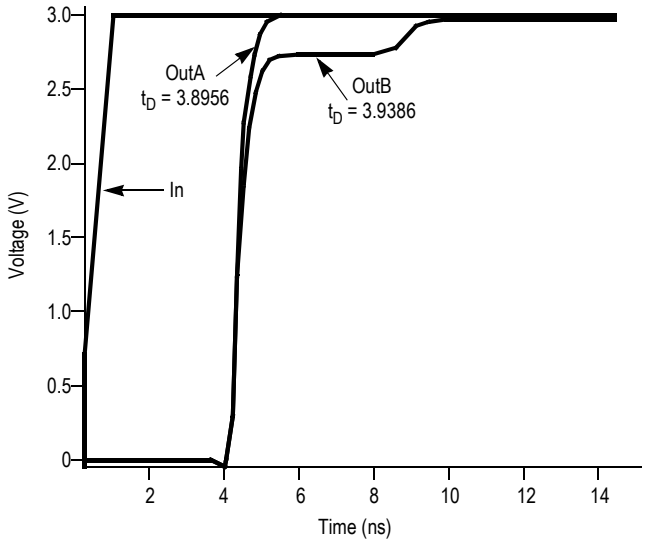
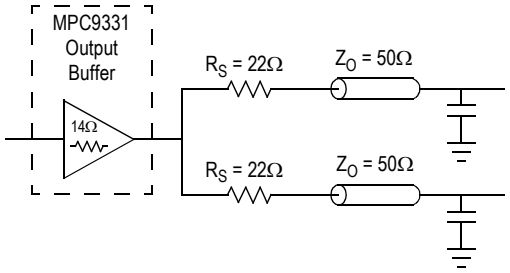


Figure 5. Single versus Dual Line Termination Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$

$25\Omega = 25\Omega$

Figure 6. Optimized Dual Line Termination

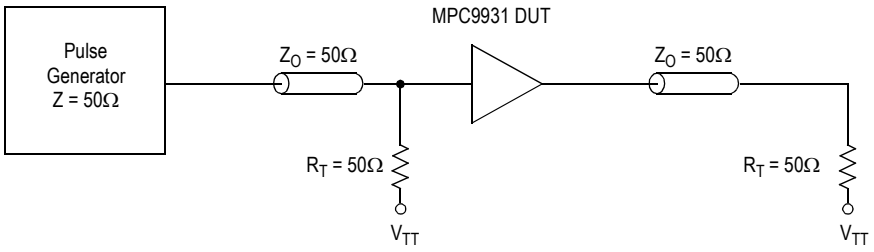
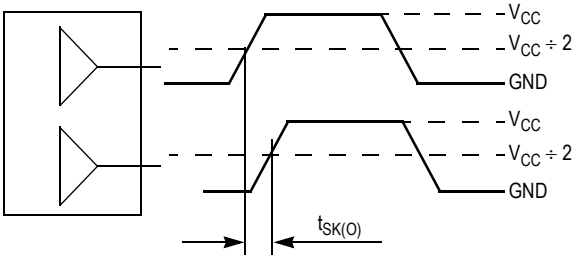


Figure 7. CCLK MPC9331 AC Test Reference for V_{cc} = 3.3 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-Output Skew $t_{SK(O)}$

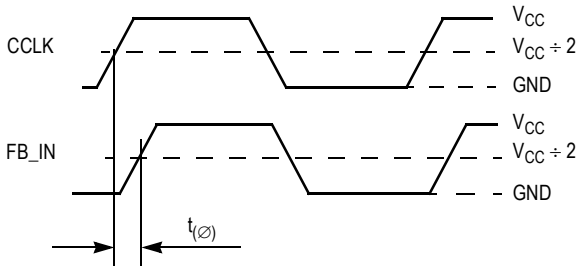
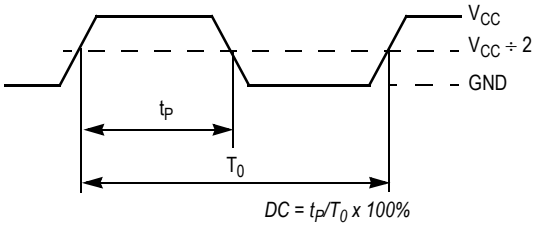
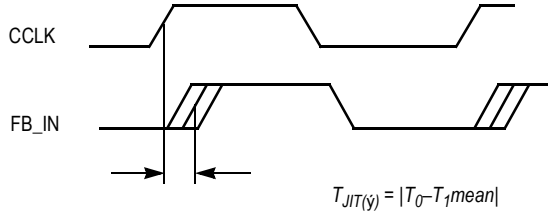


Figure 9. Propagation Delay ($t_{(\varnothing)}$, Static Phase offset) Test Reference



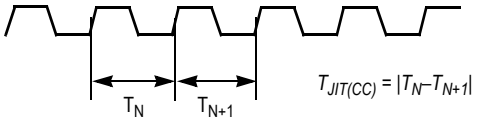
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



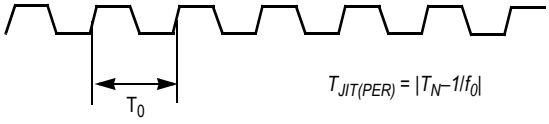
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

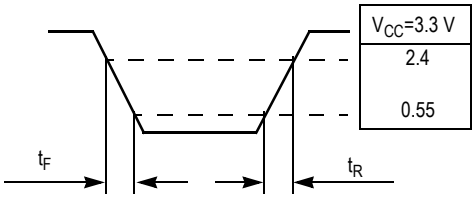
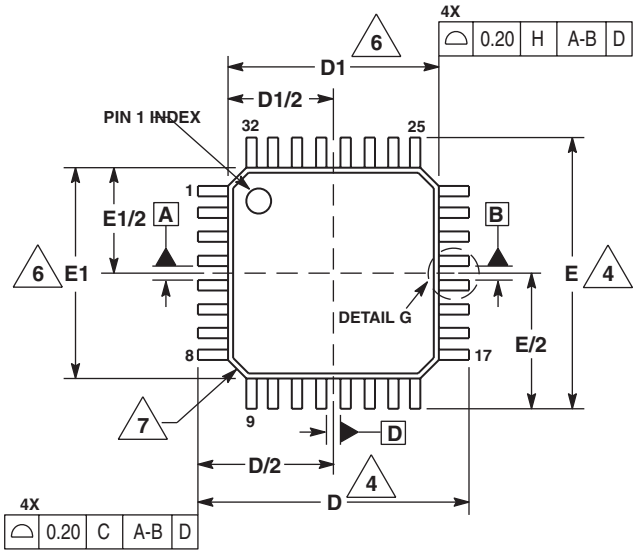
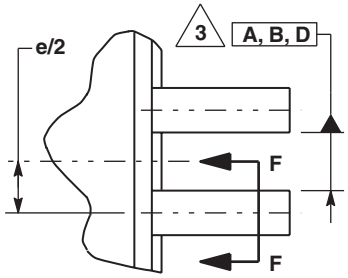


Figure 14. Output Transition Time Test Reference

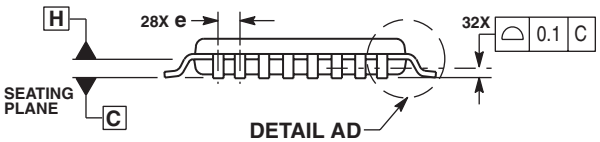
PACKAGE DIMENSIONS



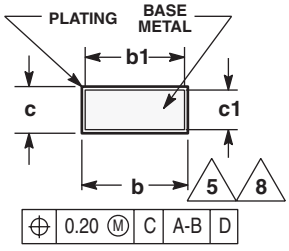


DETAIL G

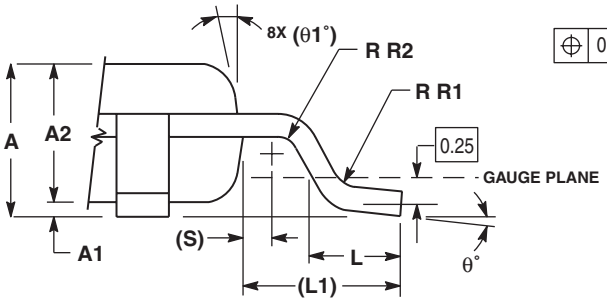
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.



DETAIL AD



SECTION F-F



DETAIL AD

DIM	MILLIMETERS MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12° REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
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MPC9331
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