Dual PLL Clock Generator

MPC9100

DUAL PLL CLOCK GENERATOR

The MPC9100 is a dual PLL phase locked loop clock generator. The device synthesizes a 14.318 MHz input reference to provide a buffered copy of the input reference, a 31.3344MHz clock output and a 45.1584 clock output.

The device features a fully integrated crystal oscillator as the clock reference source. No external components are required other than the 14.318 MHz crystal. The TCLK input is used only for factory test and cannot be used as the PLL clock reference. To reduce total die area the PLL loop filter capacitors are brought outside the chip. The FCAP pins are used to connect these capacitors to the internal PLL's. 0.01µf capacitors are recommended.

The device features three synchronous output enable pins to allow for shutting down specific clocks. When driven to a logic LOW the OE pins will freeze the selected clock in its low state. Internal timing has been established that guarantee transition into and out of the freeze state will not produce output glitches. These control inputs have internal pull up resistors so that they will default to the output active state.

The TEST0–2 pins allow for the testing of the internal logic of the device. Most of the states are reserved for factory test use with one exception. When the TEST 0 pin is driven low the internal state machines will be reset and the outputs will be driven into high impedance. The TEST pins also have internal pull up resistors such that they will default into the normal operation mode of the chip.

The MPC9100 features separate internal power buses to try to isolate the output noise from the internal PLL's and the other outputs. The VCCA pins are the power supply pins for the analog PLL's, the VCCI pin is the power supply for the internal core logic and the VCCO's are the power pins for the output buffers. All of these pins should be tied to a common power plane on the printed circuit board.



FA SUFFIX
TQFP PACKAGE
CASE 873A–02

FUNCTION TABLES

TEST2	TEST1	TEST0	Function
0	0	0	Factory Test
0	0	1	Factory Test
0	1	0	Factory Test
0	1	1	Factory Test
1	0	0	Factory Test
1	0	1	Factory Test
1	1	0	Master Reset/Tristate
1	1	1	Normal Operation

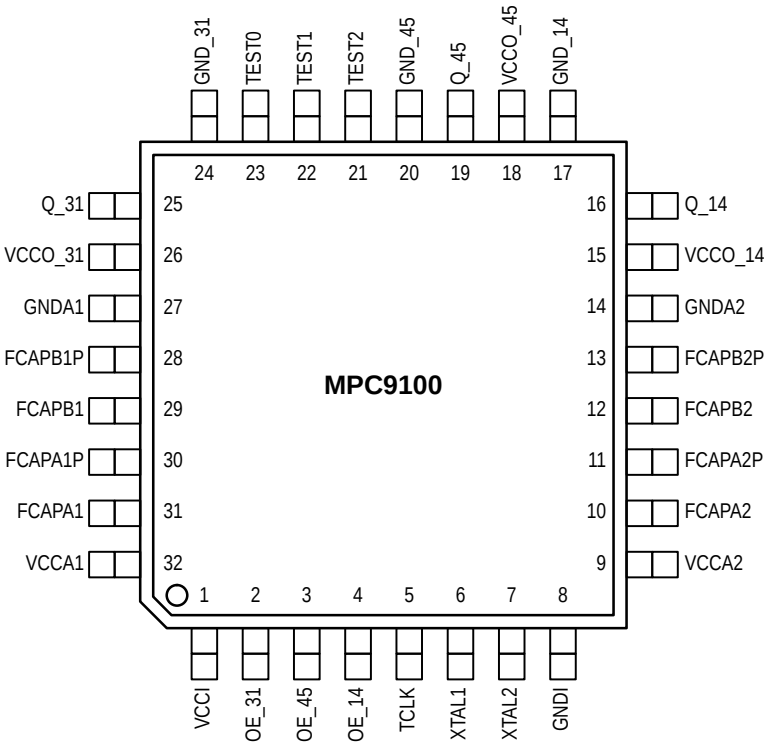
OE_XX	Function
0	Output LOW
1	Output Active

PIN DESCRIPTION

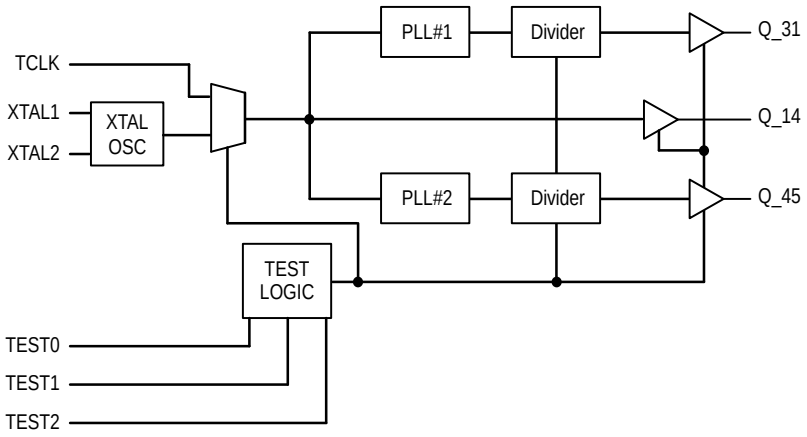
Pin	Description
Q_31	31.3344MHz Output
Q_14	14.318MHz Output
Q_45	45.1584MHz Output
VCCO_XX	Output Buffer Power Supply
GNDO_XX	Output Buffer Ground
VCCI	Core Logic Power Supply
GNDI	Core Logic Ground
VCCAX	PLL Power Supply
GNDAX	PLL Ground
XTAL1	Crystal Oscillator Input
XTAL2	Crystal Oscillator Input
TCLK	LVCMOS Reference Clock Input
FCAPXX	PLL Filter Capacitor Input
FCAPXXP	PLL Filter Capacitor Input

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Pinout: 32–Lead TQFP Package (Top View)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
f_{ref}	Reference Input Frequency	10	20	MHz	

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage	0.8			V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA[1]
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA[1]
I_{IN}	Input Current			±120	µA	Note 2
I_{CC}	Maximum Quiescent Supply Current				mA	
C_{IN}				4	pF	
C_{pd}			25		pF	

1. The MPC9100 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up resistors which affect input current, $\overline{\text{PECL_CLK}}$ has a pull–down resistor.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.15		1.0	ns	0.8 to 2.0V, 50Ω to V_{CC}/2
t_{pw}	Output Duty Cycle	45		55	%	50Ω to V_{CC}/2
f_{Xtal}	Crystal Oscillator Frequency Range	10		20	MHz	Note 2
t_{PLZ}, t_{PHZ}	Output Disable Time	2.0	5.0	8.0	ns	50Ω to V_{CC}/2
t_{PZL}	Output Enable Time	3.0	6.5	10	ns	50Ω to V_{CC}/2
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100	±250	ps	Note 3
t_{lock}	Maximum PLL Lock Time			10	ms	

1. X_1, X_2, X_3, and X_4 all to be determined. The specs hold only when the MPC9100 is used in the external feedback mode.
2. See Applications Info section for crystal specifications.
3. All outputs switching.

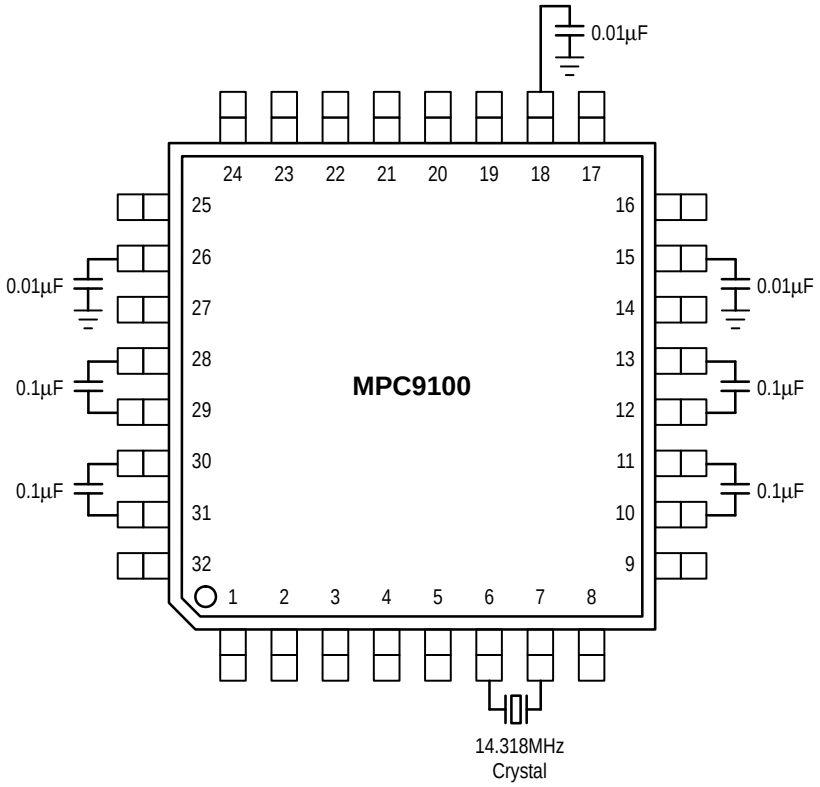


Figure 1. Recommended External Components
(See Applications Section for Optional Analog Supply Filter)

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9100 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9100 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9100.

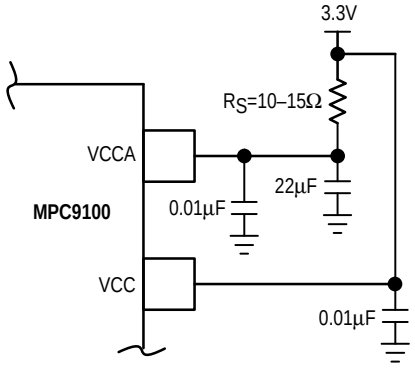


Figure 2. Power Supply Filter

Figure 2 illustrates a typical power supply filter scheme. The MPC9100 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC9100. The current into the VCCA pin is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 2 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

Although the MPC9100 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the On–Board Crystal Oscillator

The MPC9100 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9100 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC9100 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Driving Transmission Lines

The MPC9100 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9100 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9100 clock driver is effectively doubled due to its capability to drive multiple lines.

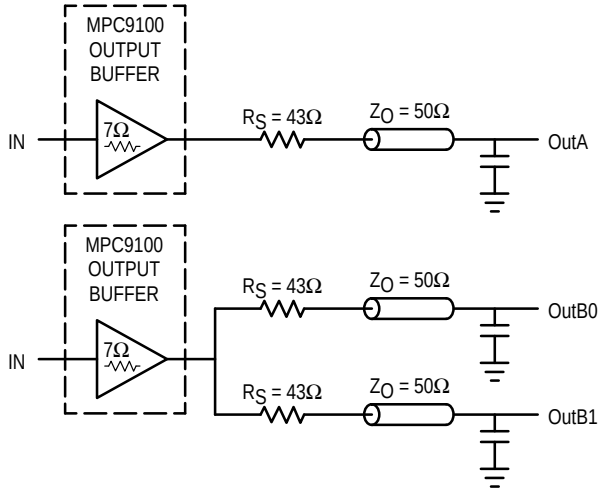


Figure 3. Single versus Dual Transmission Lines

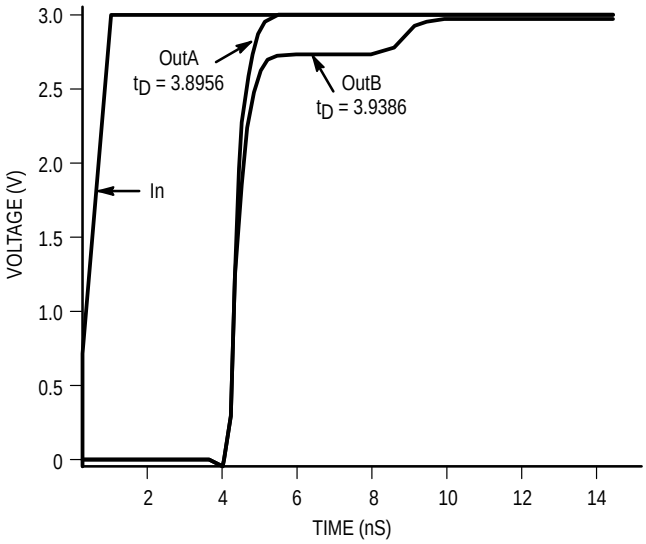


Figure 4. Single versus Dual Waveforms

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC9100 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC9100. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

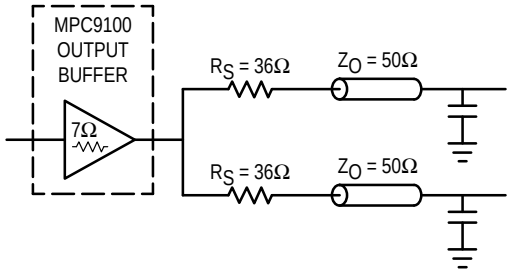
$$VL = VS (Zo / (Rs + Ro + Zo))$$

$Zo = 50\Omega \parallel 50\Omega$
$Rs = 43\Omega \parallel 43\Omega$
$Ro = 7\Omega$

$$VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



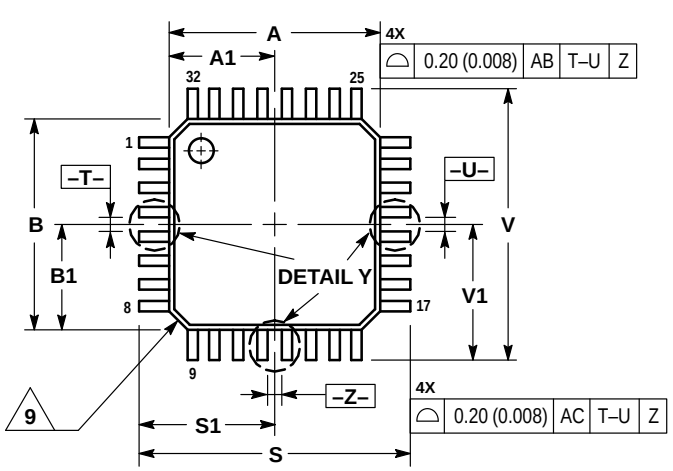
$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

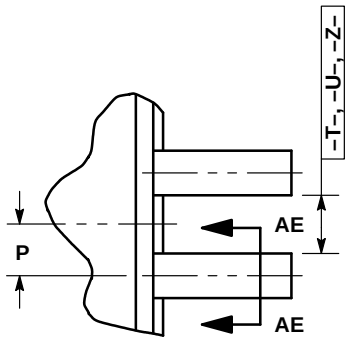
Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

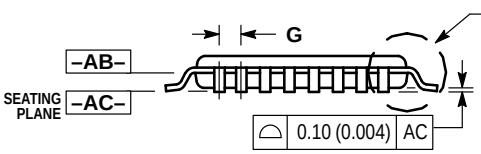
OUTLINE DIMENSIONS

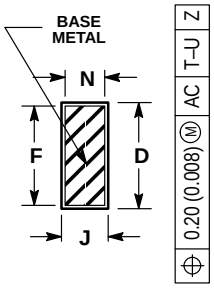
FA SUFFIX
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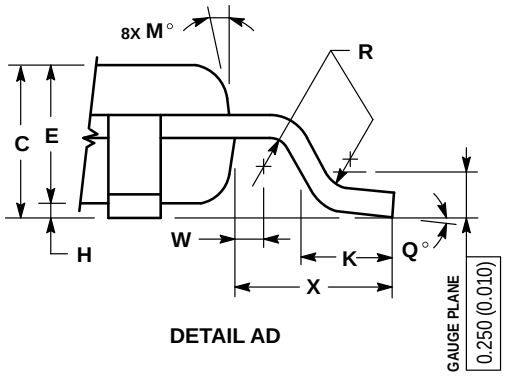


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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