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MEGAWIN

Features

- 80C51 Central Processing Unit
- 4KB On-Chip program memory
- ISP capability; optional 1KB/2KB/4KB ISP memory shared with *data flash* memory.
- IAP capability; up to 11K bytes programmable *data flash* available shared with ISP memory.
- On-Chip 256 bytes scratch-pad RAM and 256 bytes auxiliary RAM; Be capable of addressing up to 64K bytes external memory
- MOVC-disabling, encrypting, and locking flash memory realize security mechanism.
- Three 16-bits timer/counter, Timer2 is an up/down counter with programmable clock output on P1.0
- Eight sources, four-level-priority interrupt capability
- Enhanced UART, provides frame-error detection and hardware address-recognition
- Dual DPTR for fast-accessing of data memory
- 15 bits Watch-Dog-Timer with 8-bits pre-scalar, one-time enabled
- Power control: Idle mode and Power-Down mode; Power-Down can be woken-up by P3.2/P3.3/P4.2/P4.3
- Low EMI: inhibits ALE emission
- Four 8-bits bi-directional ports; extra four-bits additional P4 are available for PLCC-44 and PQPF-44
- On-Chip flash program/data memory:
  - The data endurance of the embedded flash gets over 20,000 times.
  - Greater than 100 years data rentention under room temperature
- Operating Voltage:
  - 4.5V~5.5V for MPC89E51A
  - 2.4V~3.6V for MPC89L51A, minimum 2.7V requirement in flash write operation (ISP/ICP/……)
  - Built-in Low-Voltage-Reset circuit.
- Operating Temperature
  - Industrial (-40°C to +85°C)*
- Maximum Operating Frequency:
  - Optional 12T or 6T mode
  - Up to 48MHz@12T or 24MHz@6T, Industrial range
- Three package types:
  - PDIP 40: MPC89x51AE
  - PLCC 44: MPC89x51AP
  - PQFP 44: MPC89x51AF

  *: Tested by sampling

General Description

MPC89x51A is a single-chip 8-bits micro-controller with the instruction sets fully compatible with industrial-standard 80C51 series microcontroller.

There is 4 Kbytes flash memory embedded for application program, 11 Kbytes *data flash* shared by In-System Programming code, and In-Application-Programming code. In-System Programming and In-Application Programming allow the users to download new code or data while the microcontroller sits in the running state.

There are 512 bytes on-chip RAM embedded that are provided to implement wide field applications. The user can configure the device to run in 12 clocks per machine cycle, or 6 clocks per machine cycle to achieve twice performance.

MPC89x51A is built with four 8-bits I/O ports, one 4-bits I/O ports, three 16-bits timer/counters, an eight-source, four-priority-level interrupt structure, an enhanced UART and on-chip crystal oscillator. It was fabricated in advanced embedded flash CMOS technology.

Excellent flash-endurance, flash-retention, and code-protecting security make MPC89x51A as an excellent microcontroller.

If the supply voltage of the device is lower than 3.7V/2.4V (Operate in the 5V/3V), the device can automatically go to reset, and we have named it the Low-Voltage-Reset.

Order Information:

Part Number	Temperature Range	Package	Packing	Operation Voltage x : (L/E)
MPC89x51AE	**Industrial**	**PDIP-40**	**Tube**	**L:3V / E:5V**
MPC89x51AP	**Industrial**	**PLCC-44**	**Tube**	**L:3V / E:5V**
MPC89x51AF	**Industrial**	**PQFP-44**	**Tube**	**L:3V / E:5V**

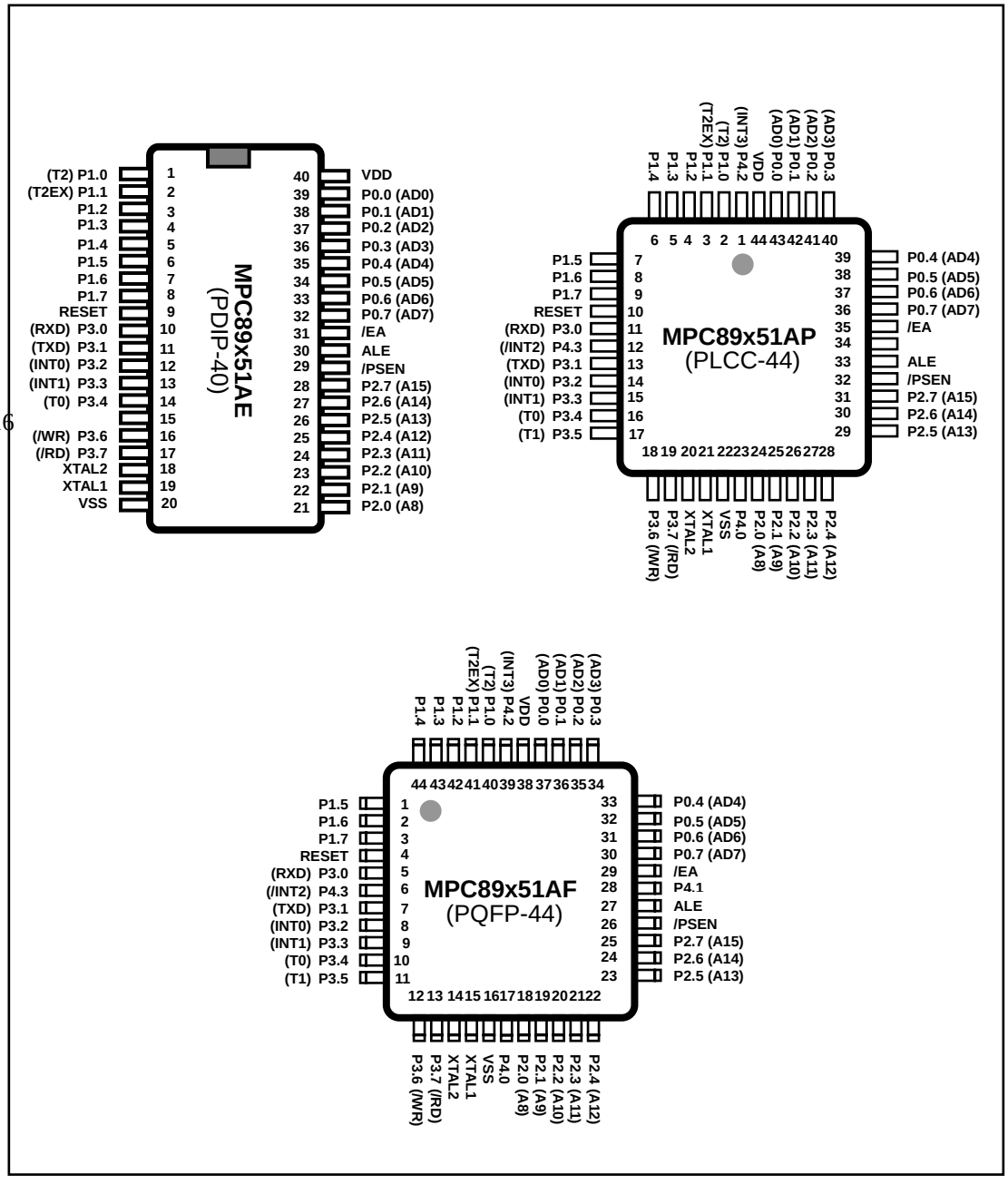
Pin Description

Pin Definition

Pin Name	Pin Number			Type	Description
	DIP-40	PLCC-44	PQFP-44		
P0.0 (AD0)	39	43	37	B	Port0 is an open-drain, bi-directional IO port. When *1*s are written to Port0, they become high-impedance inputs. Port0 is also multiplexed with low-order address or data bus during accesses to external program and data memory.
P0.1 (AD1)	38	42	36		
P0.2 (AD2)	37	41	35		
P0.3 (AD3)	36	40	34		
P0.4 (AD4)	35	39	33		
P0.5 (AD5)	34	38	32		
P0.6 (AD6)	33	37	31		
P0.7 (AD7)	32	36	30		
P1.0 (T2)	1	2	40	BU	General-purposed I/O with weak pull-up resistance inside. When *1*s are written into Port1, the strong output driving PMOS only turn-on two clock periods and then the weak pull-up resistance keep the port high. P1.0 is also used as one of event sources for timer2, or output carrier of timer2, alias T2. P1.1 is also used as one of interrupt-controlling sources for time2, alias T2EX.
P1.1 (T2EX)	2	3	41		
P1.2	3	4	42		
P1.3	4	5	43		
P1.4	5	6	44		
P1.5	6	7	1		
P1.6	7	8	2		
P1.7	8	9	3		
P2.0 (A8)	21	24	18	BU	Port2 is an 8-bits bi-directional I/O port with pull-up resistance. Except being as GPIO, Port2 emits the high-order address bytes during accessing to external program and data memory.
P2.1 (A9)	22	25	19		
P2.2 (A10)	23	26	20		
P2.3 (A11)	24	27	21		
P2.4 (A12)	25	28	22		
P2.5 (A13)	26	29	23		
P2.6 (A14)	27	30	24		
P2.7 (A15)	28	31	25		
P3.0 (RXD)	10	11	5	BU	General-purposed I/O with weak pull-up resistance inside. When *1*s are written into Port1, the strong output driving PMOS only turn-on two clock periods and then the weak pull-up resistance
P3.1 (TXD)	11	13	7		
P3.2 (INT0)	12	14	8		
P3.3 (INT1)	13	15	9		
P3.4 (T0)	14	16	10		

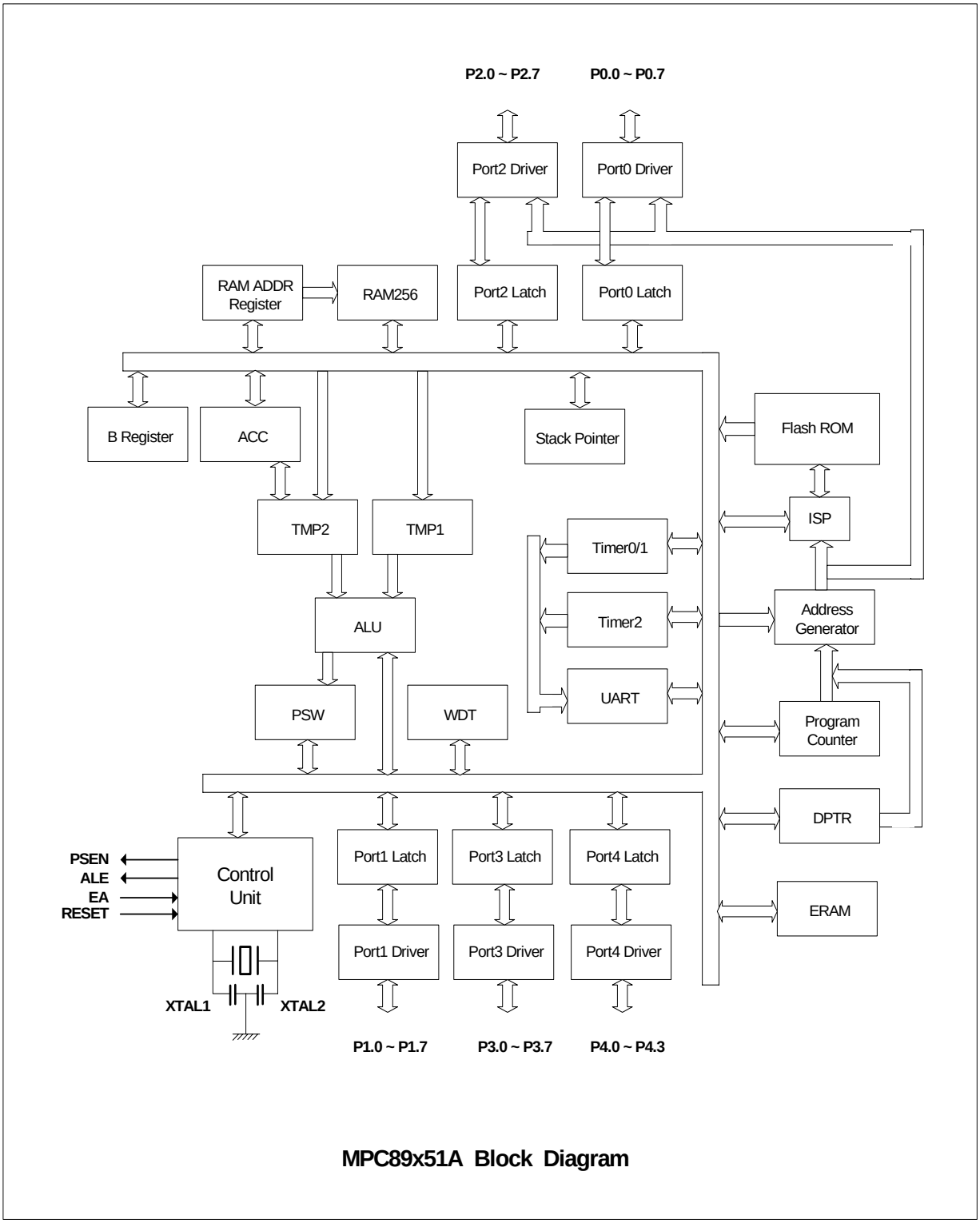
P3.5 (T1) P3.6 (/WR) P3.7 (/RD)	15 16 17	17 18 19	11 12 13		keep the port high. Port3 also serves other special functions of this device. P3.0 and P3.1 act as receiver and transceiver of the data for UART function block, Alias RXD and TXD. P3.2 and P3.3 also act as external interrupt sources, alias INT0 and INT1. P3.4 and P3.5 also act as event sources for timer0 and timer1 individually, alias T0 and T1. P3.6 also acts as write signal while access to external memory, alias /WR. P3.7 also acts as read signal while access to external memory, alias /RD.
P4.0 P4.1 P4.2 (/INT3) P4.3 (/INT2)		23 34 1 12	17 28 39 6	BU	Port4 is extended I/O ports such like Port1. It can be available only on 44L-PLCC and 44L-PQFP package.
RESET	9	10	4	IS	A high on this pin for at least two machine cycles will reset the device.
ALE	30	33	27	O	Output pulse for latching the low bytes of address during accesses to external memory.
/PSEN	29	32	26	O	The read strobe to external program memory, low active.
/EA	31	35	29	I	EA must be kept at low to enable the device to fetch program code from external flash memory. An internal pull-up resistance has been embedded in this pin.
XTAL1	19	21	15	I	Input to the inverting oscillator amplifier.
XTAL2	18	20	14	O	Output from the inverting amplifier.
VDD	40	44	38	P	Power Supply
VSS	20	22	16	G	Ground

Pin Configuration



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Block Diagram



MPC89x51A Block Diagram

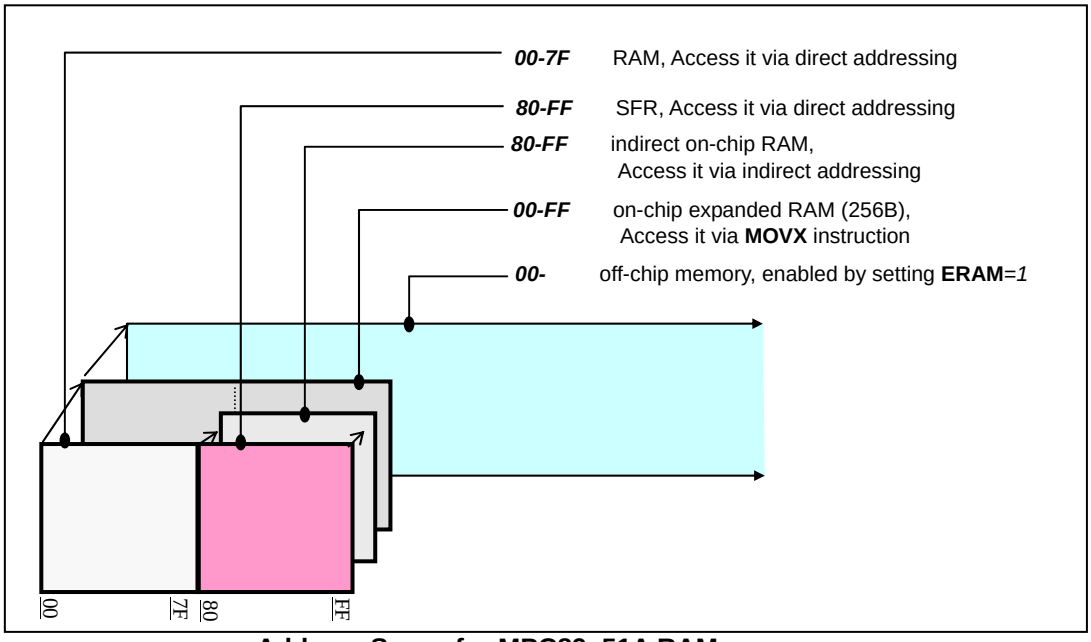
Special Function Register

F8								
F0	B							
E8	P4							
E0	ACC	WDTCR	IFD	IFADRH	IFADRL	IFMT	SCMD	ISPCR
D8								
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0	XICON							
B8	IP	SADEN						
B0	P3							IPH
A8	IE	SADDR						
A0	P2		AUXR1					
98	SCON	SBUF						
90	P1			*Reserved*				
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	
80	P0	SP	DPL	DPH				PCON

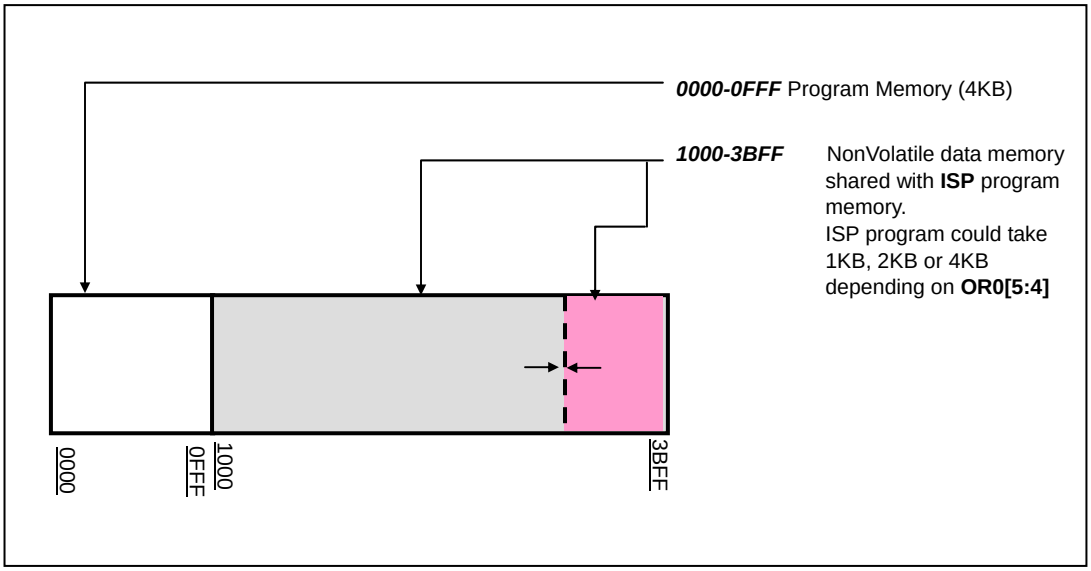
SYMBOL	DESCRIPTION									INITIAL VALUE
P0	Port 0									11111111B
SP	Stack Pointer									00000111B
DPL	Data Pointer Low									00000000B
DPH	Data Pointer High									00000000B
PCON	Power Control	SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL	01110000B
TCON	Timer Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000B
TMOD	Timer Mode	GATE	C//T	M1	M0	GATE	C//T	M1	M0	00000000B
TL0	Timer Low 0									00000000B
TL1	Timer Low 1									00000000B
TH0	Timer High 0									00000000B
TH1	Timer High 1									00000000B
AUXR	Auxiliary							ERAM	AO	xxxxx00B
P1	Port 1							T2EX	T2	11111111B
SCON	Serial Control	SM0 /FE	M1	SM2	REN	TB8	RB8	TI	RI	00000000B
SBUF	Serial Buffer									xxxxxxxxB
P2	Port 2									11111111B
AUXR1	Auxiliary 1					GF2			DPS	xxxx0xx0B
IE	Interrupt Enable	EA		ET2	ES	ET1	EX1	ET0	EX0	00000000B
SADDR	Slave Address									00000000B
P3	Port 3	RD	WR	T1	T0	INT1	INT0	TXD	RXD	11111111B
IPH	Interrupt Priority High	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
IP	Interrupt Priority Low			PT2	PS	PT1	PX1	PT0	PX0	x0000000B
SADEN	Slave Address Mask									00000000B
XICON	External Interrupt Control	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2	
T2CON	Timer 2 Control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	00000000B
T2MOD	Timer2 mode							T2OE	DCEN	xxxxxx00B
RCAP2L	Timer2 Capture Low									00000000B
RCAP2H	Timer2 Capture High									00000000B
TL2	Timer Low 2									00000000B
TH2	Timer High 2									00000000B
PSW	Program Status Word	CY	AC	F0	RS1	RS0	OV	-	P	00000000B
ACC	Accumulator									00000000B
WDTCR	Watch-dog-timer Control register	-	-	ENW	CLW	WIDL	PS2	PS1	PS0	xx000000B
IFD	ISP Flash data									11111111B
IFADRH	ISP Flash Address High									00000000B
IFADRL	ISP Flash Address Low									00000000B
IFMT	ISP Mode Table	-	-	-	-	-	MS2	MS1	MS0	xxxxx000B
SCMD	ISP Serial Command									xxxxxxxxB
ISPCR	ISP Control Register	ISPEN	BS	SRST	-	-	ICK2	ICK1	ICK0	000xx000B
P4	Port 4	-	-	-	-	EBH	EAH	E9H	E8H	xxxx1111B
B	B Register									00000000B

Memory

Organization



Address Space for MPC89x51A RAM



Address Space for MPC89x51A embedded Flash memory

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
		ISPAS1	ISPAS0	-	MOVCL	SB	LOCK

Non-volatile register OR0

7	6	5	4	3	2	1	0
FZWDTCR			OSCDN			HWBS	EN6T

Non-volatile register OR1

Nonvolatile Registers:

There are two Nonvolatile Registers named **OR0** and **OR1** individually. They are designed to configure the MPC89x51A options.

Generally these two nonvolatile registers will be written via a popular NVM writer, say Hi-Lo System All-11, Leaper-48 and Megawin-Provided MCU writer. Furthermore, the user can change the NVM register **OR1** by the ISP program in a manner as same as writing the *data flash*, but **OR0** can only be written via an off-line popular NVM writer.

NVM register: OR0 *(*Option Register 0*):*

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
-	**-**	**ISPAS1**	**ISPAS0**	**-**	**MOVCL**	**SB**	**LOCK**

{**ISPAS1**, **ISPAS0**}: Used to identify the start address for ISP program
{*0, 0*}:= The ISP space is from 0x2C00 to 0x3BFF (4K size).
{*0, 1*}:= The ISP space is from 0x3400 to 0x3BFF (2K size).
{*1, 0*}:= The ISP space is from 0x3800 to 0x3BFF (1K size)
{*1, 1*}:= No ISP space.
These two bits decide where the ISP program locates, and how the ISP program and the *data flash* shares the 11K embedded flash.

MOVCL: Used to determine if MOVC instruction will be disabled.
0:= MOVC is conditionally disabled.
1:= MOVC is always available.

SB: Used to determine if the program code will be scrambled while it is dumped.
0:= Code dump from Writer is scrambled.
1:= Code dump from Writer is transparent.

LOCK: Used to determine if the program code will be locked against the popular writer.
0:= lock code.
1:= does not lock code
If the code is locked, all the data dumped from a popular will always show *FF*h.

Please check file "initial Configuration.pdf" to get the default value of the OR0.

NVM register: OR1 *(*Option Register 1*):*

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
FZWDTCR			**OSCDN**			**HWBS**	**EN6T**

FZWDTCR: Used to freeze the WDT-controlling register.

0:= Configure the SFR **WDTCR** to be reset only via power-up action; not by software reset nor reset from the Watch Dog Timer.

1:= (default) Permit all the reset events from power-up, software and the Watch Dog Timer could reset the SFR **WDTCR**.

OSCDN: Used to adjust the behavior of crystal oscillator.

0:= The DC gained of crystal oscillator amplifier is doubled but bandwidth is reduced. It will bring help to EMI reducing and improve the power consumption. Dealing with application, it does not need high frequency clock (under 20MHz). It is recommended to do so.

1:= The gained of crystal oscillator is enough for oscillator to start oscillating up to 48 MHz.

HWBS: Used to configure the MPC89x51A boot from ISP program or normal application program after the power-on sequence.

0:= The MPC89x51A will boot from ISP start address after power-on.

1:= No operation. The MPC89x51A will boot from normal application program.

EN6T: Used to configure the MPC89x51A run in 6T 12T mode or 6T mode.

0:= The MPC89x51A will run in 6T mode

1:= The MPC89x51A will run in 12T mode

The default value of the **OR1** is *FF*h.

RAM

There are 512 bytes RAM built in MPC89x51A.

The user can visit the leading 128-bytes RAM via direct addressing instructions, we have named those RAM as *direct RAM* that occupies address space 00h to 7Fh.

Followed 128-bytes RAM can be visited via indirect addressing instructions, we have named those RAM as *indirect RAM* that occupied address space 80h to *FF*h.

The other 256-bytes RAM is named expanded RAM that still occupied address space 00h to FFh. An user can access it via general register **R*i***, or via data pointers **DPTR** associated with *MOVX* instructions, say MOVX A, @R1 or MOVX A, @DPTR. To reserve the natural characteristic of instruction *MOVX* which is designed to access external memory, the user can set the bits **ERAM** in SFR **AUXR** as 1, and by doing so is to hide the *expanded RAM* and to visit the external memory.

Embedded Flash

There is totally 15 K bytes flash embedded in the MPC89x51A.

The leading 4 K bytes flash memory is designed for storage of the user program, followed 11 K bytes flash memory is shared with nonvolatile *data flash* and ISP program.

While the program counter of MPC89x51A is spanning over 0FFFh, the device will fetch its program code from the external memory at once ignoring the **/EA** pin status. In that case, it will never fetch the program code from the following embedded flash.

The user can develop the ISP program and put it into the embedded flash that addressed from 2C00h, 3400h, or 3800h by configuring **OR0[5:4]**. Excluding the ISP program, the remained flash spaces can be taken as *data flash* which can be read, even written by the application program or the ISP program from the user.

Functional Description

TIMERS/COUNTERS

MPC89x51A has three 16-bits timers, and they are named **T0**, **T1** and **T2**.Each of them can also be used as a general event counter, which counts the transition from 1 to 0.

While **T0/T1/T2** is used as "timer" function, the time unit that used to measure the timer is *machine cycle*. A machine cycle equals 12 or 6 oscillator periods, and depends on 12T mode or 6T mode that the user configured this device.

While **T0/T1/T2** is used as "1-0 event counter" function, the counting event is the "high-to-low transition" of primitive pin **T0/T1/T2**. In this mode, the device periodically samples the status of pin **T0/T1/T2** once for each machine cycle. Whenever the sampled result turns from 1 to 0, the device will count once on the counter. Becarefully, this kind of implementation for the counter requires the high-duty or low-duty from pin **T0/T1/T2** and must not too short compared to a machine cycle.

There are two SFR designed to configure timers **T0** and **T1**. They are **TMOD**, and **TCON**.
There are extra two SFR designed to configure timer **T2**. They are **T2MOD**, and **T2CON.**

SFR**: TMOD**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
(for timer1 use)				(for timer0 use)			
GATE	**C//T**	**M1**	**M0**	**GATE**	**C//T**	**M1**	**M0**

GATE: Gating control when set. If GATE=1, Timer/Counter *x* is enabled only while "/INT*x*" pin is high and **"**TR*x*" control bits is set. When cleared Timer *x* is enabled whenever "TR*x*" control bits is set.

C//T: Timer or Counter function selector. *0*: =timer (Default), *1*: =counter

{M1, M0}: mode select

{0, 0}: = 13-bits timer/counter for Timer0 and Timer1

{0, 1}: = 16-bits timer/counter for Timer0 and Timer1

{1, 0}: = 8-bits timer/counter with automatic reload for Timer0 and Timer1

{1, 1}: = for Timer0: = TL0 is 8-bits timer/counter, TH0 is locked into 8-bits timer

for Timer1:= Timer/Counter1 Stopped

SFR**: TCON**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
TF1	**TR1**	**TF0**	**TR0**	**IE1**	**IT1**	**IE0**	**IT0**

TF1: =Timer1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or clearing the bits in software.

TR1: =Timer1 run control bits. Set/Cleared by software.

TF0: =Timer0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or clearing the bits in software.

TR0: =Timer1 run control bits. Set/Cleared by software.

IE1: =Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.

IT1: =Interrupt 1 type control bits. Set/Cleared by software to specified falling edge/low level triggered interrupt.

IE0: =Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.

IT0: =Interrupt 0 type control bits. Set/Cleared by software to specified falling edge/low level triggered interrupt.

SFR**: T2MOD**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
						T2OE	**DCEN**

T2OE: Timer 2 Output Enable bits. It enables Timer2 overflow rate to toggle P1.0.

DCEN: Down Count Enable bits. When set, this allows Timer2 to be configured as a down counter.

SFR**: T2CON**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C//T2**	**CP/RL2**

TF2: Timer2 overflow flag. It will be set by a Timer2 overflow and must be cleared by software.
TF2 will not be set when either **TCLK** or **RCLK** =1.

EXF2: Timer2 external flag. It will be set when either a capture or reload is caused by a negative transition on pin **T2EX** and **EXEN2**=1. When Timer2 interrupt is enabled, **EXF2**=1 will cause the CPU to vector to the timer2 interrupt routine. **EXF2** must be cleared by software. **EXF2** does not cause an interrupt in Auto-Reload Up-Down mode (**ARUD**).

RCLK: When set causes the serial port to use Timer2 overflow pulse for its receive clock in mode and mode 3. RCLK=0 causes Timer1 overflow pulse to be used.

TCLK: When set causes the serial port to use Timer2 overflow pulse for its transmit clock in mode 1 and mode 3. **RCLK**=0 causes Timer1 overflow pulse to be used.

EXEN2: Timer-2 external enable flag. When set, allows a capture or reload to occur. As a result of a negative transition on **T2EX** if Timer2 is not being used to clock the serial port.
EXEN2=0 causes Timer2 to ignore events at **T2EX**.

TR2: Start/Stop control for Timer2.

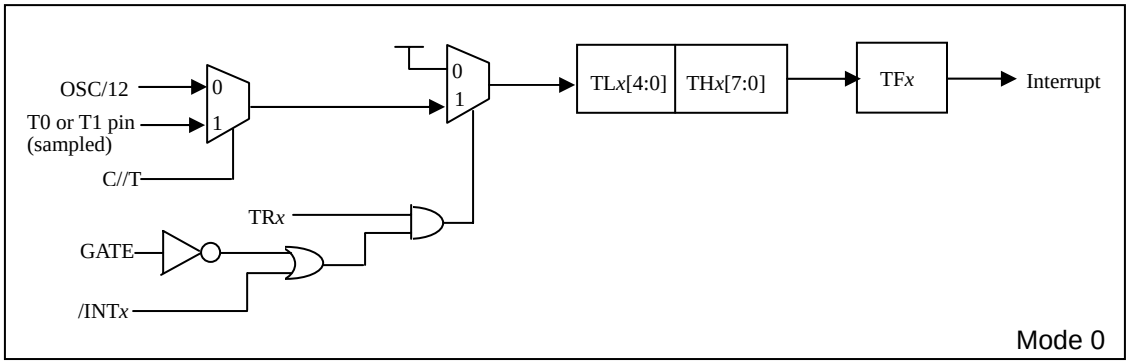
C/T2: Timer or counter select. 0 is for timer and 1 is for external event counter.

CP/RL2: Capture/Reload flag. When set, captures will occurs on a negative transition at **T2EX** if **EXEN2**=1. When cleared, auto-reloads will occur either with Timer2 overflows or a negative transition at **T2EX** when **EXEN2**=1. When whether **TCLK** or **RCLK** is 1, this bits is ignored and the timer is forced to auto-reload on Timer2 overflow.

TIMER0 (T0) AND TIMER1 (T1)

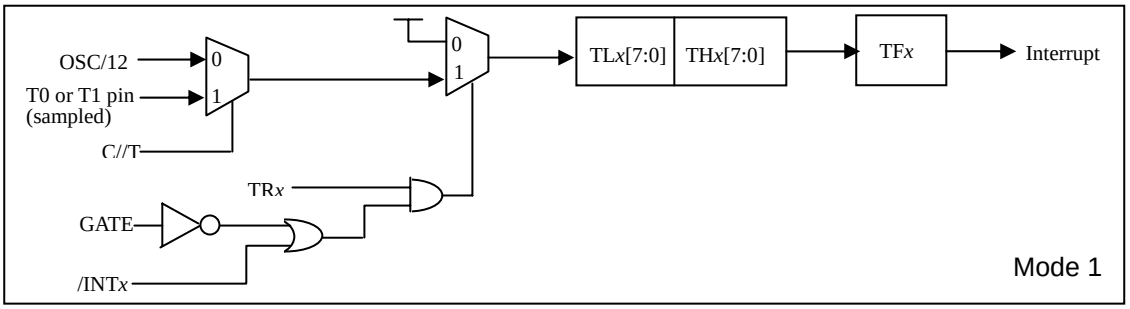
Mode 0

The timer register is configured as a 13-bits register. As when the count rolls over from all 1s to all 0s, it sets the timer interrupt flag **TFx**. The counted input is enabled to the timer when **TRx** = 1 and either GATE=0 or INTx = 1. Mode 0 operation is the same for Timer0 and Timer1.



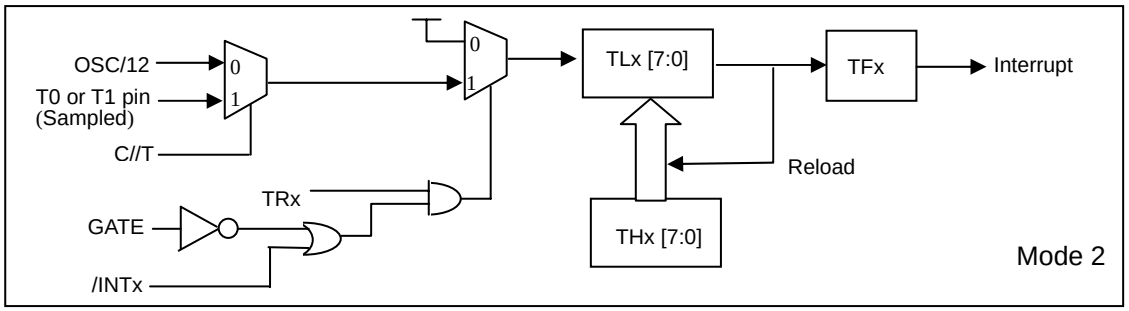
Mode 1

Mode1 is the same as Mode0, except that the timer register is being run with all 16 bits.



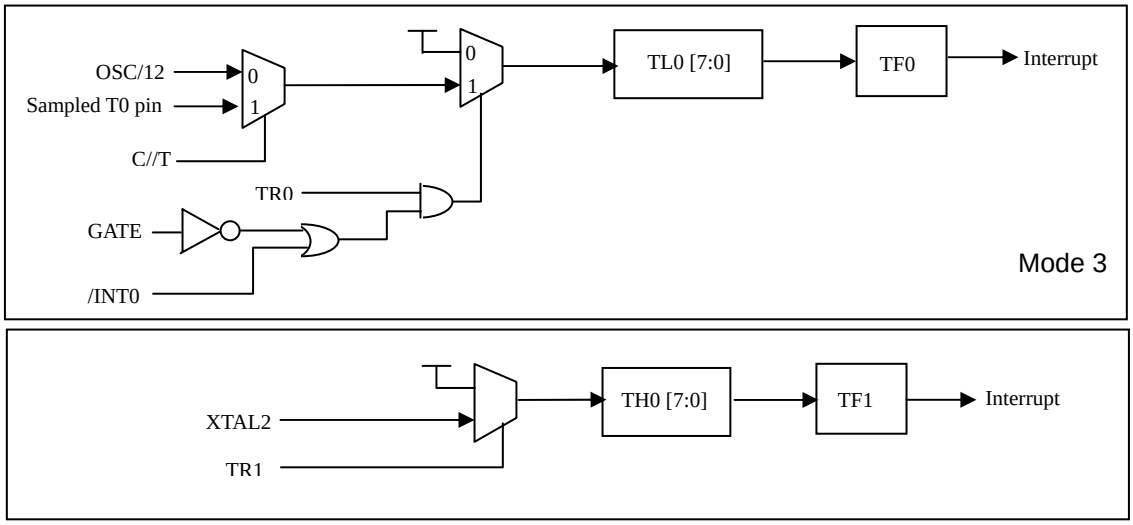
Mode 2

Mode 2 configures the timer register as an 8-bits counter (TL*x*) with automatic reload. Overflow from TL*x* does not only set TF*x*, but also reloads TL*x* with the content of TH*x*, which is determined by user's program. The reload leaves TH*x* unchanged. Mode 2 operation is the same for Timer0 and Timer1.



Mode 3

Timer1 in Mode3 simply holds its count, the effect is the same as setting TR1 = 1. Timer0 in Mode 3 enables TL0 and TH0 as two separate 8-bits counters. TL0 uses the Timer0 control bits such like C/T, GATE, TR0, INT0 and TF0. TH0 is locked into a timer function (can not be external event counter) and take over the use of TR1, TF1 from Timer1. TH0 now controls the Timer1 interrupt.



TIMER2

Timer2 is a 16-bits timer/counter which can operate as either an event timer or an event counter as selected by **C/I/T2** in the special function register **T2CON**. Timer2 has four operation modes:Capture Mode(CP), Auto-Reload Up/Down Mode(ARUD), Auto-Reload Up-Only mode(ARUO) and Baud-Rate Generator Mode(BRG).

Logical OR (RCLK, TCLK)	CP/RL2	TR2	DCEN	Mode
x	x	0	x	OFF
1	x	1	0	Baud-Rate Generation
0	1	1	0	Capture
0	0	1	0	Auto-Reload Up-only
0	0	1	1	Auto-Reload Up/Down

Timer2 Mode Table

Timer2 is also can be configured as a periodical signal generator.

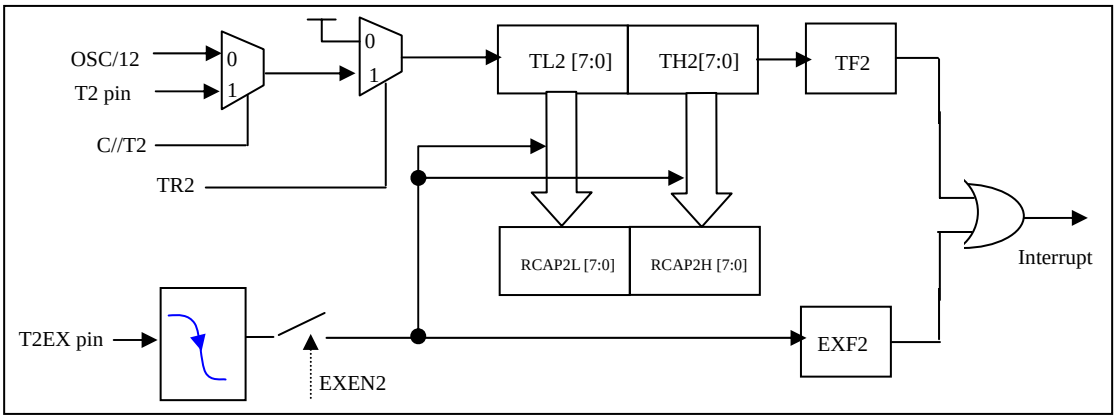
The MPC89x51A is able to generate a programmable clock output on P1.0. When T2OE bits is set and C//T2 bits is cleared, Timer2 overflow pulse will generate a 50% duty clock and output that to P1.0. The frequency of clock-out is calculated according to the following formula.

$$\frac{\text{Oscillator frequency}}{\text{4 x (65536 – RCAP2H, RCAP2L)}}$$

In the clock-out mode, Timer2 rollover will not generate an interrupt.

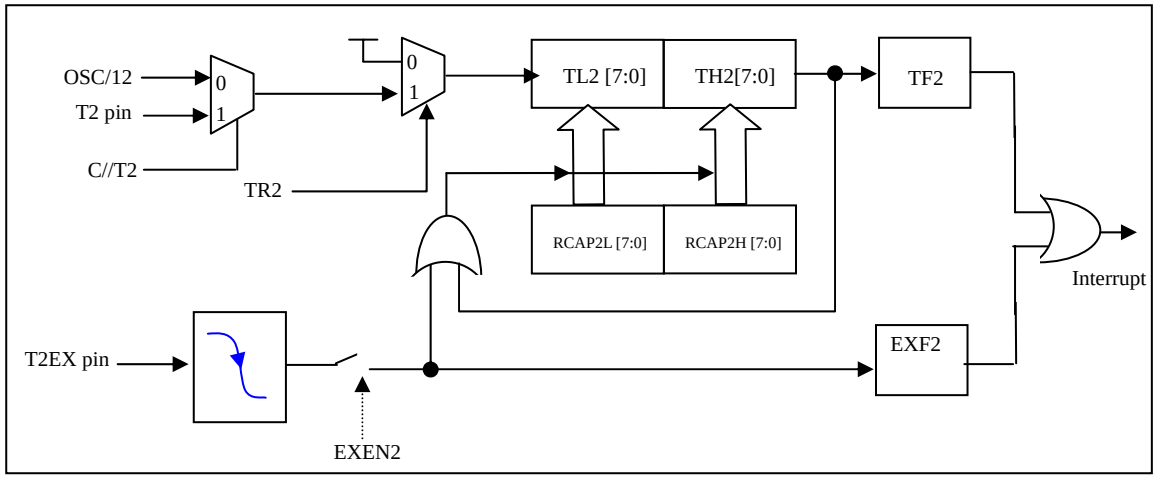
Capture Mode (CP)

In the Capture mode, Timer2 is incremented by either OSC/12 or external pin (T2) 1-to-0 transition. TR2 controls the event to timer2, and a 1-to-0 transition on T2EX pin will trigger RCAP2H and RCAP2L registers to capture the Timer2 contents onto them if EXEN2 is set. An overflow in Timer2 sets TF2 flag and a 1-to-0 transition in T2EX pin sets EXF2 flag if EXEN2=1. TF2 and EXF2 is Ored to request the interrupt service.



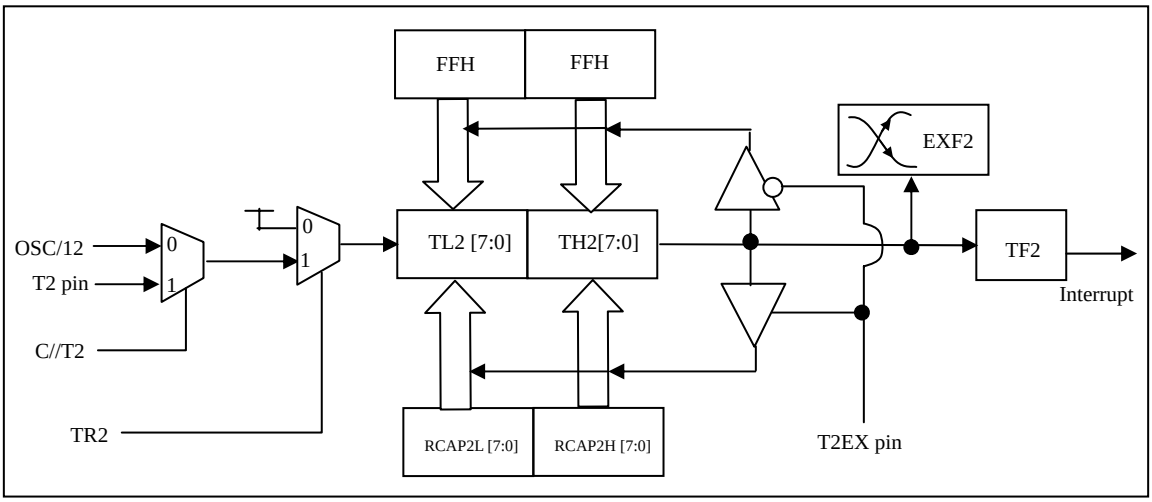
Auto-Reload Up-Only Mode (ARUO)

In ARUO mode, Timer2 can be configured to count up with a software-defined value to be reloaded. When reset is applied to the DCEN =0 and CP/RL2=0, Timer2 is at ARUO mode. An overflow on Timer2 or 1-to-0 transition on T2EX pin will load RCAP2H and RCAP2L contents onto Timer2, also set TF2 and EXF2, respectively.



Auto-Reload Up-Down Mode (ARUD)

In ARUD mode, Timer2 can be configured to count up or down. When DCEN =1 and CP/RL2=0, Timer2 is at ARUD mode. The counting direction is determined by T2EX pin. If T2EX=**1**, counting up; otherwise, counting down. An overflow on Timer2 will set TF2 and toggle EXF2. EXF2 cannot generate interrupt request in this mode. If the counting direction is DOWN, the overflow loads 0xFFFF onto Timer2, and if counting direction is UP, the overflow loads RCAP2H, RCAP2L contents onto Timer2.



Baud-Rate Generator Mode (BRG)

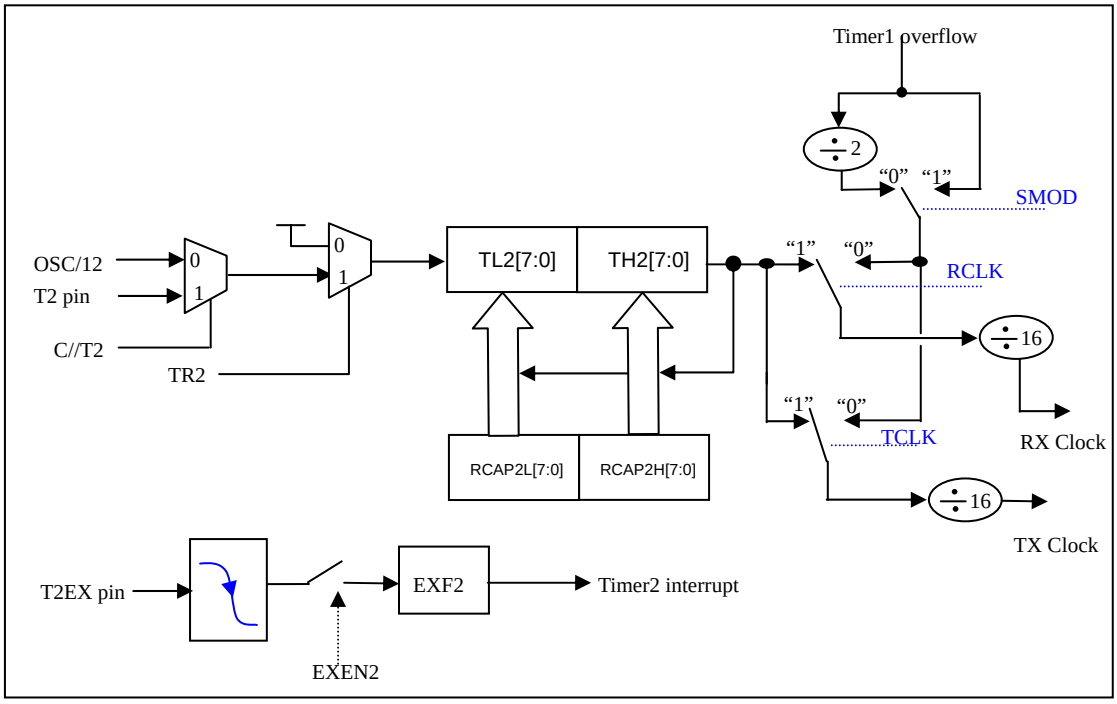
Timer2 can be configured to generate various baud-rate. Bits TCLK and/or RCLK in T2CON allow the serial port transmit and receive baud rates to be derived from either Timer1 or Timer2. When TCLK=0, Timer1 is used as the serial port transmit baud rate generator. When TCLK=1, Timer2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated from Timer1 and the other from Timer2.

In BRG mode, Timers is operated very like auto-reload up-only mode except that the T2EX pin cannot control reload. An overflow on Timer2 will load RCAP2H, RCAP2L contents onto Timer2, but TF2 will not be set. A 1-to-0 transition on P2EX pin can set EXF2 to request interrupt service if EXEN2=1.

The baud rate in UART Mode1 and Mode3 are determined by Timer2's overflow rate given below:

$$\text{Baud Rate} = \frac{\text{Timer2 overflow rate}}{16} \quad \text{(counting T2EX)}$$

$$\text{Baud Rate} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H, RCAP2L})\ ]\ ]} \quad \text{(as a timer)}$$



Interrupt

There are eight interrupt sources available in MPC89x51A. Each interrupt source can be individually enabled or disabled by setting or clearing a bits in the SFR named **IE**. This register also contains a global disable bits (**EA**), which can be cleared to disable all interrupts at once.

Each interrupt source has two corresponding bits to represent its priority. One is located in SFR named **IPH** and the other in **IP/XICON** register. Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. The following table shows the internal polling sequence in the same priority level and the interrupt vector address.

Source	Vector address	Priority within level
External interrupt 0	03H	1 (highest)
Timer 0	0BH	2
External interrupt 1	13H	3
Timer1	1BH	4
Serial Port	23H	5
Timer2	2BH	6
External interrupt 2	33H	7
External interrupt 3	3BH	8

The external interrupt /INT0, /INT1, /INT2 and /INT3 each can be either level-activated or transition-activated, depending on bits**IT0** and **IT1** in SFR **TCON**, **IT2** and **IT3** and **XICON**. The flags that actually generate these interrupts are bits**IE0** and **IE1** in **TCON**, **IE2** and **IE3** in **XICON**. When an external interrupt is generated, the flag that generated it is cleared by the hardware. When the service routine is vectored *only if the interrupt was transition –activated*, and then the external requesting source controls the request flag, rather than the on-chip hardware.

The Timer0 and Timer1 interrupts are generated by **TF0** and **TF1**, which are set by a rollover in their respective Timer/Counter registers in most cases. When a timer interrupt is generated, the flag, which generated it, is cleared by the on-chip hardware as soon as the service routine is vectored to.

The serial port interrupt is generated by the logical *OR* of **RI** and **TI**. Neither of these flags is cleared by hardware when the service routine is vectored to. The service routine should poll **RI** and **TI** to determine which one to request service and it will be cleared by software.

The timer2 interrupt is generated by the logical *OR* of **TF2** and **EXF2**. Just the same as serial port, neither of these flags is cleared by hardware when the service routine is vectored to.

All of the bits that generate interrupts can be set or cleared by software, and it has the same

impact as done through by hardware. In other words, interrupts or pending interrupts can be generated or canceled in software.

The following content describes several SFR related to interrupt mechanism.

SFR: **IE *(***Interrupt Enabling***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
EA		**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

EA: Global disables all interrupts when cleared.

ET2: When set, enables Timer2 interrupt.

ES: When set, enables the serial port interrupt.

ET1: When set, enables Timer1 interrupt.

EX1: When set, enables external interrupt 1.

ET0: When set, enables Timer 0 interrupt.

EX0: When set, enables external interrupt 0.

SFR: **IP *(***Interrupt Priority Low***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
-	**-**	**PT2**	**PS**	**PT1**	**PX1**	**PT0**	**PX0**

PT2: If set, Set priority for timer2 interrupt higher

PS: If set, Set priority for serial port interrupt higher

PT1: If set, Set priority for timer1 interrupt higher

PX1: If set, Set priority for external interrupt 1 higher

PT0: If set, Set priority for timer0 interrupt higher

PX0: If set, Set priority for external interrupt 0 higher

SFR: **IPH *(***Interrupt Priority High***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
PX3H	**PX2H**	**PT2H**	**PSH**	**PT1H**	**PX1H**	**PT0H**	**PX0H**

PX3H: If set, Set priority for external interrupt 3 highest

PX2H: If set, Set priority for external interrupt 2 highest

PT2H: If set, Set priority for timer2 interrupt highest

PSH: If set, Set priority for serial port interrupt highest

PT1H: If set, Set priority for timer1 interrupt highest

PX1H: If set, Set priority for external interrupt 1 highest

PT0H: If set, Set priority for timer0 interrupt highest

PX0H: If set, Set priority for external interrupt 0 highest

IP (or XICON) and IPH are combined to form 4-level priority interrupt as the following table.

{IPH.x , IP.x}	Priority Level
11	1 (highest)
10	2
01	3
00	4

SFR: **XICON (**External Interrupt Control**):**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
PX3	**EX3**	**IE3**	**IT3**	**PX2**	**EX2**	**IE2**	**IT2**

PX3: If set, Set priority for external interrupt 3 higher

EX3: If set, Enables external interrupt 3.

IE3: Interrupt 3 Edge flag. Sets by hardware when external interrupt edge detected. Cleared when interrupt processed.

IT3: Interrupt 3 type control bits. Set/Cleared by software to specified falling edge/low level triggered interrupt.

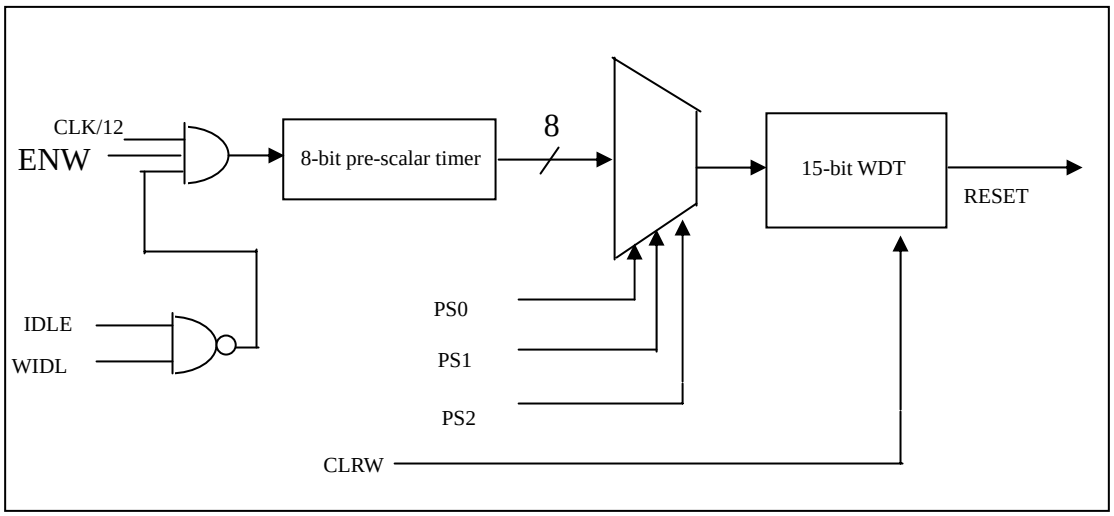
PX2: If set, Set priority for external interrupt 3 higher

EX2: If set, enables external interrupt 2.

IE2: Interrupt 2 Edge flag. Sets by hardware when external interrupt edge detected. Cleared when interrupt processed.

IT2: Interrupt 2 types control bits. Set/Cleared by software to specify falling edge/low level triggered interrupt.

Watchdog Timer



SFR: **WDTCR (**Watchdog Timer Control**):**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
-	**-**	**ENW**	**CLRW**	**WIDL**	**PS2**	**PS1**	**PS0**

ENW: Enable WDT while it is set. ENW cannot be cleared by firmware.
1: = enable watchdog timer, 0: = does not use watchdog timer

CLRW: Clear WDT to recount while it is set. Hardware will automatically clear this bits.

WIDL: Set this bits to disable WDT generating reset even though the μC is in idle mode.

{PS2, PS1, PS0}: select the pre-scalar output.
{*0, 0, 0*}: = set the pre-scaling value 2
{*0, 0, 1*}: = set the pre-scaling value 4
{*0, 1, 0*}: = set the pre-scaling value 8
{*0, 1, 1*}: = set the pre-scaling value 16
{1, *0, 0*}: = set the pre-scaling value 32
{*1, 0, 1*}: = set the pre-scaling value 64
{*1, 1, 0*}: = set the pre-scaling value 128
{*1, 1, 1*}: = set the pre-scaling value 256

Serial IO Port (UART)

The serial port of MPC89x51A is duplex. It can transmit and receive simultaneously. The receiving and transmitting of the serial port share the same SFR **SBUF**, but actually there are two SBUF registers implemented in the chip, one is for transmitting and the other is for receiving. The serial port can be operated in 4 different modes.

Mode 0

Generally, this mode purely is used to extend the I/O features of this device.

Operating under this mode, the device receives the serial data or transmits the serial data via pin RXD, while there is a clock stream shifted via pin TXD which makes convenient for external synchronization. An 8-bits data is serially transmitted/received with LSB first. The baud rate is fixed at 1/12 the oscillator frequency.

Mode1

A 10-bitsdata is serially transmitted through TXD or received through RXD. The frame data includes a start bits (*0*), 8 data bits and a stop bits (*1*). After the receiving, the device will keep the stop bits in **RB8** which from SRF **SCON**.

$$\textbf{Baud Rate (for Mode 1)} = \frac{2^{\textbf{SMOD}}}{32} \times \textbf{(Timer-1 overflow rate)}$$

$$\text{or} = \frac{\textbf{(Timer-2 overflow rate)}}{16}$$

Mode2

An 11-bits data is serially transmitted through **TXD** or received through **RXD**. The frame data includes a start bits (*0*), 8 data bits, a programmable 9th bits and a stop bits (1). On transmit, the 9th data bits comes from **TB8** in SFR **SCON**. On receive, the 9th data bits goes into **RB8** in **SCON**. The baud rate is programmable, and permitted to be set either 1/32 or 1/64 the oscillator frequency.

$$\text{Baud Rate (for Mode 2)} = \frac{2^{\text{SMOD}}}{64} \times F_{osc}$$

Mode3

Mode 3 is the same as mode 2 except the baud rate is variable.

$$\text{Baud Rate (for Mode 3)} = \frac{2^{\text{SMOD}}}{32} \times \text{(Timer-1 overflow rate)}$$

$$\text{or} = \frac{\text{(Timer-2 overflow rate)}}{16}$$

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in mode 0 by the condition **RI** = *0* and **REN** = *1*. Reception is initiated in the other modes by the incoming start bits with *1*-to-*0* transition if **REN**=*1*.

There are several SFR related to serial port configuration described as following.

SFR: **SCON** ***(***Serial Port Control***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
SM0/FE	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

FE: Frame Error bits. This bits is set by the receiver when an invalid stop bits is detected. The FE bits is not cleared by valid frames, but should be cleared by software. The **SMOD0 (PCON.6)** bits must be set to enable access to the FE bits.

{ SM0, **SM1 }**: Used to set operating mode of the serial port. It is enabled to access by clearing SMOD0.

{ *0, 0* } := set the serial port operate under Mode 0
{ *0, 1* } := set the serial port operate under Mode 1
{ *1, 0* } := set the serial port operate under Mode 2
{ *1, 1* } := set the serial port operate under Mode 3

SM2: Enable the *automatic address recognition* feature in mode 2 and 3. If **SM2**=*1*, **RI** will not be set unless the received 9th data bits is 1, indicating an address, and the received bytes is a Given or Broadcast address. In mode1, if SM2=1 then RI will not be set unless a valid stop Bits was received, and the received bytes is a Given or Broadcast address.

REN: Enable the serial port reception. *1* := enable *0* := disable

TB8: The 9th data bits, which will be transmitted in Mode 2 and Mode 3.

RB8: In mode 2 and 3, the received 9th data bits will go into this bits.

TI: Transmit interrupt flag. After a transmit has been finished, the hardware will set this bits.

RI: Receive interrupt flag. After reception has been finished, the hardware will set this bits.

SFR: **SBUF** ***(***Serial port Buffer register***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
(data to be transmitted or received data)							

Automatic Address Recognition

There is an extra feature makes the device convenient to act as a master, which communicates to multiple slaves simultaneously. It is really *Automatic Address Recognition*.

There are two SFR **SADDR** and **SADEN** implemented in the device. The user can read or write both of them. Finally, the hardware will make use of these two SFR to "generate" a "compared bytes". The formula specifies as following.

Bit[*i*] of **Compared Byte** = (**SADEN[** *i* **] == 1**)? **SADDR**[*i*] **:** ***x***

For example:

Set **SADDR** = 11000000b
Set **SADEN** = 11111101b
⇨ The achieved "Compared Bytes" will be "110000x0" (*x* means don't care)

For another example:

Set **SADDR** = 11100000b
Set **SADEN** = 11111010b
⇨ The achieved "Compared Bytes" will be "11100x0x"

After the generic "Compared Bytes" has been worked out, the MPC89x51A will make use of this bytes to determine how to set the bits **RI** in SFR **SCON**.

Normally, an UART will set bits **RI** whenever it has done a bytes reception; but for the UART in the MPC89x51A, if the bits **SM2** is set, it will set **RI** according to the following formula.

RI = (SM2 == *1*) && (SBUF == *Compared Byte*) && (RB8 == *1*)

In other words, not all data reception will respond to RI, while specific data does.
By setting the SADDR and the SADEN, the user can filter out those data bytes that doesn't like to care. This feature brings great help to reduce software overhead.

The above feature adapts to the serial port when operated in Mode1, Mode2, and Mode3.
Dealing with Mode 0, the user can ignore it.

Frame Error Detection

A missing bits in stop bits will set the **FE** bits in the **SCON** register. The **FE** bits shares the **SCON** bits 7 with **SM0** and its actual function for **SCON.7** is determined by **SMOD0** (**PCON.6**). If **SMOD0** is set, **SCON.7** functions as **FE**, otherwise functions as **SM0**. When used as **FE** bits, it can only be cleared by software.

Reset

The RESET pin is used to reset this device. It is connected into the device to a Schmitt Trigger buffer to get excellent noise immunity.

Any positive pulse from RESET pin must be kept at least two-machine cycle, or the device cannot be reset.

Power Saving Mode and POF

There are two power saving modes which are selectable to drive the MPC89x51A to enter power-saving mode.

1. IDLE mode

The user can set the bits **PCON.0** to drive this chip entering IDLE mode.
In the IDLE mode, the internal clock is gated off to the CPU, but not to the interrupt, timer and serial port functions.

There are two ways to terminate the idle. Activation of any enabled interrupt will cause **PCON.0** to be cleared by hardware to terminating the idle mode. The interrupt will be serviced and following RETI, the next instruction to be executed will be performed right after the instruction that causes the device entering the idle mode. Another way to wake-up from idle is to pull **RESET** pin high to generate internal hardware reset.

2. POWER-DOWN mode

The user can set the bits **PCON.1** to drive this chip entering *POWER-DOWN* mode.

In the *POWER-DOWN* mode, the on-chip oscillator is stopped. The contents of on-chip RAM and SFRs are maintained.

The power-down mode can be woken-up by either hardware reset or **/INT0**, **/INT1**, **/INT2** and **/INT3** external interrupts. When it is woken-up by **RESET** pin, the program will execute from the address 0x0000, and be carefully to keep **RESET** pin active for at least 10ms in order to get a stable clock while waking up this chip from *POWER-DOWN* mode. If it is woken-up from I/O, the program will jump to related interrupt service routine. To use I/O wake-up, interrupt-related registers have to be programmed accurately before power-down is entered. ***Pay attention to add at least one "NOP" instruction subsequent to the power-down instruction if I/O waken-up is used.***

Mode	Program Memory	ALE	PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Float	Data	Data	Data

Pin Status in IDLE Mode and POWER-DOWN Mode

3. POWER-ON FLAG (POF)

The register bits in PCON.4 is set only by power-on action. System RESET from watch-dog-timer, software RESET and RESET pin can not set this bits. It can be cleared by firmware.

In System Programming (ISP)

To develop a good program for ISP function, the user has to understand the architecture of the embedded flash.

The embedded flash consists of 30 pages. Each page contains 512 bytes.

Dealing with flash, the user must erase it in page unit before writing (programming) data into it. Erasing flash means setting the content of that flash as *FF*h. Two erase modes are available in this chip. One is *mass mode* and the other is *page mode*. The *mass mode* gets more performance, but it erases the entire flash. The page mode is something performance less, but it is flexible since it erases flash in page unit.

Unlike RAM's real-time operation, to erase flash or to write (program) flash often takes longer time to finish.

Furthermore, it is a quite complex timing procedure to erase/program flash. Fortunately, the

MPC89x51A carried with convenient mechanism to help the user read/change the flash content. Just filling the target address and data into several SFR, and triggering the built-in ISP automation, the user can easily erase, read, and program the embedded flash and option registers **OR1**.

There are several SFR designed to help the user implement the ISP functionality.

SFR: **IFD** ***(***ISP Flash Data register***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
(Data to be written into flash, or data got from flash)							

IFD is the data port register for ISP operation. The data in IFD will be written into the desired address in operating ISP write and it is the data window of readout in operating ISP read.

SFR: **IFADRH** ***(***ISP Flash Address High***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
(High bytes of the address pointing to flash memory)							

IFADRH is the high-bytes address port for all ISP modes.

SFR: **IFADRL** ***(***ISP Flash Address Low***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
(Low bytes of the address pointing to flash memory)							

IFADRL is the low-bytes address port for all ISP modes.

SFR: **IFMT** ***(***ISP Flash Mode Table***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
reserved					**Mode Selection**		

Mode Selection			To Operate
0	*0*	*0*	Standby
0	*0*	*1*	AP-memory read
0	*1*	*0*	AP-memory/Data-flash program
0	*1*	*1*	AP-memory/Data-flash page erase
1	*1*	*1*	OR1 memory erase (IFADRL[0]=1).
1	*0*	*1*	OR1 memory read (IFADRL[0] =1)
1	*1*	*0*	OR1 memory program (IFADRL[0] = 1)

Note: **OR0** cannot be changed by ISP operation. It can be accessed only by Writer. Only **OR1** can be changed by ISP program.

SFR: **SCMD** ***(***Sequential Command Data register for ISP***) :***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
ISP-Command (Device ID)							

SCMD is the command port for triggering ISP activity. If SCMD is filled with sequential *46*h, *B9*h and if ISPCR.7 = 1, ISP activity will be triggered.
When this register is read, the device ID of MPC89x51A will be returned (2 bytes). The MSB bytes of DID is ***F0***h and LSB bytes ***01***h. IFADRL[0] is used to select HIGH/LOW bytes of DID.

SFR: **ISPCR *(***ISP Control register***):***

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
ISPEN	**SWBS**	**SWRST**	**-**	**-**	**WAIT**		

ISPEN: ISP function enabling bits
0: = Disable ISP program to change flash
1: = Enable ISP program to change flash

SWBS: Secondary Booting program selecting
0: = Boot from main-memory.
1: = Boot from ISP memory.

SWRST: software reset trigger
0: = No operation
1: = Generate software system reset. It will be cleared by hardware automatically.

***Notice*: Software reset actions could reset other SFR, but it never influences bits ISPEN and SWBS. The ISPEN and SWBS only will be reset by power-up action, not software reset.**

WAIT: Waiting time selection while the flash is busy.

	CPU Wait time (Machine Cycle)			
ISPCR[2:0]	Page Erase	Program	Read	Recommended System clock
0 0 0	43769	240	43	40M
0 0 1	21885	120	22	20M
0 1 0	10942	60	11	10M
0 1 1	5471	30	6	5M

Procedures demonstrating ISP function

```
IFMT  ← xxxxx011b          /* choice page-erasing command */
ISPCR ← 100xx010b          /* set ISPEN=1 to enable flash change.
                              set WAIT=010, 10942 MC; assumed 10M X's*/
IFADRH ← (page address high byte)
IFADRL ← (page address low byte)   /* specify the address of the page to be erased */
SCMD  ← 46h
SCMD  ← B9h                /* trig ISP activity */
(CPU progressing will be hold here )
(CPU continues)
```

Erase a specific flash page

```
IFMT ← xxxxx010 b                    /* choice byte-programming command */
ISPCR ← 100xx010b                    /* set ISPEN=1 to enable flash change.
                                        set WAIT=010, 60 MC; assumed 10M X's*/
IFADRH ← (Address high byte)         /* specify the address to be programmed */
IFADRL ← (Address low byte)
IFD ← (byte date to be written into flash)   /* prepare data source */
SCMD ← 46h                           /* trig ISP activity */
SCMD ← B9h
(CPU progressing will be hold here)
(CPU continues)
```

Program a byte into flash

```
IFMT ← xxxxx001 b                    /* choice byte-read command */
ISPCR ← 100xx010b                    /* set ISPEN=1 to enable flash change.
                                        set WAIT=010, 11 MC; assumed 10M X's*/
IFADRH ← (Address high byte)         /* specify the address to be read */
IFADRL ← (Address low byte)
SCMD ← 46h                           /* trig ISP activity */
SCMD ← B9h
(CPU progressing will be hold here)
(CPU continues and currently IFD contain the desired data byte )
```

Read a byte from flash

Booting Program Entrance

The MPC89x51A boots according to the following rule.

```
If  ( HWBS == 0 )  &&  ( { ISPAS1, ISPAS0} ≠ { 1, 1 })
        System will boot from ISP program
else
        System will boot from normal AP program
```

Above rule is adaptive only for power-up procedure, not software reset.

Switching from ISP program to AP program

The device permits the user normally start running the AP program as soon as the ISP program has finished updating the flash content. Just program an instruction at the tail of ISP program as

```
ISPCR ← 001xxxxxb
```

which disables flash-writing authority, set **SWBS** *0*, and trigger a software reset. After that, the system will be reset (not powered-up), and the system will refer to **SWBS** to startup from AP program entrance. For power-up procedure, the **HWBS** will be referred to decide the program entrance, but for software reset, **SWBS** will be referred.

Switch to the ISP program from AP program

The device also permits the user program switches directly to the ISP program. Just program an instruction in the AP program as

```
ISPCR ← x11xxxxx_b
```

which sets **SWBS** *1* to direct the device boot from AP program, and trigger a software reset. After that, the system will be reset (not powered-up), and the system will refer to **SWBS** to startup from ISP program entrance.

In-Application Program

The In-Application Program feature is designed for user to Read/Write nonvolatile *data flash*. It may bring great help to store parameters those should be independent of power-up and power-done action. In other words, the user can store data in *data flash* memory, and after shutting down the MCU and rebooting the MCU, user still can get the original value which had stored in.

The user can program the *data flash* according to the same way as ISP program, and gets deeper understanding related to SFR **IFD, IFADRL, IFADRH, IFMT, SCMD, and ISPCR**.

The *data flash* can be programmed by the AP program as well as the ISP program.

The ISP program may program the AP memory and *data flash*, while the AP program may program the *data flash* but not the ISP memory. If the AP program desires to change the ISP memory associated with specific address space, the hardware will ignore it.

Note : Even the users do not need ISP space, the OR0[5:4] still needs to be programmed with {10} if IAP data flash is desired. In other words, the maximum available size in data flash for IAP operation is 10K bytes.

Note for Other SFR

SFR: **AUXR**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
-	**-**	**-**	**-**	**-**	**-**	**ERAM**	**AO**

ERAM: Define if hide the expanded RAM, so to access to the external RAM
0: = The internal auxiliary RAM access is enabled
1: =The internal auxiliary RAM access is disabled. The MOVX instructions always direct to external RAM.

AO: *0*: = ALE is emitted at a constant rate of 1/6 the oscillator frequency for 12T mode, and at a constant rate of 1/3 the oscillator frequency for 6T mode
1: = ALE is active only during access to external memory for both MOVC and MOVX

SFR: **AUXR1**

Bits-7	Bits-6	Bits-5	Bits-4	Bits-3	Bits-2	Bits-1	Bits-0
-	**-**	**-**	**-**	**GF2**	**-**	**-**	**DPS**

GF2: General purpose flag
DPS: Data pointer switch
0: = Make the data pointer-0 active
1: = Make the data pointer-1 active

Absolute Maximum Rating (MPC89E51A)

Parameter	Rating	Unit
Ambient temperature under bias	-55 ~ +125	℃
Storage temperature	-65 ~ + 150	℃
Voltage on any Port I/O Pin or RST with respect to Ground	-0.5 ~ VCC + 0.5	V
Voltage on VCC with respect to Ground	-0.5 ~ +6.0	V
Maximum total current through VCC and Ground	500	mA
Maximum output current sunk by any Port pin	40	mA

*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (MPC89E51A)

VSS = 0V, TA = 25 ℃ and 12 clocks per machine cycle ,unless otherwise specified

Symbol	Parameter	Test Condition	Specification			Unit
			Min.	Typ.	Max.	
V_{IL1}	Input low voltage (P0, 1,2,3,4)	Vcc=5.0V			0.8	V
V_{IL2}	Input low voltage **(RESET)**	Vcc=5.0V			1.6	V
V_{IH1}	Input high voltage (P0, 1, 2, 3, 4,EA)	Vcc =5.0V	2.0			V
V_{IH2}	Input high voltage **(RESET)**	Vcc=5.0V	3.0			V
I_{OL1}	Sinking Current for output Low (P1, P2, P3, P4)	Vcc=5.0V	4	6		mA
I_{OL2}	Sinking Current for output Low (P0, ALE, PSEN)	Vcc=5.0V	8	12		mA
I_{OH1}	Sourcing Current for output High (P1, P2, P3, P4)	Vcc = 5.0V	150	220		uA
I_{OH2}	Sourcing Current for output High (ALE, PSEN)	Vcc = 5.0V	14	20		mA
I_{IL}	Logic 0 input current (P1,2,3,4)	Vpin=0V		18	50	uA
I_{TL}	Logic 1 to 0 transition current (P1,2,3,4)	Vpin=2.0V		270	600	uA
I_{CC}	Operating current @20MHz	Vcc=5.0V			30	mA
I_{IDLE}	Idle mode current @ 20MHz	Vcc=5.0V			7	mA
I_{PD}	Power down current	Vcc=5.0V			50	uA
Rrst	Internal pull-down resistance in **RESET**		45K~116K			ohm

Absolute Maximum Rating (MPC89L51A)

Parameter	Rating	Unit
Ambient temperature under bias	-55 ~ +125	℃
Storage temperature	-65 ~ + 150	℃
Voltage on any Port I/O Pin or RST with respect to Ground	-0.3 ~ VCC + 0.3	V
Voltage on VCC with respect to Ground	-0.3 ~ +4.2	V
Maximum total current through VCC and Ground	500	mA
Maximum output current sunk by any Port pin	40	mA

*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

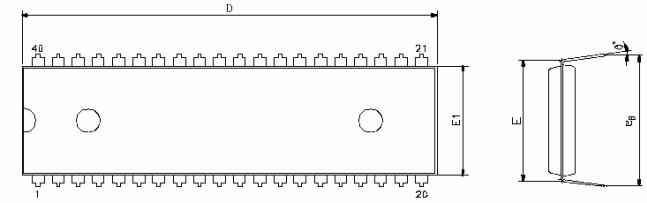
DC Characteristics (MPC89L51A)

VSS = 0V, TA = 25 ℃ and 12 clocks per machine cycle ,unless otherwise specified

Symbol	Parameter	Test Condition	Specification			Unit
			Min.	Typ.	Max.	
V_{IL1}	Input low voltage (P0, 1,2,3,4)	Vcc=3.3V			0.8	V
V_{IL2}	Input low voltage **(RESET)**	Vcc=3.3V			1.5	V
V_{IH1}	Input high voltage (P0, 1, 2, 3, 4,EA)	Vcc =3.3V	2.0			V
V_{IH2}	Input high voltage **(RESET)**	Vcc=3.3V	3.0			V
I_{OL1}	Sinking Current for output Low (P1, P2, P3, P4)	Vcc=3.3V	2.5	4		mA
I_{OL2}	Sinking Current for output Low (P0, ALE, PSEN)	Vcc=3.3V	5	8		mA
I_{OH1}	Sourcing Current for output High (P1, P2, P3, P4)	Vcc = 3.3V	40	70		uA
I_{OH2}	Sourcing Current for output High (ALE, PSEN)	Vcc =3.3V	8	13		mA
I_{IL}	Logic 0 input current (P1,2,3,4)	Vpin=0V		8	50	uA
I_{TL}	Logic 1 to 0 transition current (P1,2,3,4)	Vpin=2.0V		110	600	uA
I_{CC}	Operating current @20MHz	Vcc=3.3V			30	mA
I_{IDLE}	Idle mode current @ 20MHz	Vcc=3.3V			6	mA
I_{PD}	Power down current	Vcc=3.3V			50	uA
Rrst	Internal pull-down resistance in **RESET**		45K~116K			ohm

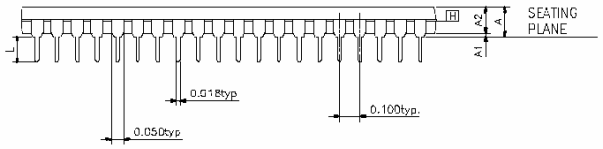
Package Dimension

40-pin PDIP (MPC89x51AE)



Symbols	MIN		NOR		MAX	
A					0.220	5.59
A1	0.015	0.38				
A2	0.150	3.81	0.155	3.94	0.160	4.06
D	2.055	52.20	2.060	52.32	2.070	52.58
E			0.600	15.24	SBC	
E1	0.540	13.72	0.545	13.84	0.550	13.97
L	0.115	2.92	0.130	3.30	0.150	3.81
E8	0.630	16.00	0.650	16.51	0.670	17.02
θ°	0	0	7	7	15	15

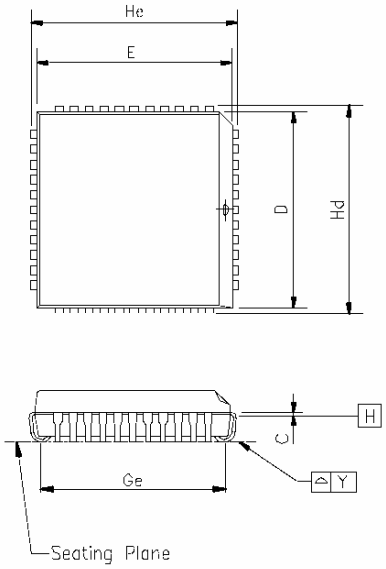
Inch/mm



NOTE:
1.JEDEC OUTLINE : MS-011 AC

旺宏科技股份有限公司 Megawin Technology Co.,			
3RD. ANGLE SYS.	比例 SCALE:	材質 MTRL:	製程 FINISH:	數量 QTY:
繪圖: DWN: 日期: DATE:	圖名: TITLE: DUAL INLINE PLASTIC DATA SHEET P-DIP 40 LEADS (600mil)			
審核: CHK: 日期: DATE:	圖號: DWG#: J1-0140P-001			
核准: APPL: 日期: DATE:	檔名: FILE: J1-0140P-001-01	版別: DATE: 01	張數: DATE: 1	

44-pin PLCC (MPC89x51AP)



Symbols	MIN		NOR		MAX	
A					0.185	4.70
A1	0.020	0.51				
A2	0.145	3.68	0.150	3.81	0.155	3.94
b1	0.026	0.66	0.028	0.71	0.032	0.81
b	0.016	0.41	0.018	0.46	0.022	0.56
c	0.007	0.18	0.010	0.25	0.013	0.33
D	0.648	16.46	0.653	16.59	0.658	16.71
E	0.648	16.46	0.653	16.59	0.658	16.71
e			0.050	1.27	BSC	
Gd	0.590	14.99	0.610	15.49	0.630	16.00
Ge	0.590	14.99	0.610	15.49	0.630	16.00
Hd	0.680	17.27	0.690	17.53	0.700	17.78
He	0.680	17.27	0.690	17.53	0.700	17.78
L	0.090	2.29	0.100	2.54	0.110	2.79
Y					0.004	0.10

Inch/mm

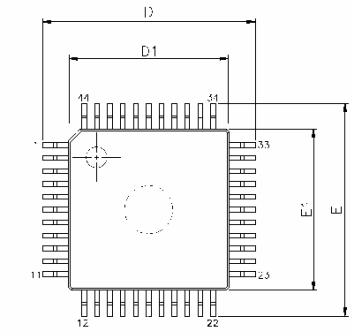
* *NOTE:*

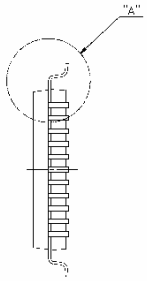
1. JEDEC OUTLINE : MO-047 AC
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY
3. DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION .

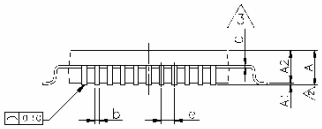
旺泉科技股份有限公司
Megawin Technology Co.,

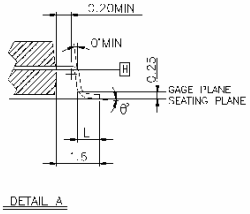
3RD ANGLE SYS	比例 SCALE	材質 MTRL	製程 FINISH	數量 QTY
繪圖 DWN 日期 DATE	圖名: PLASTIC CHIP CARRIER DATA SHEET 44 LEADS 0.05" LEAD SPACING SQUARE			
審核 CHK 日期 DATE	圖號: J1-06044-001			
核准 APPD 日期 DATE	檔名: J-044P-1	版次 REV: 02	張次 SHT: 1	

44-pin PQFP (MPC89x51AF)









DETAIL A

Symbols	MIN		NOR		MAX	
A					0.106	2.70
A1	0.010	0.25	0.012	0.30	0.014	0.35
A2	0.075	1.90	0.079	2.00	0.087	2.20
b			0.012	0.30	(TYP.)	
D	0.512	13.00	0.520	13.20	0.528	13.4
D1	0.390	9.90	0.394	10.00	0.398	10.10
E	0.512	13.00	0.520	13.20	0.528	13.40
E1	0.390	9.90	0.394	10.00	0.398	10.10
L	0.029	0.73	0.035	0.88	0.037	0.93
e			0.031	0.80	(TYP.)	
θ°	0	0			7	7
C	0.004	0.10	0.006	0.15	0.008	0.2

Inch/mm

NOTES:

1.JEDEC OUTLINE:MO-108 AA-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

笙泉科技股份有限公司 Megawin Technology Co.,			
ANGLE ±2°	比例 SCALE	材質 MTRL	製程 FINISH	數量 QTY
繪圖: DRAWN 日期: DATE	圖名: TITLE: METRIC PLASTIC QUAD FLAT PACKAGE OUTLINE 10x10MM BODY 44L DATA SHEET		
審核: CHK 日期: DATE	圖號: DWG# J1-0344Q-001		
核定: APPR 日期: DATE	檔名: FILE J-QFP44	版別: REV 03	張數: QTY 1

Revision History

Version	Date	Page	Description
A3	2004/10		- reorganized
A4	2004/11	P27	- Added Procedures demonstrating ISP function
A5	2005/01		- Re-Format - Mark the reset pin resistance - Remove the read-only limitation on SFR AUXR - Document on option register OR1.7 - Fix the Baud-Rate-Computing formula for Timer-1
A6	2005/3/30	P6	- Update PQFP-44 package shape
A7	2005/6/14	P5, 8, 33	- Modify pin /EA location for PDIP and PLCC package - Modify bits definition for SFR PCON - Absolute Maximum Rating
A8	2006/08	P33, 34	- Revises the possible operating temperature.
A9	2007/03	P34	- Modify the Storage Temperature
A10	2007/12	P2 P34, 35	- Add 2.7V requirement in flash write operation. - Modify Absolute Maximum Rating.
A11	2008/12		- Formatting