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MPC8308 PowerQUICC II Pro Processor Hardware Specification

This document provides an overview of the MPC8308 features and its hardware specifications, including a block diagram showing the major functional components. The MPC8308 is a cost-effective, low-power, highly integrated host processor. The MPC8308 extends the PowerQUICC family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

NOTE

The information provided in this document is preliminary and is based on estimates only and refers to the pre-silicon phase, with no device characterization done. Freescale reserves the right to change the contents of this document as appropriate.

Contents

1. Overview 1
2. Electrical Characteristics 2
3. Power Characteristics 6
4. Clock Input Timing 7
5. RESET Initialization 8
6. DDR2 SDRAM 10
7. DUART 14
8. Ethernet: Three-Speed Ethernet, MII Management . 15
9. USB 22
10. High-Speed Serial Interfaces (HSSI) 24
11. PCI Express 34
12. Enhanced Local Bus 43
13. Enhanced Secure Digital Host Controller (eSDHC) . 47
14. JTAG 53
15. I^2C 56
16. Timers 58
17. GPIO 59
18. IPIC 60
19. SPI 60
20. Package and Pin Listings 62
21. Clocking 75
22. Thermal 79
23. System Design Information 81
24. Ordering Information 85
25. Document Revision History 86

1 Overview

Figure 1 shows the major functional units within the MPC8308. The e300 core in the MPC8308, with its 16 Kbytes of instruction and 16 Kbytes of data cache, implements the Power Architecture user instruction set architecture and provides hardware and software debugging

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support. In addition, the MPC8308 offers a PCI Express controller, two three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSEC), a DDR2 SDRAM memory controller, a SerDes block, an enhanced local bus controller (eLBC), an integrated programmable interrupt controller (IPIC), a general purpose DMA controller, two I^2C controllers, dual UART (DUART), GPIOs, USB, general purpose timers, and an SPI controller. The high level of integration in the MPC8308 helps simplify board design and offers significant bandwidth and performance.

A block diagram of the device is shown in Figure 1.

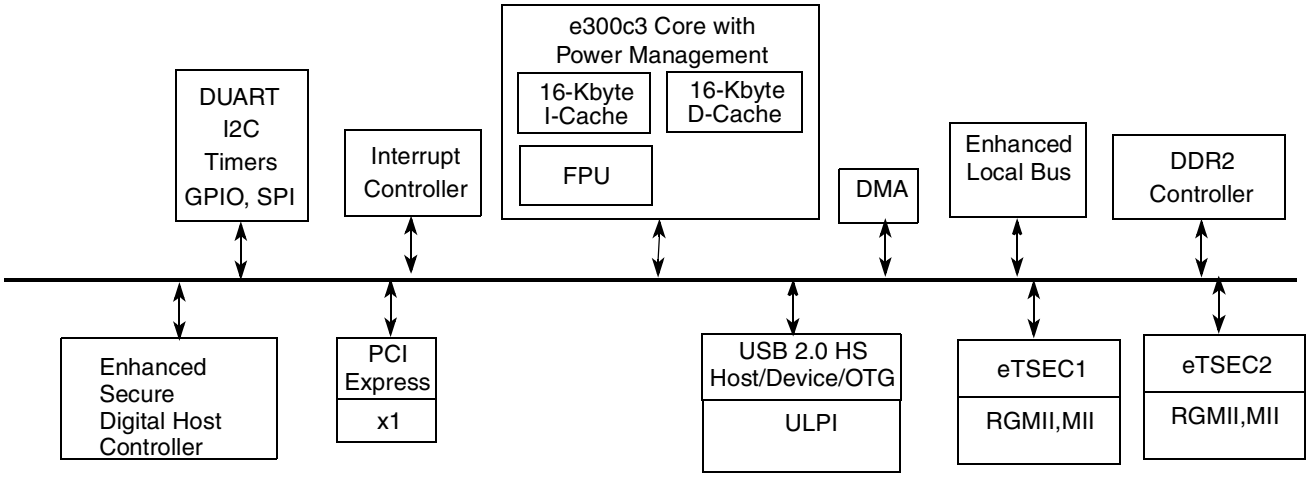


Figure 1. MPC8308 Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8308. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage	AV_{DD1}, AV_{DD2}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 1.9	V	—

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Local bus, DUART, system control and power management, eSDHC, I^2C, USB, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage		NV_{DD}	–0.3 to 3.6	V	7
SERDES PHY		$XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$	–0.3 to 1.26	V	—
eTSEC I/O Voltage		LV_{DD1}, LV_{DD2}	–0.3 to 2.75 or –0.3 to 3.6	V	6,8
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	eTSEC	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5,8
	Local bus, DUART, system control and power management, eSDHC, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage	OV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5,7
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M, L, O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
6. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
7. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH}, NV_{DDP_K} from the ball map.
8. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit
SerDes internal digital power	$XCOREV_{DD}$	1.0 V ± 50 mV	V
SerDes internal digital power	$XCOREV_{SS}$	0.0	V
SerDes I/O digital power	$XPADV_{DD}$	1.0 V ± 50 mV	V
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit
SerDes analog power for PLL	$SDAV_{SS}$	0	V
SerDes I/O digital power	$XPADV_{SS}$	0	V
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V
Analog supply for e300 core APLL	AV_{DD1}	1.0 V ± 50 mV	V
Analog supply for system APLL	AV_{DD2}	1.0 V ± 50 mV	V
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V
Differential reference voltage for DDR controller	MV_{REF}	GVDD/2 (0.49 × GV_{DD} to 0.51 × GV_{DD})	V
Standard I/O voltage (Local bus, DUART, system control and power management, eSDHC, USB, I^2C, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage)[2]	NV_{DD}	3.3 V ± 300 mV	V
eTSEC IO supply[3,4]	LV_{DD1}, LV_{DD2}	2.5 V ± 125 mV 3.3 V ± 300 mV	V
Analog and digital ground	V_{SS}	0.0	V
Junction temperature[5]	T_A/T_J	0 to 105	°C

Notes:

1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. NV_{DD} here refers to NV_{DDA}, NV_{DDB},NV_{DDG}, NV_{DDH} and NV_{DDP_K} from the ball map.
3. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
4. LV_{DD1} here refers to NV_{DDC} and LV_{DD2} refers to NV_{DDF} from the ball map.
5. Minimum temperature is specified with T_A; Maximum temperature is specified with T_J.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the device

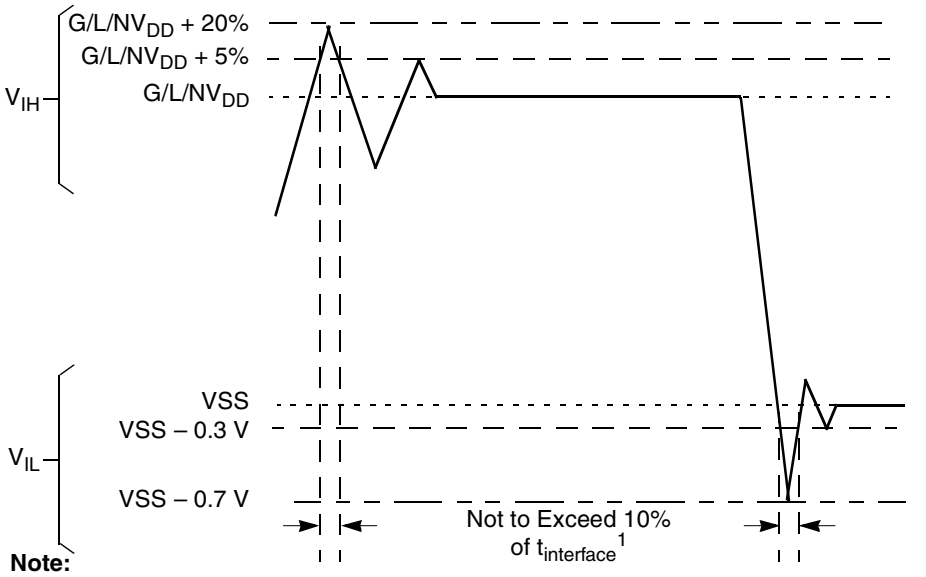


Figure 2. Overshoot/Undershoot Voltage for GVDD/NVDD/LVDD

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Driver Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
DDR2 signals[1]	18	GV_{DD} = 1.8 V
DUART, system control, I^2C, JTAG, eSDHC, GPIO,SPI, USB	42	NV_{DD} = 3.3 V
eTSEC signals	42	LV_{DD} = 2.5/3.3 V

[1] Output Impedance can also be adjusted through configurable options in DDR Control Driver Register (DDRCDR). For more information, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

2.1.4 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and NV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3.

The I/O power supply ramp-up slew rate should be slower than 4V/100 μs; this requirement is for ESD circuit.

Note that there is no specific power-down sequence requirement for the device. I/O voltage supplies (GV_{DD}, LV_{DD}, and NV_{DD}) do not have any ordering requirements with respect to one another.

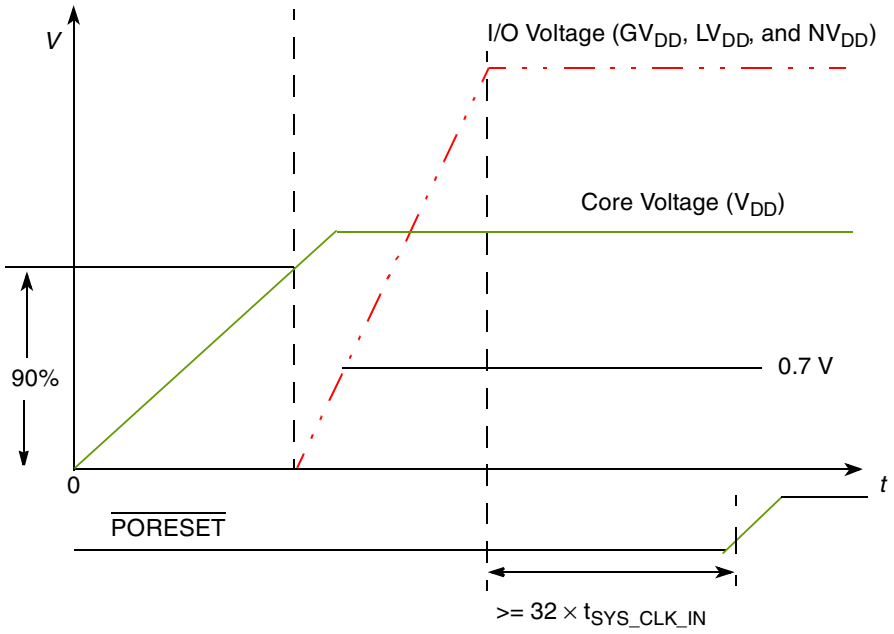


Figure 3. Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power for the device is shown in Table 4. Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8308 Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical[2]	Maximum[3]	Unit
266	133	530	900	mW
333	133	565	950	mW
400	133	600	1000	mW

Notes:

1. The values do not include I/O supply power but do include core (AV_{DD}) and PLL (AV_{DD1}, AV_{DD2}, $XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$)
2. Typical power is based on best process, a voltage of V_{DD} = 1.0V and ambient temperature of T_A = 25° C
3. Maximum power is estimated based on best process, a voltage of V_{DD} = 1.05 V and ambient temperature of T_J = 105° C

Table 5 describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8308 Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	NV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR2 R_s = 22 Ω R_t = 75 Ω	250 MHz 32 bits+ECC 266 MHz 32 bits+ECC	0.302 0.309	—	—	—	W	—
Local bus I/O load = 20 pF	62.5 MHz 66 MHZ	—	0.038 0.040	—	—	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	0.008	—	W	2 controllers
	RGMII, 125 MHz	—	—	0.078	0.044	W	
eSDHC IO Load = 40 pF	50 MHz	—	—	0.008	—	W	—
USB IO Load = 20 pF	60 MHz	—	—	0.012		W	—
Other I/O	—	—	0.017	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the system clock input (SYS_CLK_IN) DC electrical specifications for the device.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ NV_{DD}	I_{IN}	—	±10	μA

Table 7 provides the RTC clock input (RTC_PIT_CLOCK) DC electrical specifications for the device.

Table 7. RTC_PIT_CLOCK DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	3.3V – 400 mV		V
Input low voltage	—	V_{IL}	0	0.4	V

4.2 AC Electrical Characteristics

The primary clock source for the device is SYS_CLK_IN. Table 8 provides the system clock input (SYS_CLK_IN) AC timing specifications for the device.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SYS_CLK_IN frequency	$f_{SYS_CLK_IN}$	24	—	66.67	MHz	1, 6
SYS_CLK_IN period	$t_{SYS_CLK_IN}$	15	—	41.67	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6		1.2	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS_CLK_IN}$	40	—	60	%	3
SYS_CLK_IN Jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system and core must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33 kHz (max rate).

Table 9. RTC_PIT_CLOCK AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RTC_PIT_CLOCK frequency	$f_{RTC_PIT_CLOCK}$	1	32768	—	Hz	—
RTC_PIT_CLOCK rise and fall time	t_{RTCH}, t_{RTCL}	1.5	—	3	µs	—
RTC_PIT_CLOCK duty cycle	$t_{RTCHK}/t_{RTC_PIT_CLOCK}$	45	—	55	%	—

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the device.

5.1 RESET DC Electrical Characteristics

Table 10 provides the DC electrical characteristics for the RESET pins.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$		±5	µA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V

Table 10. RESET Pins DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

5.2 RESET AC Electrical Characteristics

Table 11 provides the reset initialization AC timing specifications.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ (input) to activate reset flow	32	—	$t_{SYS_CLK_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable power and clock applied to SYS_CLK_IN	32	—	$t_{SYS_CLK_IN}$	—
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS_CLK_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of PORESET	4	—	$t_{SYS_CLK_IN}$	—
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	2
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	ns	1, 2

Notes:
1. $t_{SYS_CLK_IN}$ is the clock period of the input clock applied to SYS_CLK_IN
2. POR configuration signals consists of CFG_RESET_SOURCE[0:3]

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
System PLL lock time	—	100	µs	—
e300 core PLL lock time	—	100	µs	—

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 15 provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	µA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 µA current.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8V$.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.45	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.45	—	V	—

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 17. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 1.8± 100 mV

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC @266 MHz	t_{CISKEW}	–875	875	ps	1, 2,3

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ or MECC signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = +/-(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. Memory controller ODT value of 150 Ω is recommended

Figure 4 illustrates the DDR2 input timing diagram showing the t_{DISKEW} timing parameter.

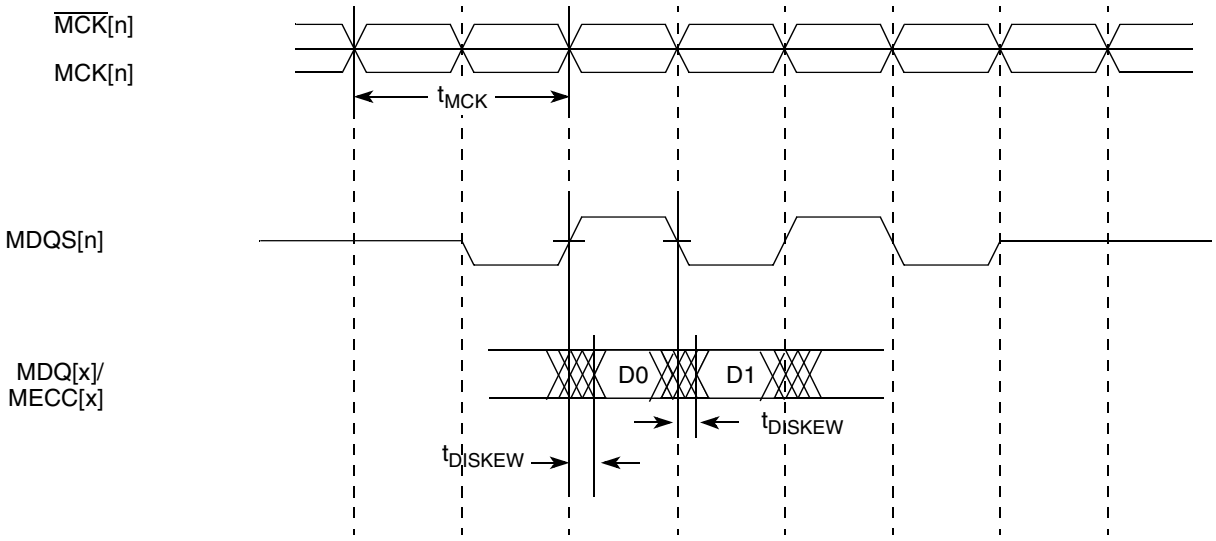


Figure 4. Timing Diagram for t_{DISKEW}

6.2.2 DDR2 SDRAM Output AC Timing Specifications

Table 18. DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz	t_{DDKHAS}	2.9	—	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz	t_{DDKHAX}	2.33	—	ns	3
$\overline{\text{MCS}}$[n] output setup with respect to MCK 266 MHz	t_{DDKHCS}	3.15	—	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz	t_{DDKHCX}	3.15	—	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM/MECC output setup with respect to MDQS 266 MHz	t_{DDKHDS}, t_{DDKLDS}	900	—	ps	5
MDQ//MDM/MECC output hold with respect to MDQS 266 MHz	t_{DDKHDX}, t_{DDKLDX}	1100	—	ps	5

Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 5 shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

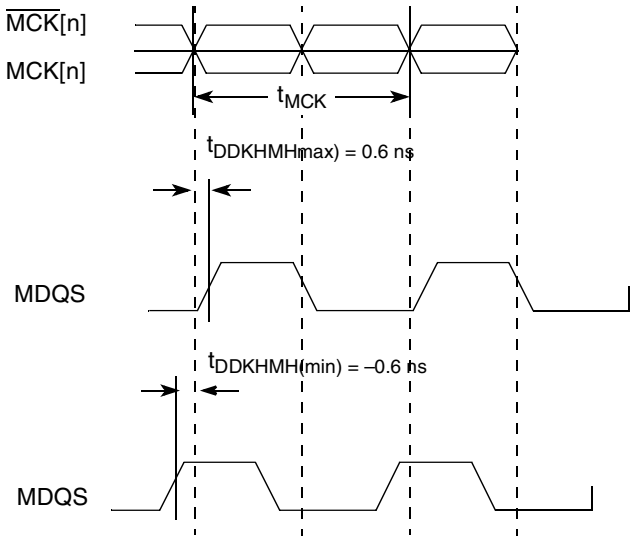


Figure 5. Timing Diagram for t_{DDKHMH}

Figure 6 shows the DDR2 SDRAM output timing diagram.

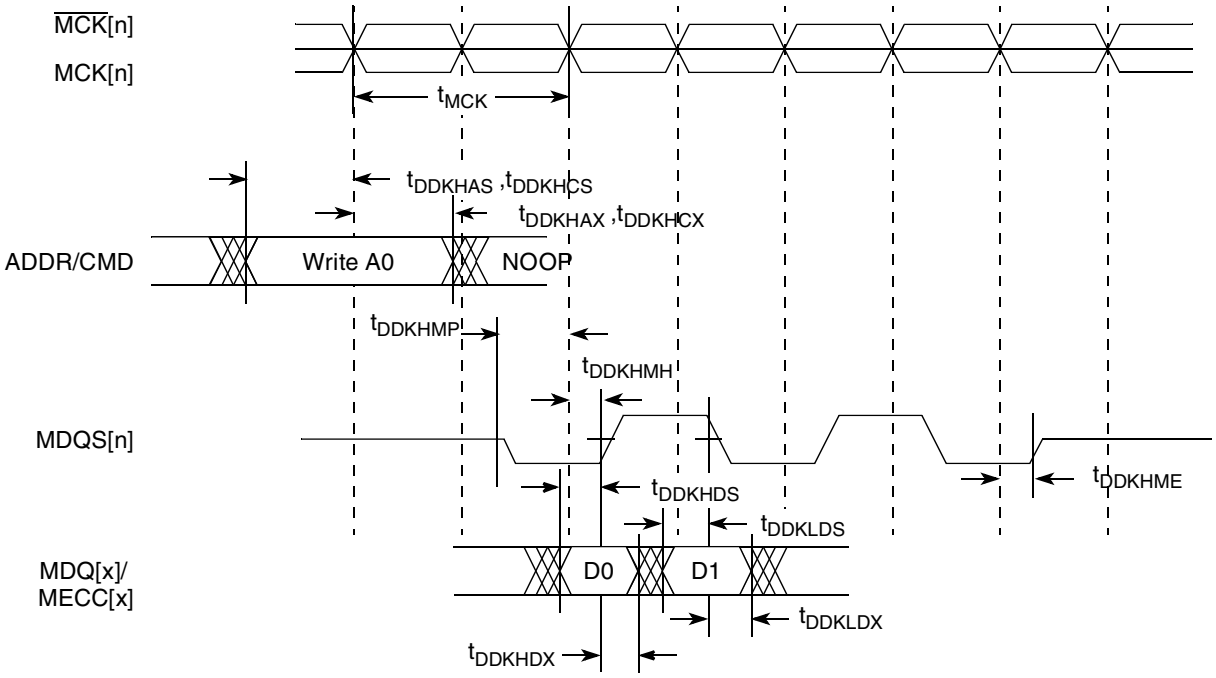


Figure 6. DDR2 SDRAM Output Timing Diagram

Figure 7 provides the AC test load for the DDR2 bus.

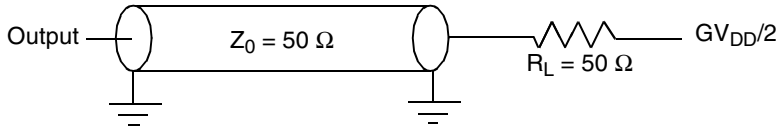


Figure 7. DDR2 AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NV_{DD} + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	NV_{DD} – 0.2	—	V

Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NV_{DD})	I_{IN}	—	± 5	µA

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management. MPC8308 supports dual Ethernet controllers.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII) and reduced gigabit media independent interface (RGMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII interface is defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RGMII interface follows the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, “Ethernet Management Interface Electrical Characteristics.”

8.1.1 eTSEC DC Electrical Characteristics

All MII and RGMII drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The RGMII signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}	—		3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD}= Min	VSS	0.50	V
Input high voltage	V_{IH}	—	—	2.1	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 22. RGMII DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD}= Min	VSS – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	15	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–15	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII and RGMII AC Timing Specifications

The AC timing specifications for MII and RGMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 shows the MII transmit AC timing diagram.

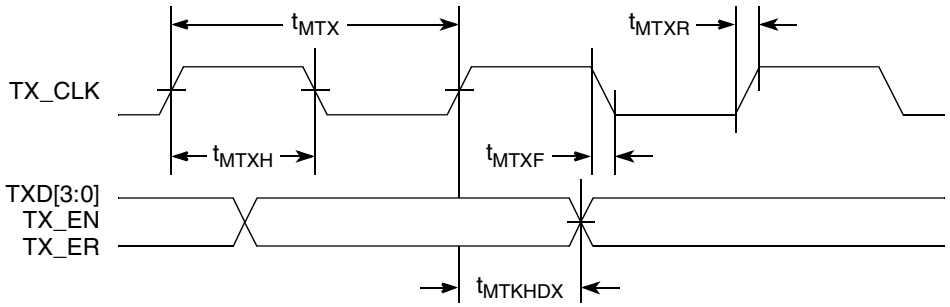


Figure 8. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} /NV_{DD} of 3.3 V ± 0.3V.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the MII receive AC timing diagram.

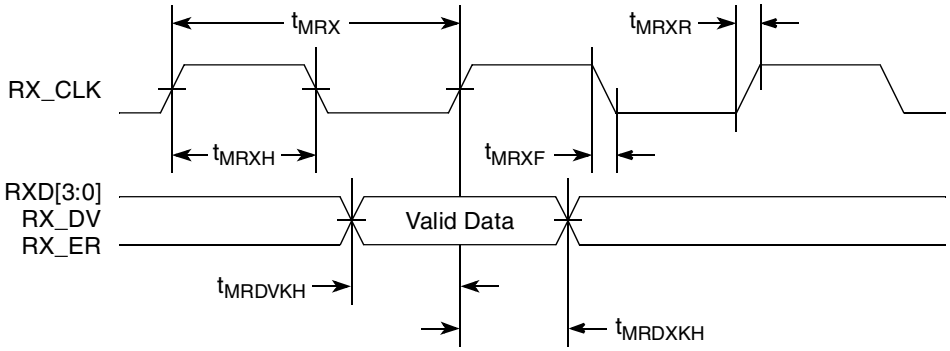


Figure 9. MII Receive AC Timing Diagram RMII AC Timing Specifications

Figure 10 provides the AC test load.

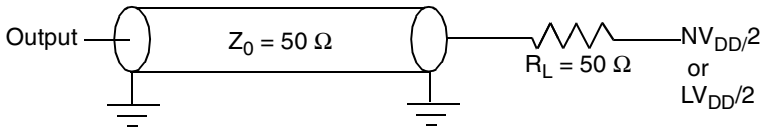


Figure 10. AC Test Load

8.2.2 RGMII AC Timing Specifications

Table 25 presents the RGMII AC timing specifications.

Table 25. RGMII AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

Table 25. RGMII AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $0.5*LV_{DD}$
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

Figure 11 shows the RGMII AC timing and multiplexing diagrams.

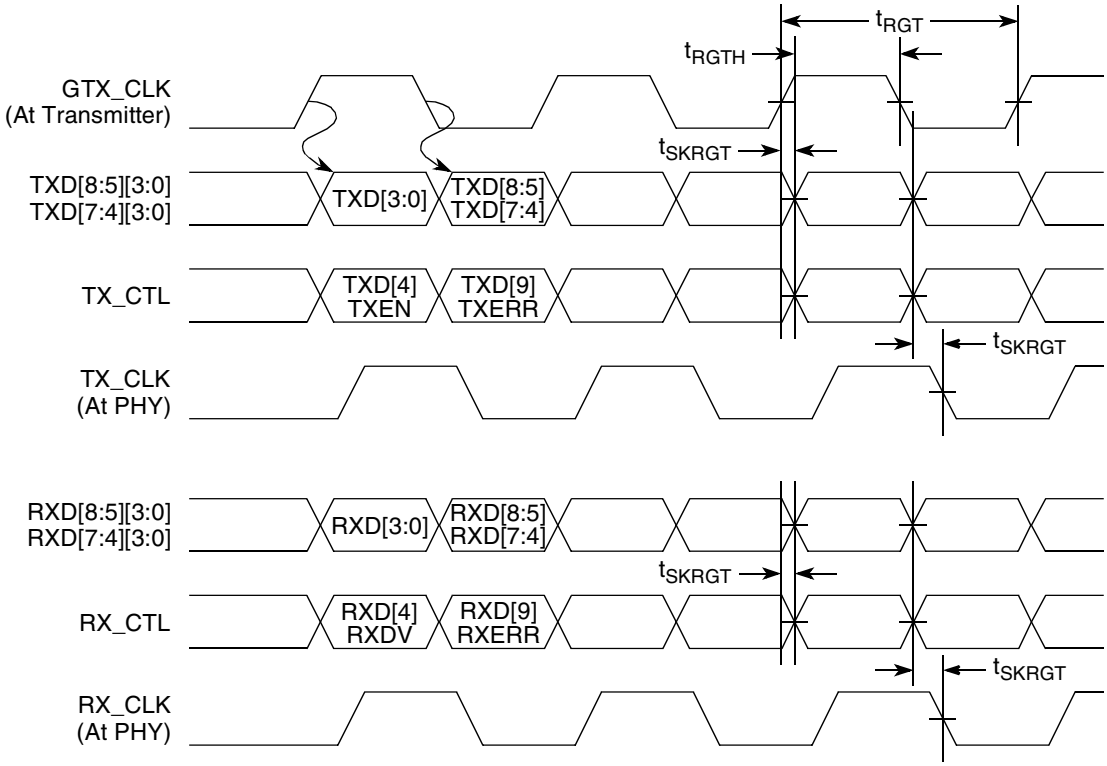


Figure 11. RGMII AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII and RGMII are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. Table 26 provides the DC electrical characteristics for MDIO and MDC.

Table 26. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DD}	—		3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = Min	2.10	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	VSS	0.50	V
Input high voltage	V_{IH}	—		2.0	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DD} = Max	V_{IN} [1] = 2.1 V	—	40	µA
Input low current	I_{IL}	NV_{DD} = Max	V_{IN} = 0.5 V	–600	—	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 27 provides the MII management AC timing specifications.

Table 27. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Table 27. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DDA}/LV_{DDB} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)
3. This parameter is dependent on the cbs_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

Figure 12 shows the MII management AC timing diagram.

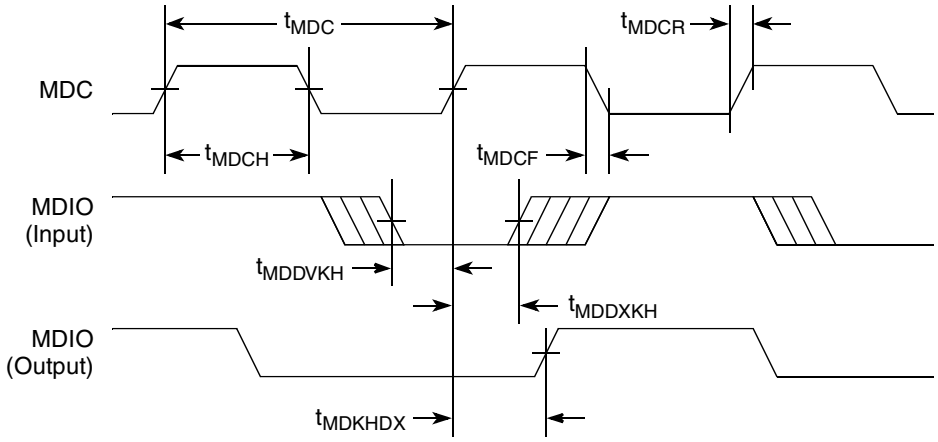


Figure 12. MII Management Interface Timing Diagram

8.4 IEEE Std 1588™ Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

8.4.1 IEEE 1588 Timer DC Specifications

Table 28 provides the IEEE 1588 timer DC specifications.

Table 28. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V

Table 28. GPIO DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NVDD$	—	± 5	μA

8.4.2 IEEE 1588 Timer AC Specifications

Table 29 provides the IEEE 1588 timer AC specifications.

Table 29. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Notes:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 USB

9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

9.1.1 USB DC Electrical Characteristics

Table 30 lists the DC electrical characteristics for the USB interface.

Table 30. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

9.1.2 USB AC Electrical Specifications

Table 31 lists the general timing parameters of the USB-ULPI interface.

Table 31. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	1, 2
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	1, 4
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	1, 4
USB clock to output valid—all outputs	t_{USKHOV}	—	9	ns	1
Output hold from USB clock—all outputs	t_{USKHOX}	1	—	ns	1

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 13 and Figure 14 provide the AC test load and signals for the USB, respectively.

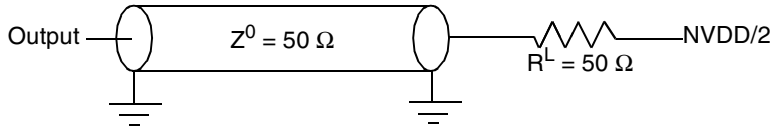


Figure 13. USB AC Test Load

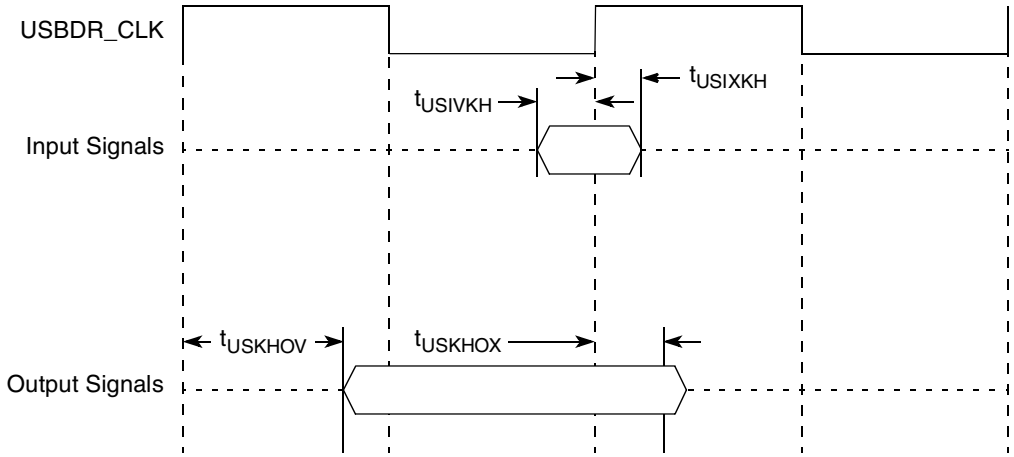


Figure 14. USB Signals

10 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

10.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 15 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's single-ended swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**)

   The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**)

   The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak–peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{TX}n}$, for example) from the non-inverting signal (TX*n*, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 24 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The common mode voltage is equal to one-half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

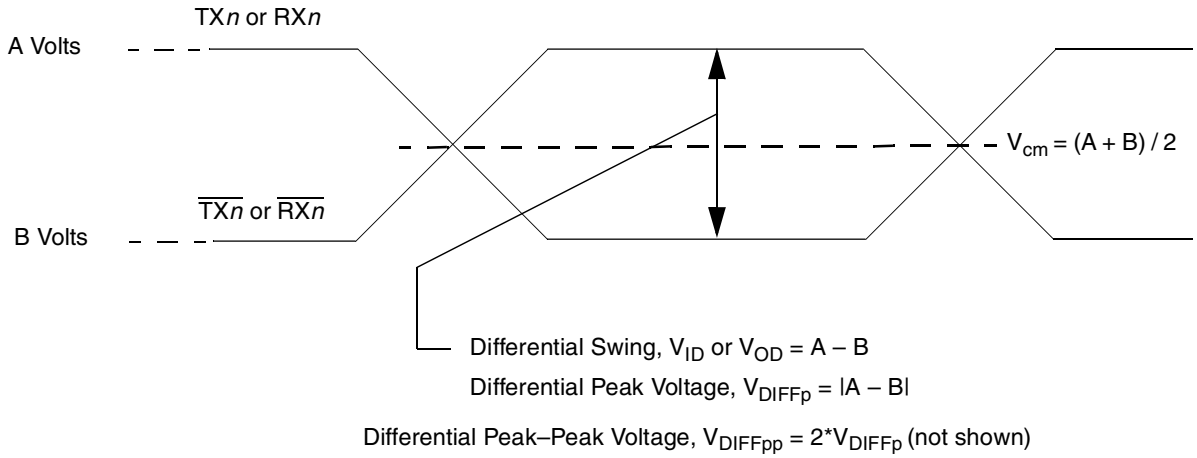


Figure 15. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV; in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

10.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD_REF_CLK}$ for PCI Express.

The following sections describe the SerDes reference clock requirements and some application information.

10.2.1 SerDes Reference Clock Receiver Characteristics

Figure 16 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 16. Each differential clock input (SD_REF_CLK or $\overline{\text{SD_REF_CLK}}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC-coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREVSS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ inputs cannot drive 50 Ω to XCOREVSS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

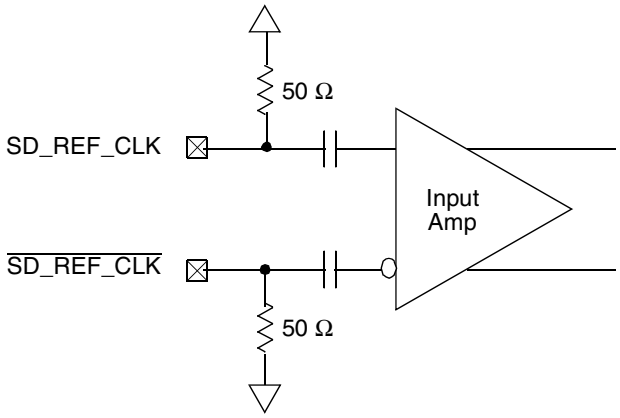


Figure 16. Receiver of SerDes Reference Clocks

10.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8308 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak–peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 10.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 17 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 18 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-Ended Mode**
  - The reference clock can also be single ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak–peak (from Vmin to Vmax) with $\overline{\text{SD_REF_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 19 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD_REF_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

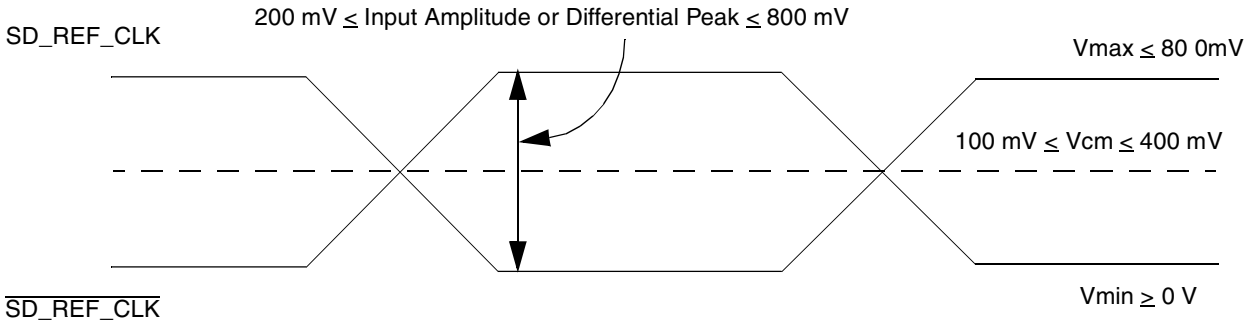


Figure 17. Differential Reference Clock Input DC Requirements (External DC-Coupled)

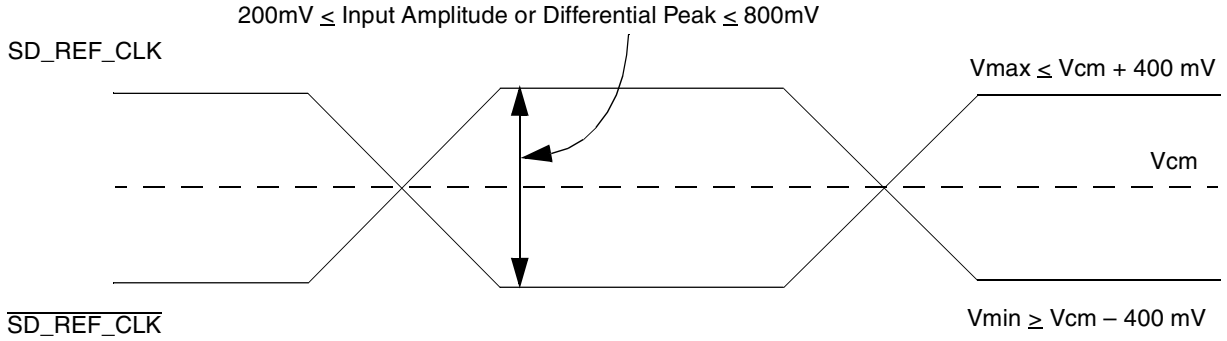


Figure 18. Differential Reference Clock Input DC Requirements (External AC-Coupled)

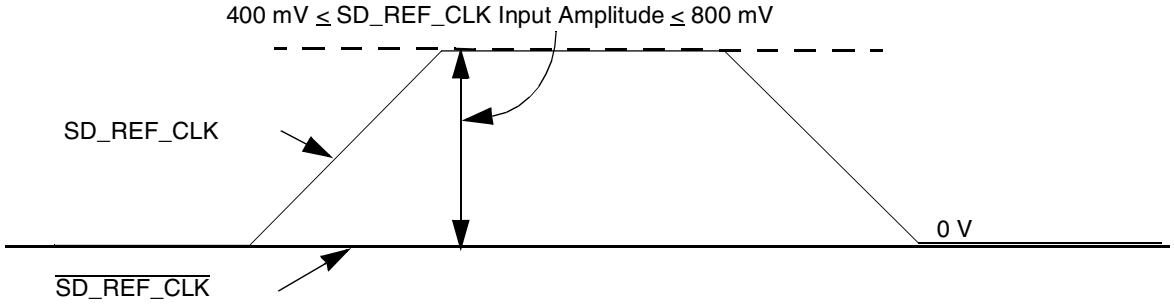


Figure 19. Single-Ended Reference Clock Input DC Requirements

10.2.3 Interfacing with Other Differential Signaling Levels

With on-chip termination to XCOREVSS, the differential reference clocks inputs are high-speed current steering logic (HCSL)-compatible and DC-coupled.

Many other low-voltage differential type outputs like low-voltage differential signaling (LVDS) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100–400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 20 to Figure 23 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8308 SerDes reference clock receiver requirement provided in this document.

Figure 20 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8308 SerDes reference clock input's DC requirement.

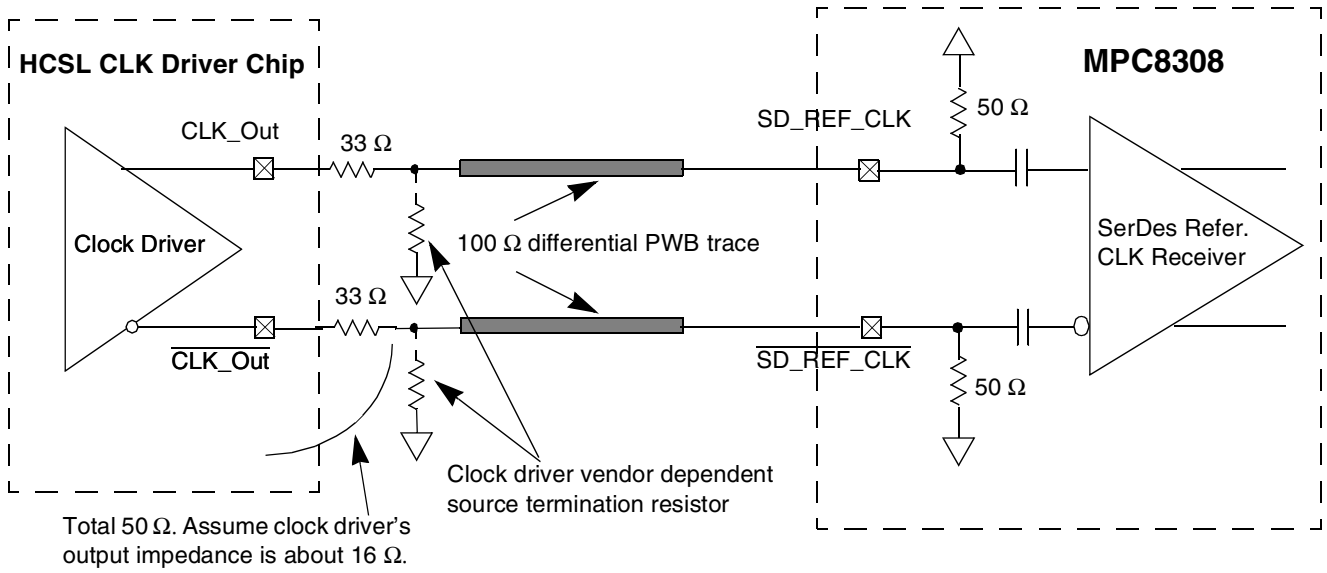


Figure 20. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 21 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8308's SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

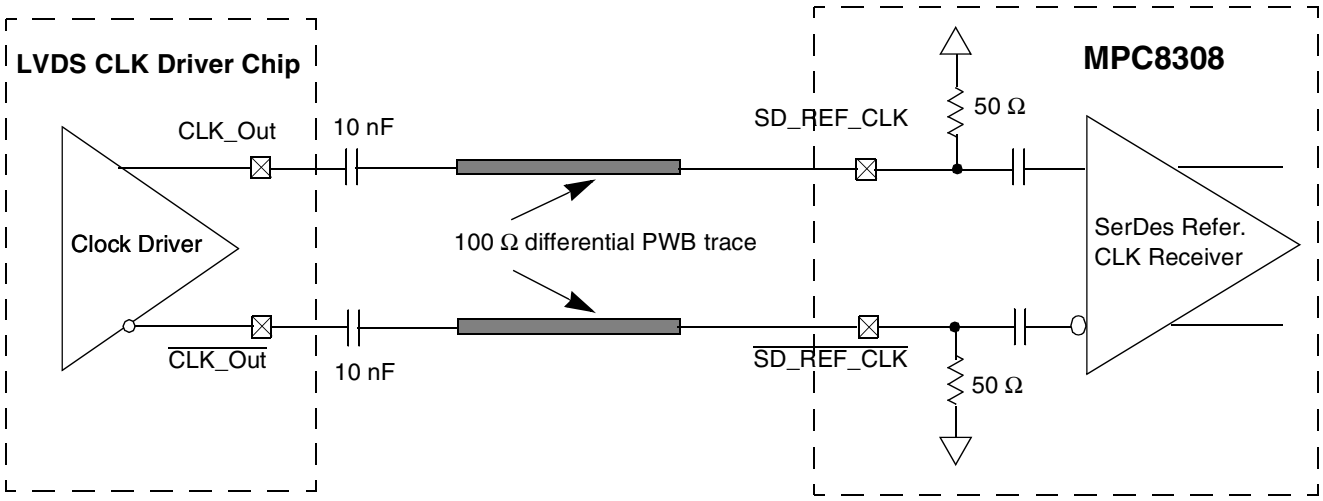


Figure 21. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 22 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8308 SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 22 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8308's SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

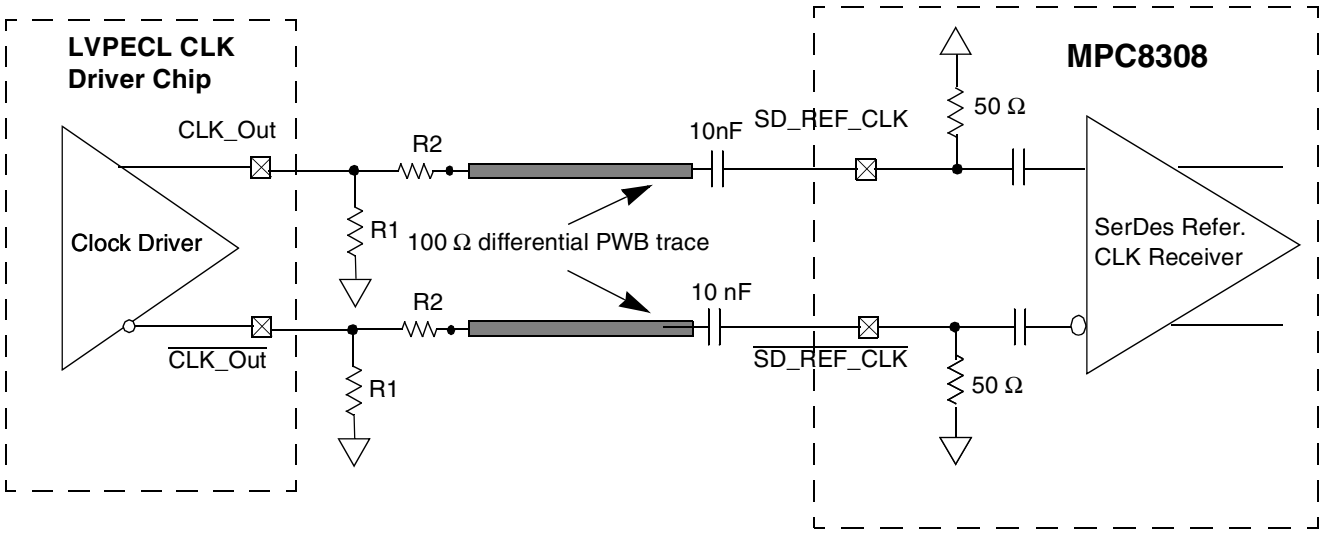


Figure 22. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 23 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the device's SerDes reference clock input's DC requirement.

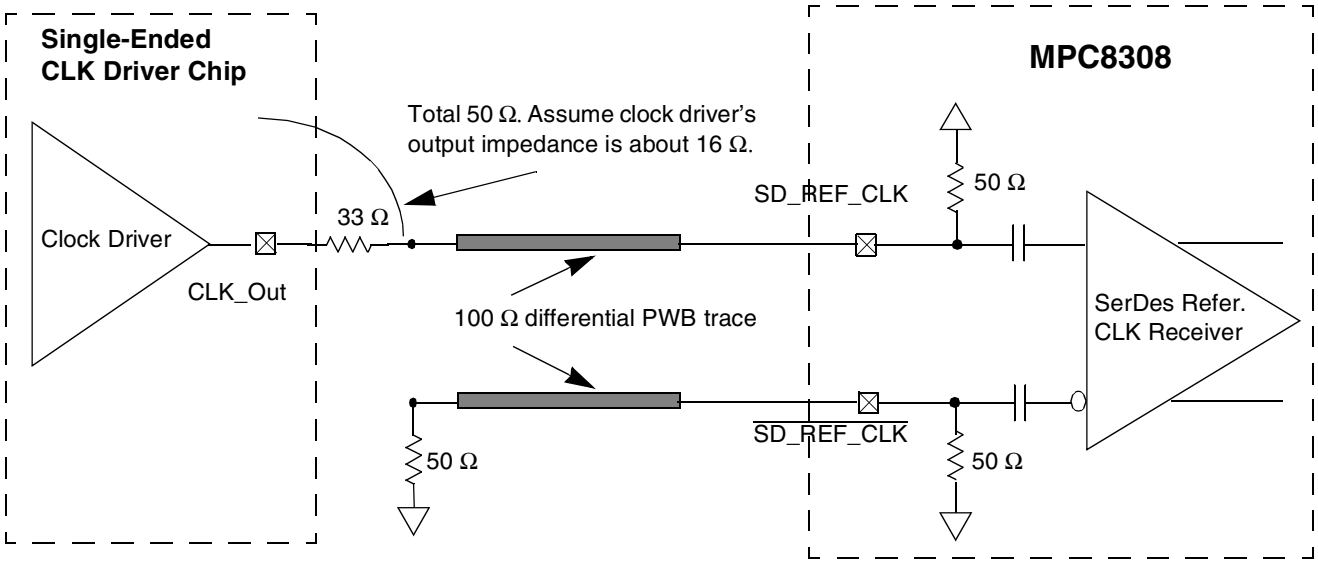


Figure 23. Single-Ended Connection (Reference Only)

10.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high-quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops, and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 32 describes some AC parameters for PCI Express protocol.

Table 32. SerDes Reference Clock AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2

Table 32. SerDes Reference Clock AC Parameters (continued)

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD_REF_CLK) to falling edge rate ($\overline{\text{SD_REF_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing (Figure 24).
4. Matching applies to rising edge rate for SD_REF_CLK and falling edge rate for $\overline{\text{SD_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate (See Figure 25).

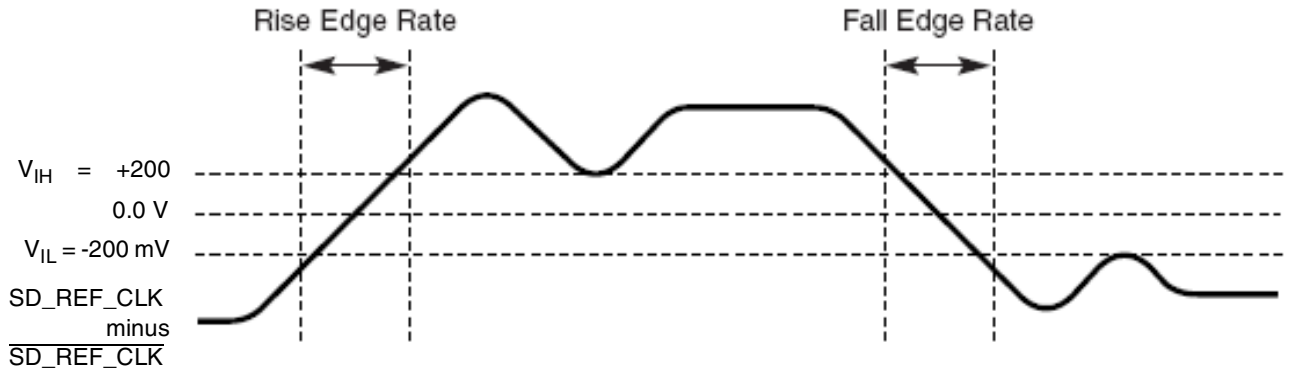


Figure 24. Differential Measurement Points for Rise and Fall Time

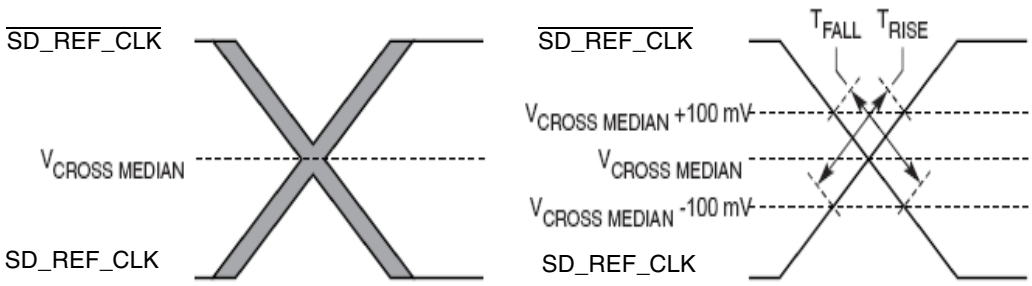


Figure 25. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. For detailed information, see Section 11.2, "AC Requirements for PCI Express SerDes Clocks."

10.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

10.3 SerDes Transmitter and Receiver Reference Circuits

Figure 26 shows the reference circuits for SerDes data lane's transmitter and receiver.

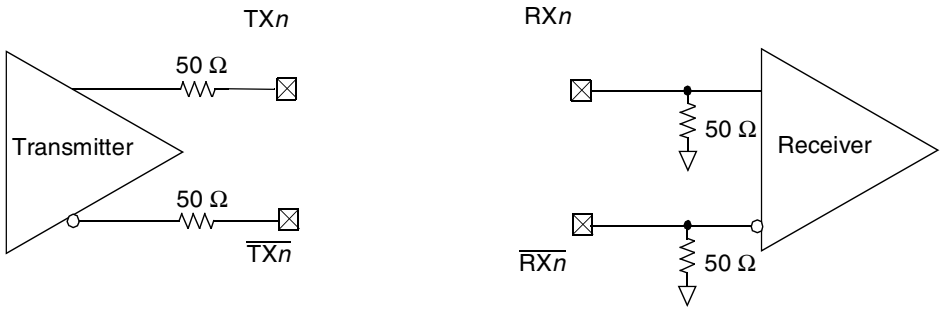


Figure 26. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in Section 11, "PCI Express."

Note that external AC-coupling capacitor is required for the PCI Express serial transmission protocol with the capacitor value defined in specification of PCI Express protocol section.

11 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

11.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$

For more information, see Section 10.2, "SerDes Reference Clocks."

11.2 AC Requirements for PCI Express SerDes Clocks

Table 33 lists the PCI Express SerDes clock AC requirements.

Table 33. SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Units	Notes
t_{REF}	REFCLK cycle time (for 125 MHz and 100 MHz)	8	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

11.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

11.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

11.4.1 Differential Transmitter (TX) Output

Table 34 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 34. Differential Transmitter (TX) Output Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
Unit interval	UI	Each U_{PETX} is 400 ps ± 300 ppm. U_{PETX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	$V_{PEDPPTX} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.8	—	1.2	V	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	Ratio of the $V_{PEDPPTX}$ of the second and following bits after a transition divided by the $V_{PEDPPTX}$ of the first bit after a transition.	–3.0	–3.5	–4.0	dB	2
Minimum TX eye width	T_{TX-EYE}	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - U_{PEEWTX}= 0.3$ UI.	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPTX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.15	UI	2, 3

Table 34. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
D+/D- TX output rise/fall time	$T_{TX-RISE}$, $T_{TX-FALL}$	—	0.125	—	—	UI	2, 5
RMS AC peak common mode output voltage	$V_{TX-CM-ACp}$	$V_{PEACPCMTX}$ = RMS($\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$	—	—	20	mV	2
Absolute delta of DC common mode voltage during L0 and electrical idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	$\|V_{TX-CM-DC\ (during\ L0)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\|$<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [Electrical Idle]	0	—	100	mV	2
Absolute delta of DC common mode between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\|$ <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of $\|V_{TX-D-}\|$	0	—	25	mV	2
Electrical idle differential peak output voltage	$V_{TX-IDLE-DIFFp}$	$V_{PEEIDPTX}$ = $\|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\|$ <= 20 mV	0	—	20	mV	2
Amount of voltage change allowed during receiver detection	$V_{TX-RCV-DETECT}$	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present.	—	600	—	mV	6
TX DC common mode voltage	$V_{TX-DC-CM}$	The allowed DC Common Mode voltage under any conditions.	—	3.6	—	V	6
TX short circuit current limit	$I_{TX-SHORT}$	The total current the Transmitter can provide when shorted to its ground	—	—	90	mA	—
Minimum time spent in electrical idle	$T_{TX-IDLE-MIN}$	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set	50	—	—	UI	—

Table 34. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX-IDLE-SET-TO-IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX-DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	RL_{TX-CM}	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX-DIFF-DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	Z_{TX-DC}	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX-SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—
AC-coupling capacitor	C_{TX}	All Transmitters are AC-coupled. The AC-coupling is required either within the media or within the transmitting component itself. An external capacitor of 100nF is recommended.	75	—	200	nF	—

Table 34. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 29 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 27.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance results in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 29). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20% and 80% at transmitter package pins into a test load as shown in Figure 29 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.

11.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 27 is specified using the passive compliance/test measurement load (Figure 29) in place of any real PCI Express interconnect + RX component. There are two eye diagrams that must be met for the transmitter. Both diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

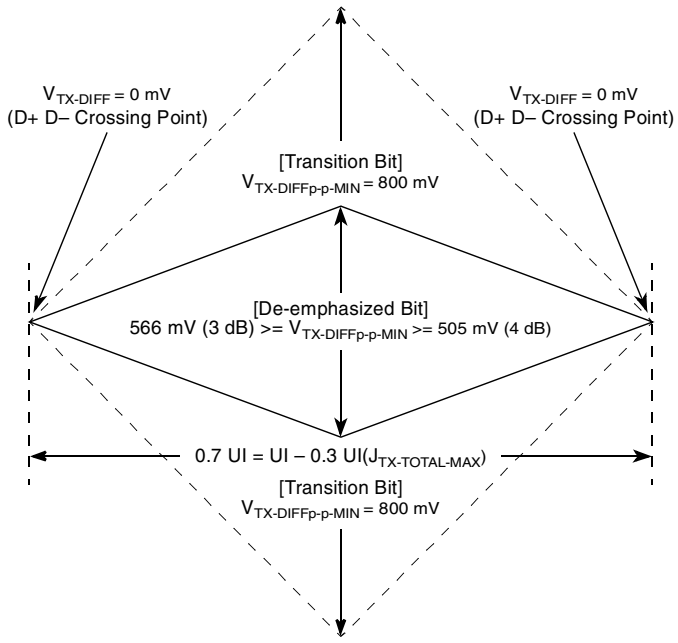


Figure 27. Minimum Transmitter Timing and Voltage Output Compliance Specifications

11.4.3 Differential Receiver (RX) Input Specifications

Table 35 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 35. Differential Receiver (RX) Input Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
Unit interval	UI	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{RX-DIFFp-p}$	$V_{PEDPPRX}$ = 2*|V_{RX-D+} - V_{RX-D-}|	0.175	—	1.200	V	2
Minimum receiver eye width	T_{RX-EYE}	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - U_{PEEWRX}= 0.6 UI.	0.4	—	—	UI	2, 3

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.3	UI	2, 3, 7
AC peak common mode input voltage	$V_{RX-CM-ACp}$	$V_{PEACPCMRX} = \lvert V_{RXD+} + V_{RXD-} \rvert /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-} \rvert /2$	—	—	150	mV	2
Differential return loss	$RL_{RX-DIFF}$	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.	15	—	—	dB	4
Common mode return loss	RL_{RX-CM}	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V.	6	—	—	dB	4
DC differential input impedance	$Z_{RX-DIFF-DC}$	RX DC differential mode impedance.	80	100	120	Ω	5
DC Input Impedance	Z_{RX-DC}	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance).	40	50	60	Ω	2, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	$V_{PEEIDT} = 2*\lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—

Table 35. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Units	Notes
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 29 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 28). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance results in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 29). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

11.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 28 is specified using the passive compliance/test measurement load (Figure 29) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (Figure 29) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 28) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package

and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 29). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

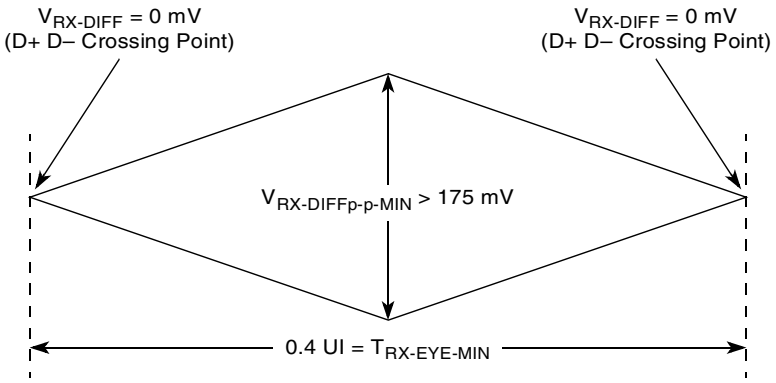


Figure 28. Minimum Receiver Eye Timing and Voltage Compliance Specification

11.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 29.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

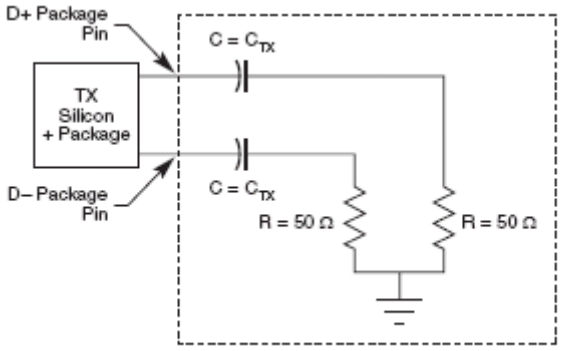


Figure 29. Compliance Test/Measurement Load

12 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

12.1 Enhanced Local Bus DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the local bus interface.

Table 36. Local Bus DC Electrical Characteristics at 3.3 V

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	NV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current, (V_{IN}[1] = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±5	μA
High-level output voltage, (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.2	V

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

12.2 Enhanced Local Bus AC Electrical Specifications

Table 37 describes the general timing parameters of the local bus interface.

Table 37. Local Bus General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (Note: to be revisited)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (Note: to be revisited)	t_{LBIXKH}	1	—	ns	3, 4

Table 37. Local Bus General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output valid (Note: to be revisited)	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LD (Note: to be revisited)	t_{LBKHOZ}	—	4	ns	5

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $NV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times NV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 30 provides the AC test load for the local bus.

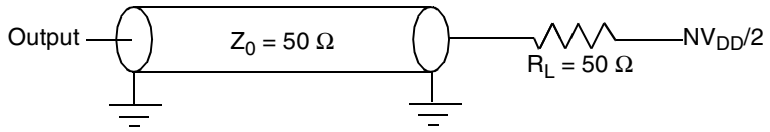


Figure 30. Local Bus AC Test Load

Figure 31 through Figure 33 show the local bus signals.

In what follows, T1, T2, T3, and T4 are internal clock reference phase signals corresponding to LCCR[CLKDIV].

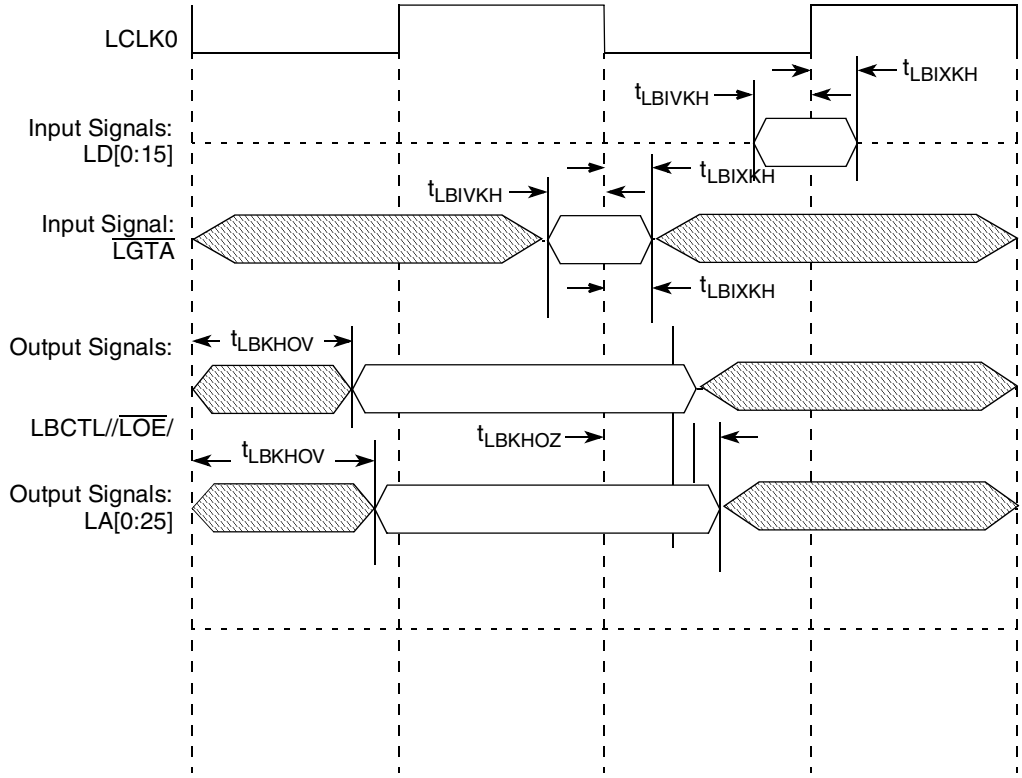


Figure 31. Local Bus Signals, Non-Special Signals Only

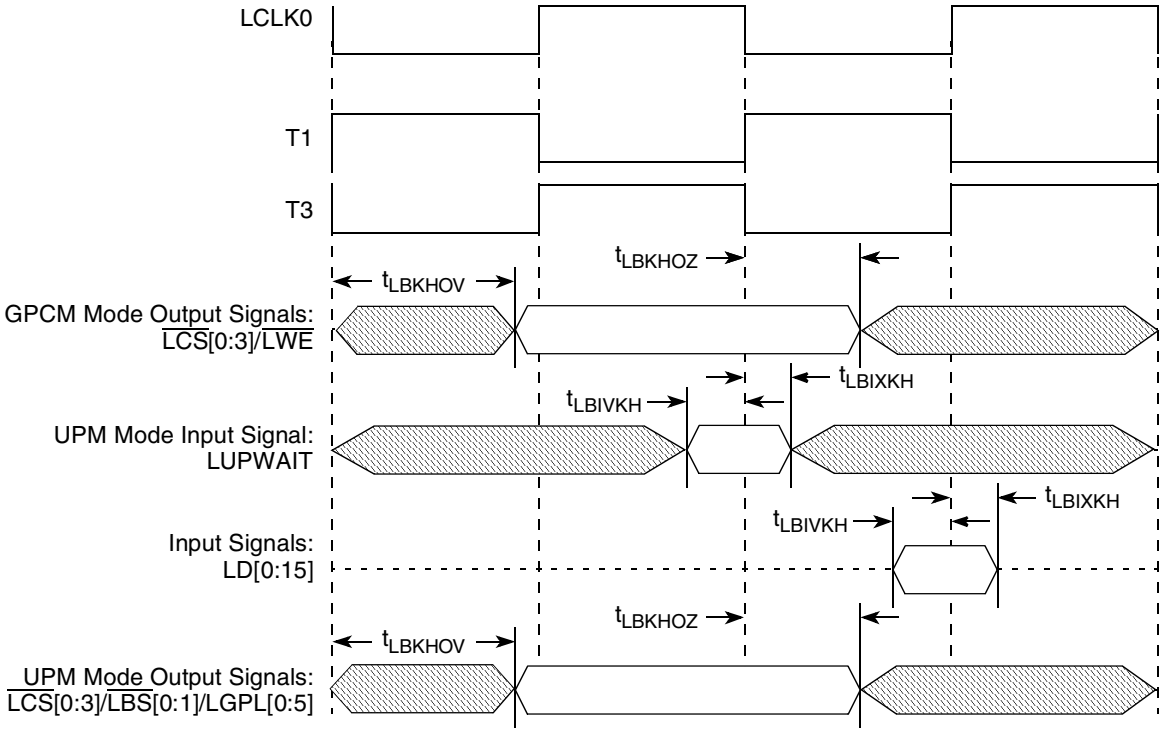


Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2

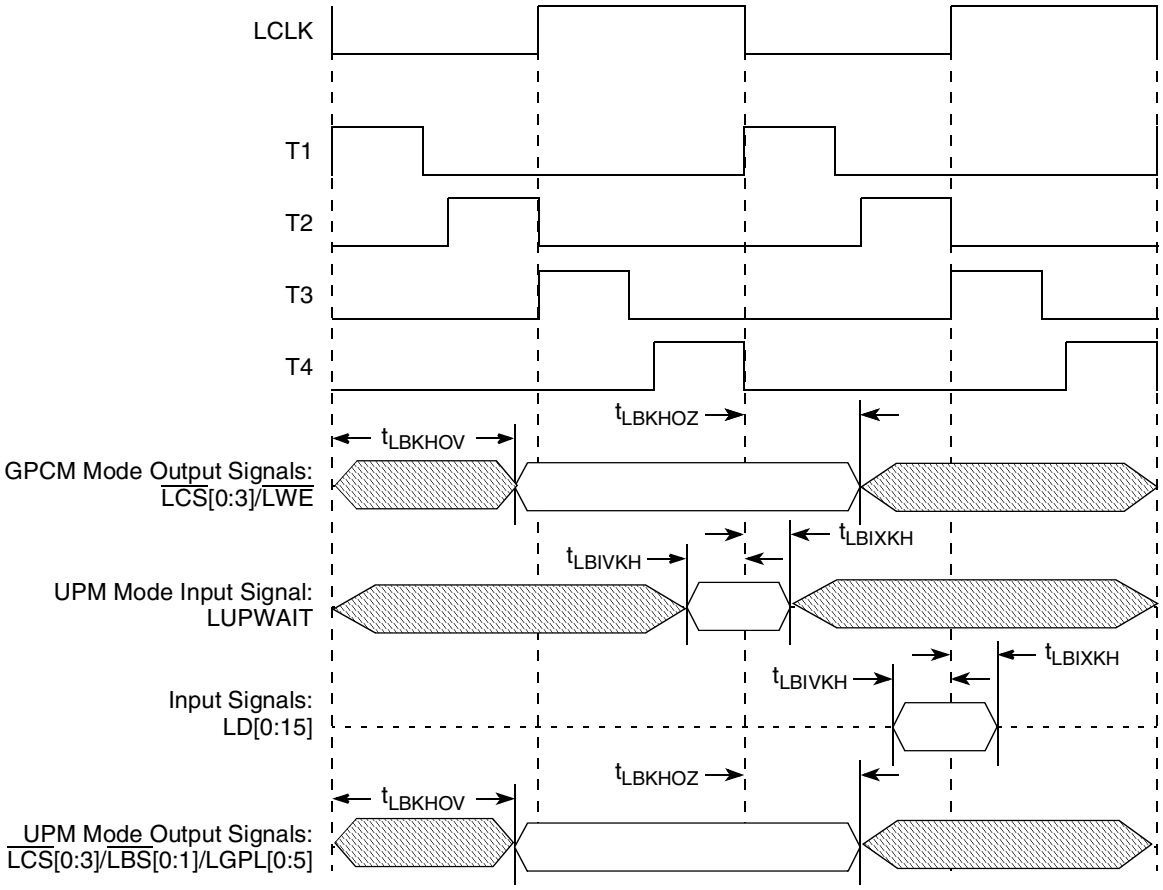


Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC/SDIO) interface of the MPC8308.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and rising edge to sample the SD_DAT[0:3], CMD, $\overline{\text{CD}}$, and WP as inputs. This behavior is true for both full- and high-speed modes.

13.1 eSDHC DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device, compatible with SDHC specifications. The eSDHC NV_{DD} range is between 3.0 V and 3.6 V.

Table 38. eSDHC interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 38. eSDHC interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V

13.2 eSDHC AC Timing Specifications (Full-Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. Table 39 provides the eSDHC AC timing specifications for full-speed mode as defined in Figure 35 and Figure 36.

Table 39. eSDHC AC Timing Specifications for Full-Speed Mode

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD_CLK clock frequency—full-speed mode	f_{SFSCK}	0	25	MHz	—
SD_CLK clock cycle	t_{SFSCK}	40	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	kHz	—
SD_CLK clock low time	t_{SFSCKL}	15	—	ns	2
SD_CLK clock high time	t_{SFSCKH}	15	—	ns	2
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	5	ns	2
Input setup times: SD_CMD, SD_DATx to SD_CLK	$t_{SFSIVKH}$	3	—	ns	2
Input hold times: SD_CMD, SD_DATx to SD_CLK	$t_{SFSIXKH}$	2	—	ns	2
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	3	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	–3	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full-speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

Figure 34 provides the eSDHC clock input timing diagram.

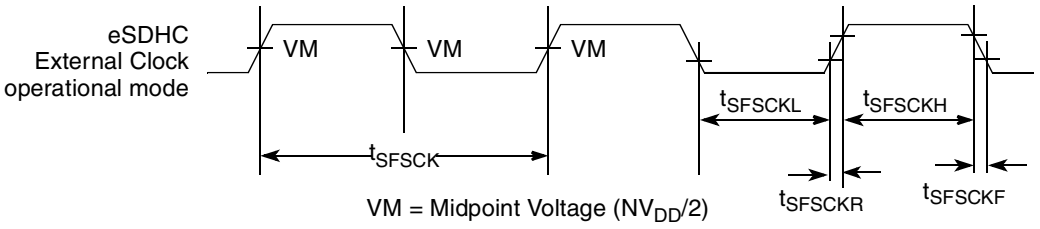


Figure 34. eSDHC Clock Input Timing Diagram

13.2.1 Full-Speed Output Path (Write)

Figure 35 provides the data and command output timing diagram.

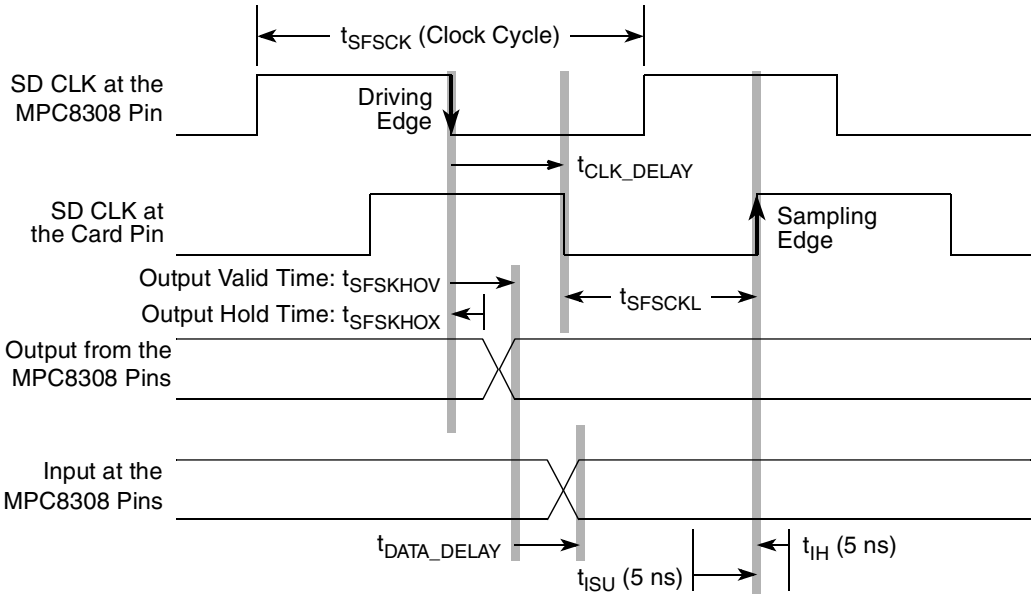


Figure 35. Full-Speed Output Path

13.2.2 Full-Speed Input Path (Read)

Figure 36 provides the data and command input timing diagram.

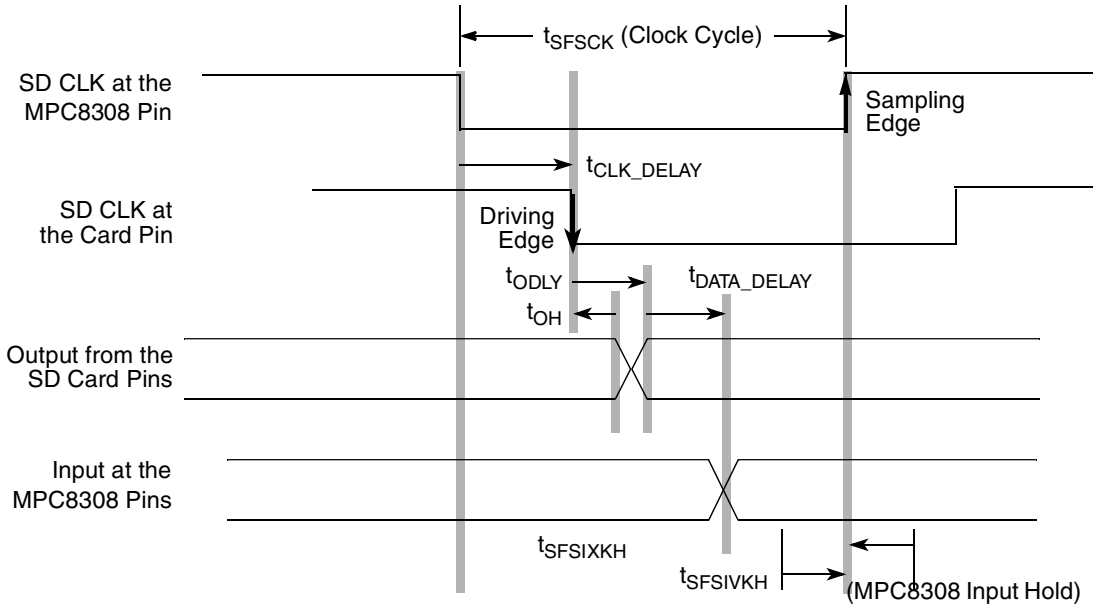


Figure 36. Full-Speed Input Path

13.3 eSDHC AC Timing Specifications

Table 40 provides the eSDHC AC timing specifications.

Table 40. eSDHC AC Timing Specifications for High-Speed Mode

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD_CLK clock frequency—high-speed mode	f_{SHSCK}	0	50	MHz	3
SD_CLK clock cycle	t_{SHSCK}	20	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	kHz	—
SD_CLK clock low time	t_{SHSCKL}	7	—	ns	2
SD_CLK clock high time	t_{SHSCKH}	7	—	ns	2
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	2
Input setup times: SD_CMD, SD_DATx	$t_{SHSIVKH}$	3	—	ns	2
Input hold times: SD_CMD, SD_DATx	$t_{SHSIXKH}$	2	—	ns	2
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	3	—	ns	2
Output Hold time: SD_CLK to SD_CMD, SD_DATx invalid	$t_{SHSKHOX}$	–3	—	ns	2
SD Card Input Setup	t_{ISU}	6	—	ns	3
SD Card Input Hold	t_{IH}	2	—	ns	3

Table 40. eSDHC AC Timing Specifications for High-Speed Mode (continued)

At recommended operating conditions NV_{DD} = 3.3 V ± 300 mV.

Parameter	Symbol [1]	Min	Max	Unit	Notes
SD Card Output Valid	t_{ODLY}	—	14	ns	3
SD Card Output Hold	t_{OH}	2.5	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full-speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.

Figure 37 provides the eSDHC clock input timing diagram.

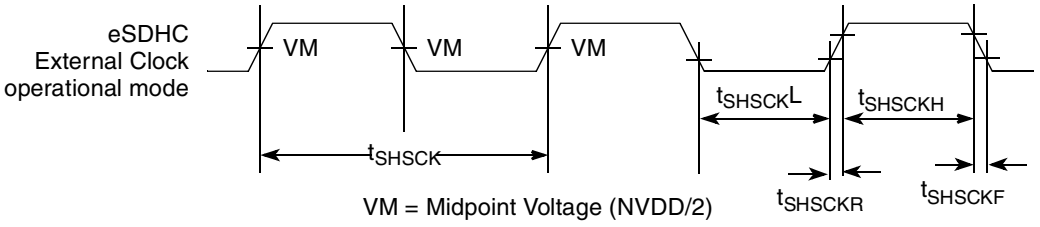


Figure 37. eSDHC Clock Input Timing Diagram

13.3.1 High-Speed Output Path (Write)

Figure 38 provides the data and command output timing diagram.

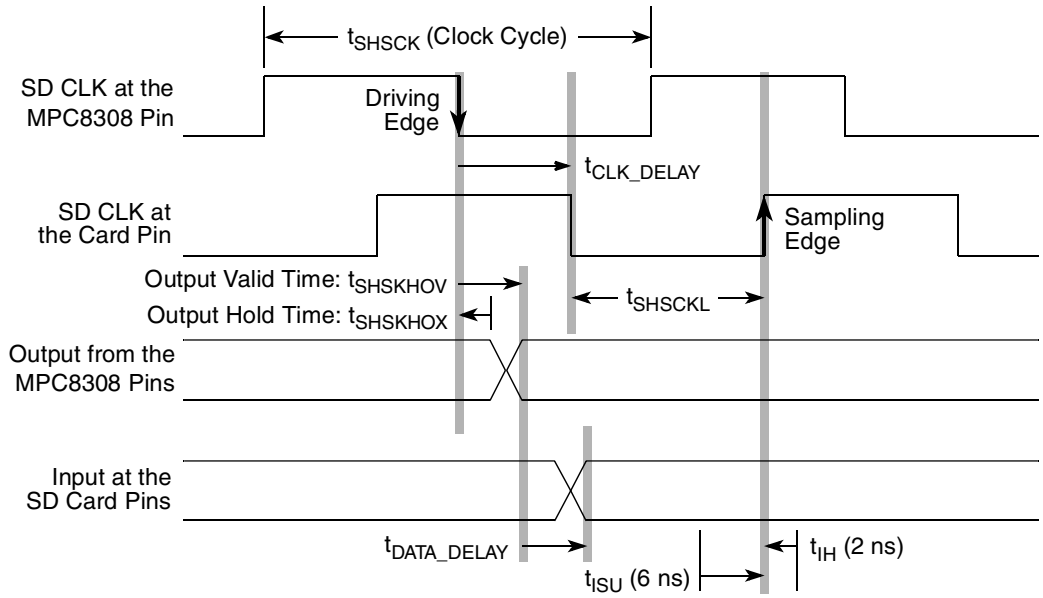


Figure 38. High-Speed Output Path

13.3.2 High-Speed Input Path (Read)

Figure 39 provides the data and command input timing diagram.

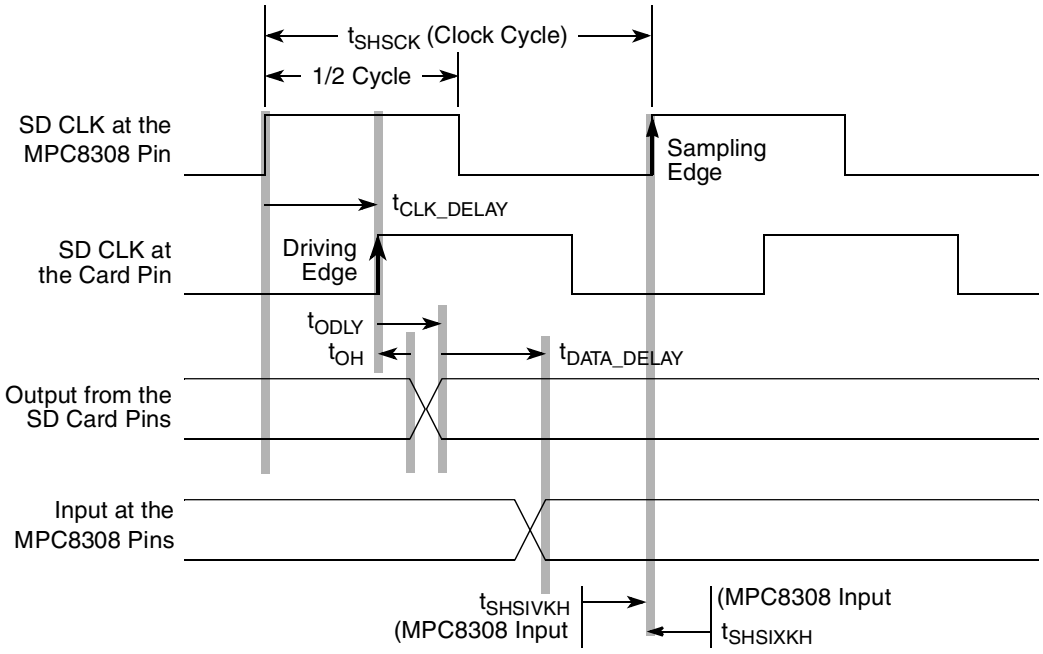


Figure 39. High-Speed Input Path

14 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

14.1 JTAG DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 41. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

Table 42 provides the JTAG AC timing specifications as defined in Figure 41 through Figure 44.

Table 42. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5

Table 42. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 40). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 40 provides the AC test load for TDO and the boundary-scan outputs.

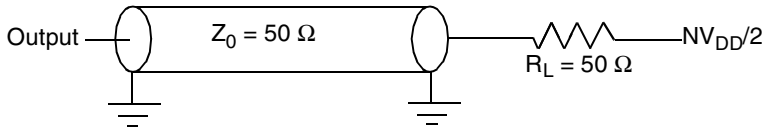


Figure 40. AC Test Load for the JTAG Interface

Figure 41 provides the JTAG clock input timing diagram.

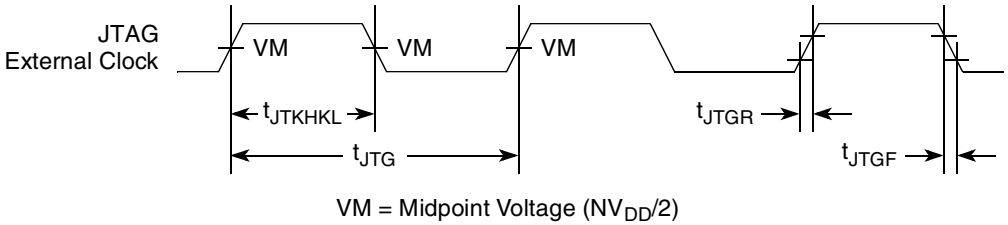


Figure 41. JTAG Clock Input Timing Diagram

Figure 42 provides the $\overline{\text{TRST}}$ timing diagram.

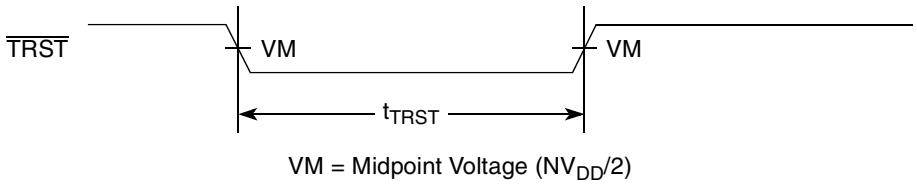


Figure 42. $\overline{\text{TRST}}$ Timing Diagram

Figure 43 provides the boundary-scan timing diagram.

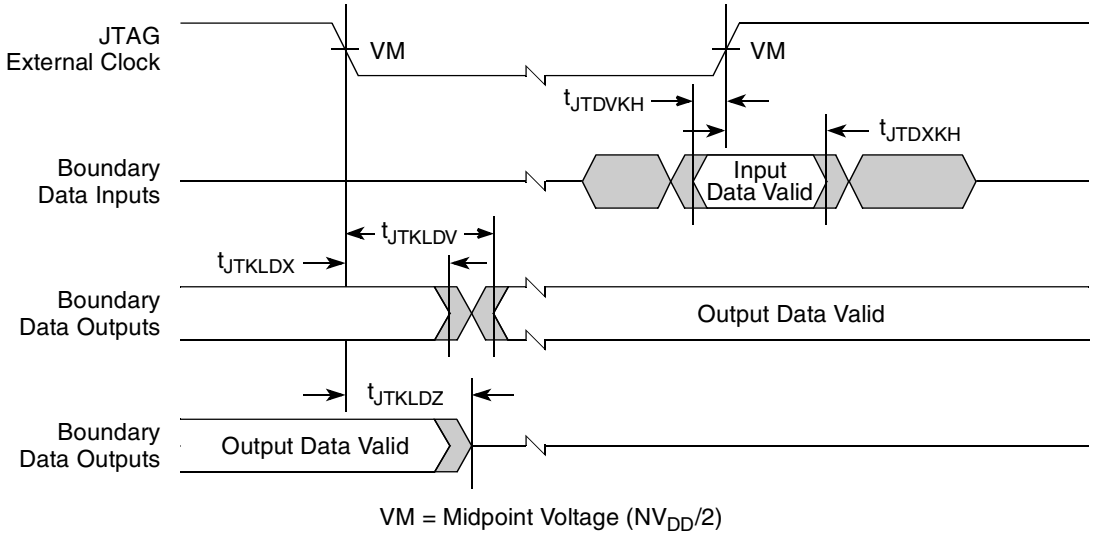


Figure 43. Boundary-Scan Timing Diagram

Figure 44 provides the test access port timing diagram.

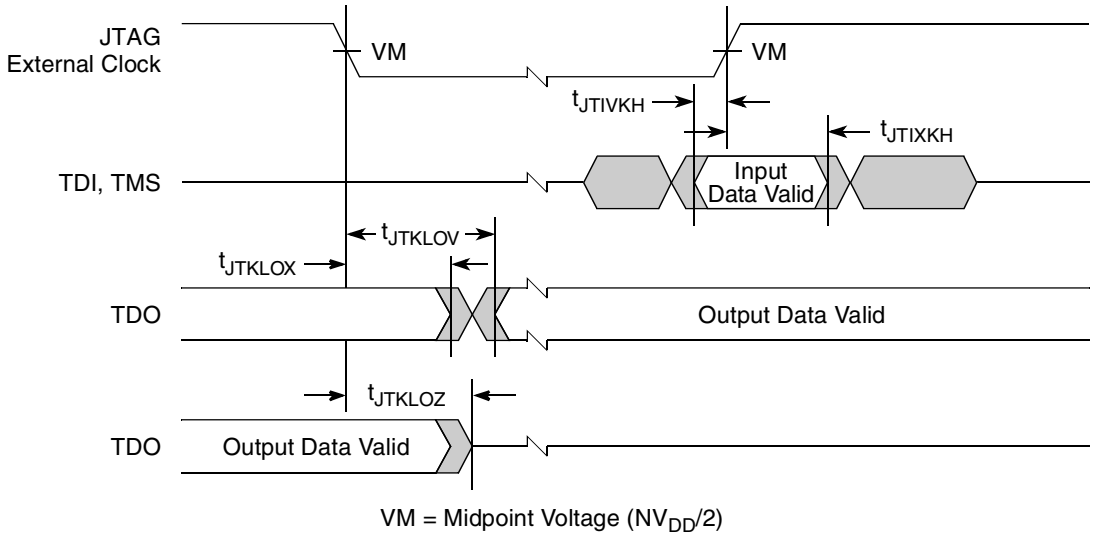


Figure 44. Test Access Port Timing Diagram

15 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

15.1 I²C DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the I²C interface.

Table 43. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high-voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Input low-voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	—
Low-level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
High-level output voltage	V_{OH}	$0.8 \times NV_{DD}$	$NV_{DD} + 0.3$	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. For information on the digital filter used, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

15.2 I²C AC Electrical Specifications

Table 44 provides the AC timing parameters for the I²C interface.

Table 44. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the low period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The device does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

Figure 45 provides the AC test load for the I²C.

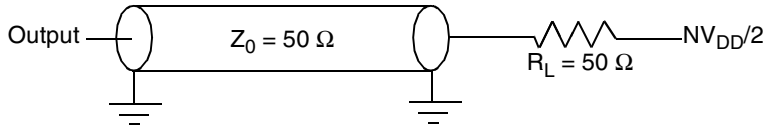


Figure 45. I²C AC Test Load

Figure 46 shows the AC timing diagram for the I²C bus.

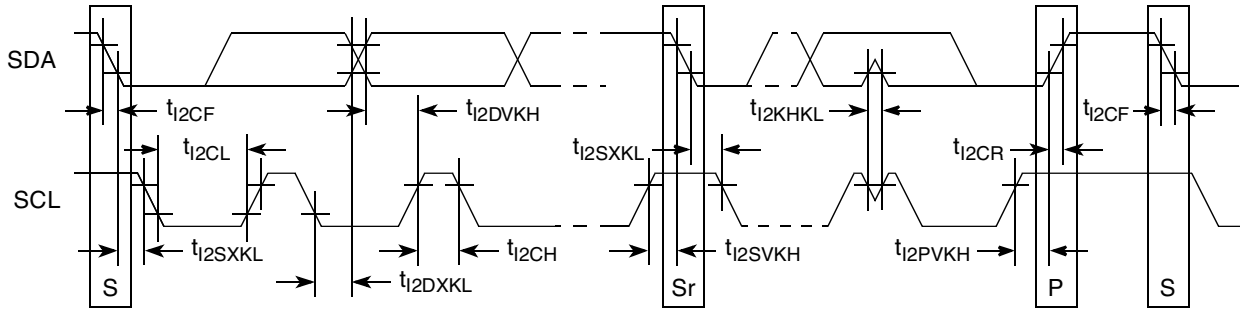


Figure 46. I²C Bus AC Timing Diagram

16 Timers

This section describes the DC and AC electrical specifications for the timers.

16.1 Timers DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8308 timers pins, including TIN, $\overline{\text{TOUT}}$, and $\overline{\text{TGATE}}$.

Table 45. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

16.2 Timers AC Timing Specifications

Table 46 provides the Timers input and output AC timing specifications.

Table 46. Timers Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

Figure 47 provides the AC test load for the Timers.

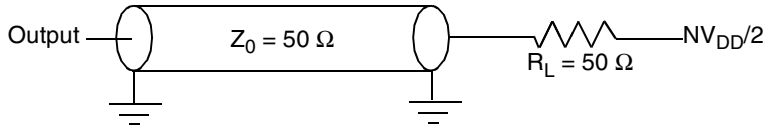


Figure 47. Timers AC Test Load

17 GPIO

This section describes the DC and AC electrical specifications for the GPIO of MPC8308

17.1 GPIO DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the GPIO.

Table 47. GPIO DC Electrical Characteristic

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NV_{DD}	—	± 5	μA

17.2 GPIO AC Timing Specifications

Table 48 provides the GPIO input and output AC timing specifications.

Table 48. GPIO Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 48 provides the AC test load for the GPIO.

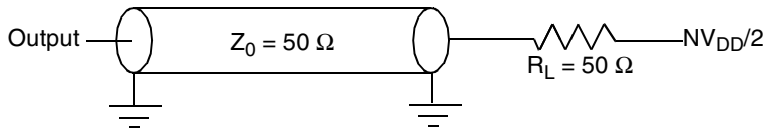


Figure 48. GPIO AC Test Load

18 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

18.1 IPIC DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the external interrupt pins.

Table 49. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

18.2 IPIC AC Timing Specifications

Table 50 provides the IPIC input and output AC timing specifications.

Table 50. IPIC Input AC Timing Specifications

Characteristic	Symbol[1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

19 SPI

This section describes the DC and AC electrical specifications for the SPI of the device.

19.1 SPI DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the MPC8308 SPI.

Table 51. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

Table 51. SPI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

19.2 SPI AC Timing Specifications

Table 52 provides the SPI input and output AC timing specifications.

Table 52. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}		8.5	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 49 provides the AC test load for the SPI.

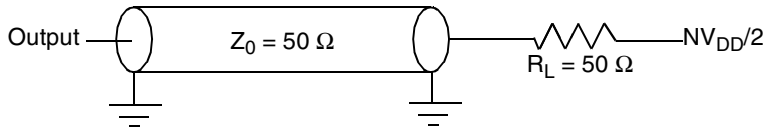
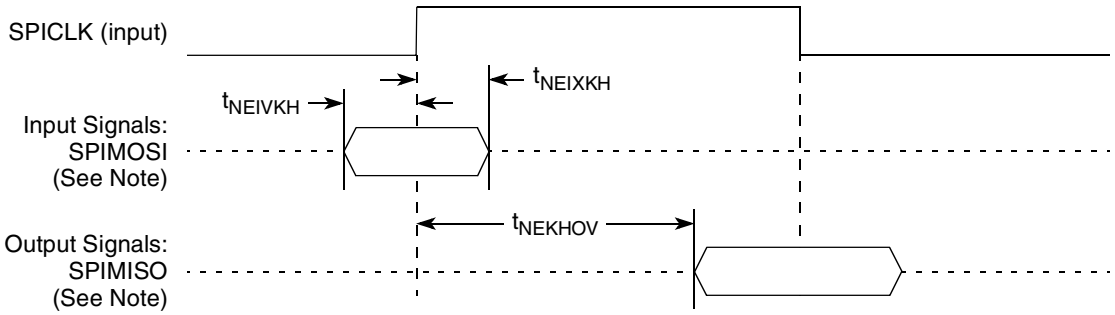


Figure 49. SPI AC Test Load

Figure 50 and Figure 51 represent the AC timing from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

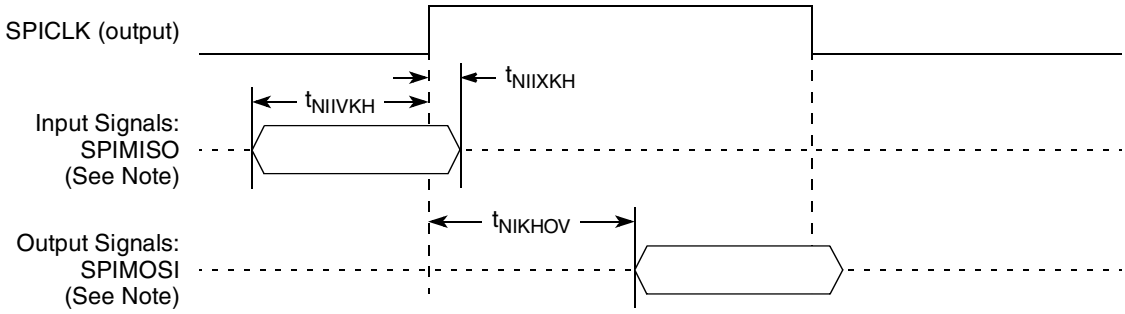
Figure 50 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 51 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 51. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8308 is available in a Moulded Array Process Ball Grid Array (MAPBGA). For information on the MAPBGA, see Section 20.1, “Package Parameters for the MPC8308 MAPBGA,” and Section 20.2, “Mechanical Dimensions of the MPC8308 MAPBGA.”

20.1 Package Parameters for the MPC8308 MAPBGA

The package parameters are as provided in the following list. The package type is 19 mm × 19 mm, 473 MAPBGA.

Package outline	19 mm × 19 mm
Interconnects	473
Pitch	0.80 mm
Module height (typical)	1.39 mm
Solder Balls	96.5 Sn/ 3.5Ag
Ball diameter (typical)	0.40 mm

20.2 Mechanical Dimensions of the MPC8308 MAPBGA

Figure 52 shows the mechanical dimensions and bottom surface nomenclature of the MAPBGA package.

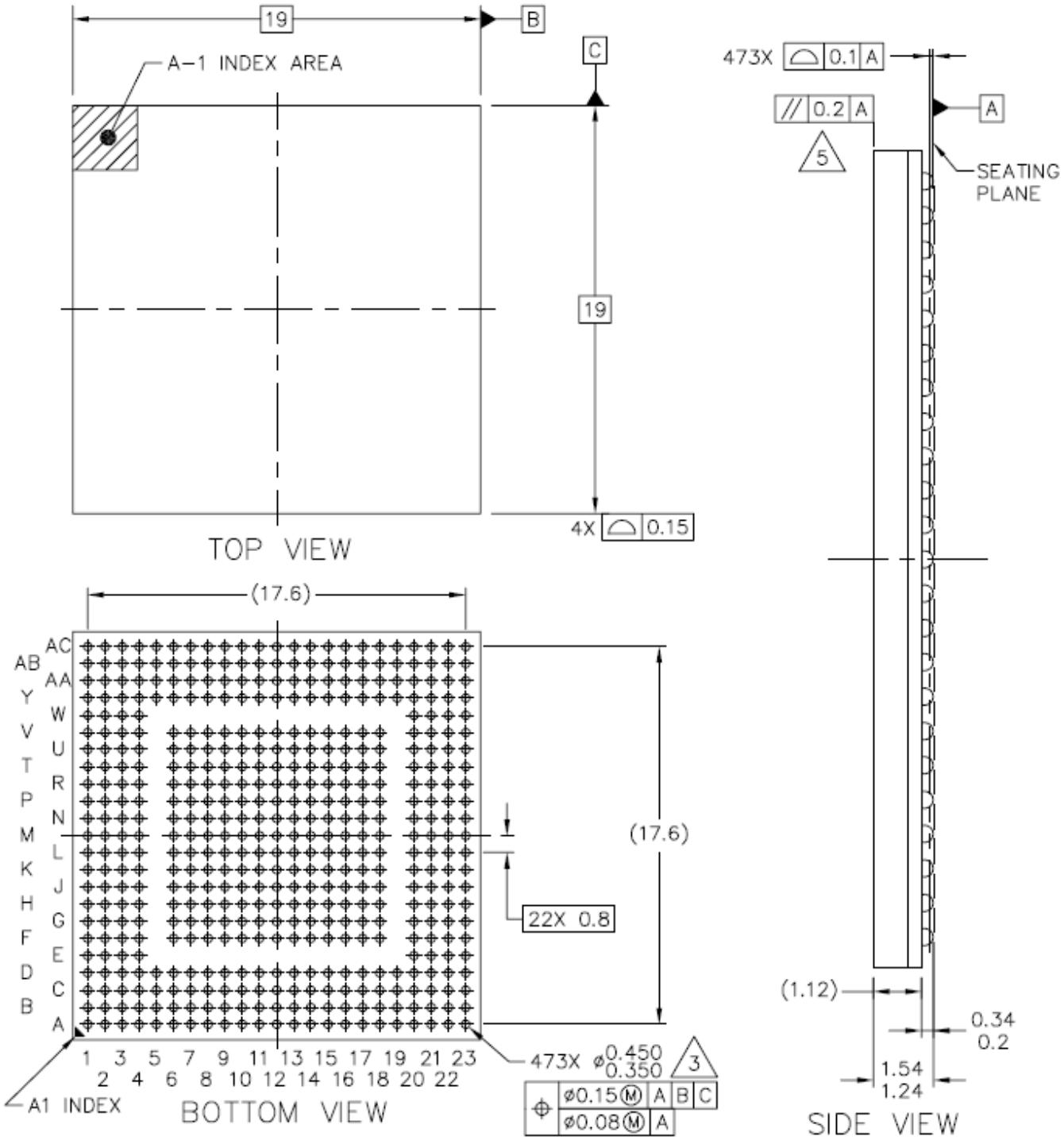


Figure 52. Mechanical Dimension and Bottom Surface Nomenclature of the MPC8308 MAPBG

Notes:
1. All dimensions are in millimeters.

2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

20.3 Pinout Listings

Table 53 provides the pin-out listing for the MPC8308, MAPBGA package.

Table 53. MPC8308 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ[0]	V6	I/O	GV_{DDA}	—
MEMC_MDQ[1]	Y4	I/O	GV_{DDA}	—
MEMC_MDQ[2]	AB3	I/O	GV_{DDA}	—
MEMC_MDQ[3]	AA3	I/O	GV_{DDA}	—
MEMC_MDQ[4]	AA2	I/O	GV_{DDA}	—
MEMC_MDQ[5]	AA1	I/O	GV_{DDA}	—
MEMC_MDQ[6]	W4	I/O	GV_{DDA}	—
MEMC_MDQ[7]	Y2	I/O	GV_{DDA}	—
MEMC_MDQ[8]	W3	I/O	GV_{DDA}	—
MEMC_MDQ[9]	W1	I/O	GV_{DDA}	—
MEMC_MDQ[10]	Y1	I/O	GV_{DDA}	—
MEMC_MDQ[11]	W2	I/O	GV_{DDA}	—
MEMC_MDQ[12]	U4	I/O	GV_{DDA}	—
MEMC_MDQ[13]	U3	I/O	GV_{DDA}	—
MEMC_MDQ[14]	V4	I/O	GV_{DDA}	—
MEMC_MDQ[15]	U6	I/O	GV_{DDA}	—
MEMC_MDQ[16]	T3	I/O	GV_{DDB}	—
MEMC_MDQ[17]	T2	I/O	GV_{DDB}	—
MEMC_MDQ[18]	R4	I/O	GV_{DDB}	—
MEMC_MDQ[19]	R3	I/O	GV_{DDB}	—
MEMC_MDQ[20]	P4	I/O	GV_{DDB}	—
MEMC_MDQ[21]	N6	I/O	GV_{DDB}	—
MEMC_MDQ[22]	P2	I/O	GV_{DDB}	—
MEMC_MDQ[23]	P1	I/O	GV_{DDB}	—
MEMC_MDQ[24]	N4	I/O	GV_{DDB}	—
MEMC_MDQ[25]	N3	I/O	GV_{DDB}	—
MEMC_MDQ[26]	N2	I/O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MDQ[27]	M6	I/O	GV_{DDB}	—
MEMC_MDQ[28]	M2	I/O	GV_{DDB}	—
MEMC_MDQ[29]	M3	I/O	GV_{DDB}	—
MEMC_MDQ[30]	L2	I/O	GV_{DDB}	—
MEMC_MDQ[31]	L3	I/O	GV_{DDB}	—
MEMC_MDM[0]	AB2	O	GV_{DDA}	—
MEMC_MDM[1]	V3	O	GV_{DDA}	—
MEMC_MDM[2]	P3	O	GV_{DDB}	—
MEMC_MDM[3]	M7	O	GV_{DDB}	—
MEMC_MDM[8]	K2	O	GV_{DDB}	—
MEMC_MDQS[0]	AC3	I/O	GV_{DDA}	—
MEMC_MDQS[1]	V1	I/O	GV_{DDA}	—
MEMC_MDQS[2]	R1	I/O	GV_{DDB}	—
MEMC_MDQS[3]	M1	I/O	GV_{DDB}	—
MEMC_MDQS[8]	K1	I/O	GV_{DDB}	—
MEMC_MBA[0]	C3	O	GV_{DDB}	—
MEMC_MBA[1]	B2	O	GV_{DDB}	—
MEMC_MBA[2]	H4	O	GV_{DDB}	—
MEMC_MA0	C2	O	GV_{DDB}	—
MEMC_MA1	D2	O	GV_{DDB}	—
MEMC_MA2	D3	O	GV_{DDB}	—
MEMC_MA3	D4	O	GV_{DDB}	—
MEMC_MA4	E4	O	GV_{DDB}	—
MEMC_MA5	F4	O	GV_{DDB}	—
MEMC_MA6	E2	O	GV_{DDB}	—
MEMC_MA7	E1	O	GV_{DDB}	—
MEMC_MA8	F2	O	GV_{DDB}	—
MEMC_MA9	F3	O	GV_{DDB}	—
MEMC_MA10	C1	O	GV_{DDB}	—
MEMC_MA11	F7	O	GV_{DDB}	—
MEMC_MA12	G2	O	GV_{DDB}	—
MEMC_MA13	G3	O	GV_{DDB}	—
$\overline{\text{MEMC_MWE}}$	D5	O	GV_{DDB}	—
$\overline{\text{MEMC_MRAS}}$	B4	O	GV_{DDB}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MEMC_MCAS}}$	C5	O	GV_{DDB}	—
$\overline{\text{MEMC_MCS}}$[0]	B6	O	GV_{DDB}	—
$\overline{\text{MEMC_MCS}}$[1]	C6	O	GV_{DDB}	—
MEMC_MCKE	H3	O	GV_{DDB}	3
MEMC_MCK [0]	A3	O	GV_{DDB}	—
MEMC_MCK [1]	U2	O	GV_{DDB}	—
MEMC_MCK [2]	G1	O	GV_{DDB}	—
$\overline{\text{MEMC_MCK}}$ [0]	A4	O	GV_{DDB}	—
$\overline{\text{MEMC_MCK}}$ [1]	U1	O	GV_{DDB}	—
$\overline{\text{MEMC_MCK}}$ [2]	H1	O	GV_{DDB}	—
MEMC_MODT[0]	A5	O	GV_{DDB}	—
MEMC_MODT[1]	B5	O	GV_{DDB}	—
MEMC_MECC[0]	L4	I/O	GV_{DDB}	—
MEMC_MECC[1]	L6	I/O	GV_{DDB}	—
MEMC_MECC[2]	K4	I/O	GV_{DDB}	—
MEMC_MECC[3]	K3	I/O	GV_{DDB}	—
MEMC_MECC[4]	J2	I/O	GV_{DDB}	—
MEMC_MECC[5]	K6	I/O	GV_{DDB}	—
MEMC_MECC[6]	J3	I/O	GV_{DDB}	—
MEMC_MECC[7]	J6	I/O	GV_{DDB}	—
MV_{REF}	G6	I	GV_{DDB}	—
Local Bus Controller Interface				
LD0	U18	I/O	NV_{DDP_K}	8
LD1	V18	I/O	NV_{DDP_K}	8
LD2	U16	I/O	NV_{DDP_K}	8
LD3	Y20	I/O	NV_{DDP_K}	8
LD4	AA21	I/O	NV_{DDP_K}	8
LD5	AC22	I/O	NV_{DDP_K}	8
LD6	V17	I/O	NV_{DDP_K}	8
LD7	AB21	I/O	NV_{DDP_K}	8
LD8	Y19	I/O	NV_{DDP_K}	8
LD9	AA20	I/O	NV_{DDP_K}	8
LD10	Y17	I/O	NV_{DDP_K}	8

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LD11	AC21	I/O	NV_{DDP_K}	8
LD12	AB20	I/O	NV_{DDP_K}	8
LD13	V16	I/O	NV_{DDP_K}	8
LD14	AA19	I/O	NV_{DDP_K}	8
LD15	AC17	I/O	NV_{DDP_K}	8
LA0	AC20	O	NV_{DDP_K}	—
LA1	Y16	O	NV_{DDP_K}	—
LA2	U15	O	NV_{DDP_K}	—
LA3	V15	O	NV_{DDP_K}	—
LA4	AA18	O	NV_{DDP_K}	—
LA5	AA17	O	NV_{DDP_K}	—
LA6	AC19	O	NV_{DDP_K}	—
LA7	AA16	O	NV_{DDP_K}	—
LA8	AB18	O	NV_{DDP_K}	—
LA9	AC18	O	NV_{DDP_K}	—
LA10	V14	O	NV_{DDP_K}	—
LA11	AB17	O	NV_{DDP_K}	—
LA12	AA15	O	NV_{DDP_K}	—
LA13	AC16	O	NV_{DDP_K}	—
LA14	Y14	O	NV_{DDP_K}	—
LA15	AC15	O	NV_{DDP_K}	—
LA16	U13	O	NV_{DDP_K}	—
LA17	V13	O	NV_{DDP_K}	—
LA18	Y13	O	NV_{DDP_K}	—
LA19	AB15	O	NV_{DDP_K}	—
LA20	AA14	O	NV_{DDP_K}	—
LA21	AB14	O	NV_{DDP_K}	—
LA22	U12	O	NV_{DDP_K}	—
LA23	V12	O	NV_{DDP_K}	—
LA24	Y12	O	NV_{DDP_K}	—
LA25	AC14	O	NV_{DDP_K}	—
$\overline{\text{LCS}}$[0]	AA13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[1]	AB13	O	NV_{DDP_K}	4
$\overline{\text{LCS}}$[2]	AA12	O	NV_{DDP_K}	4

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS}}$[3]	Y11	O	NV_{DDP_K}	4
$\overline{\text{LWE}}$[0] /$\overline{\text{LFWE}}$0/$\overline{\text{LBS}}$0	AB11	O	NV_{DDP_K}	—
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$1	AC11	O	NV_{DDP_K}	—
LBCTL	U11	O	NV_{DDP_K}	—
LGPL0/LFCLE	Y10	O	NV_{DDP_K}	—
LGPL1/LFALE	AA10	O	NV_{DDP_K}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AB10	O	NV_{DDP_K}	4
LGPL3/$\overline{\text{LFWP}}$	AC10	O	NV_{DDP_K}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$	AB9	I/O	NV_{DDP_K}	4
LGPL5	Y9	O	NV_{DDP_K}	—
LCLK0	AC12	O	NV_{DDP_K}	—
DUART				
UART_SOUT1/MSRCID0/LSRCID0	C17	O	NV_{DDB}	—
UART_SIN1/MSRCID1/LSRCID1	B18	I/O	NV_{DDB}	—
UART_SOUT2/MSRCID2/LSRCID2	D17	O	NV_{DDB}	—
UART_SIN2/MSRCID3/LSRCID3	D18	I/O	NV_{DDB}	—
PEX PHY				
TXA	C14	O	XPADVDD	—
$\overline{\text{TXA}}$	C15	O	XPADVDD	—
RXA	A13	I	XCOREVDD	—
$\overline{\text{RXA}}$	B13	I	XCOREVDD	—
SD_IMP_CAL_RX	A15	I	XCOREVDD	—
$\overline{\text{SD_REF_CLK}}$	C12	I	XCOREVDD	—
SD_REF_CLK	D12	I	XCOREVDD	—
SD_PLL_TPD	F13	O	—	—
SD_IMP_CAL_TX	A11	I	XPADVDD	—
SD_PLL_TPA_ANA	F11	O	—	—
SDAVDD_0	G12	I	—	—
SDAVSS_0	F12	I	—	—
I^2C interface				
IIC_SDA1	C9	I/O	NV_{DDA}	2
IIC_SCL1	A9	I/O	NV_{DDA}	2

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IIC_SDA2/$\overline{\text{CKSTOP_OUT}}$	D10	I/O	NV_{DDA}	2
IIC_SCL2/$\overline{\text{CKSTOP_IN}}$	C10	I/O	NV_{DDA}	2
Interrupts				
IRQ[0]/$\overline{\text{MCP_IN}}$	A17	I	NV_{DDB}	—
IRQ[1]/$\overline{\text{MCP_OUT}}$	F16	I/O	NV_{DDB}	—
IRQ[2] /$\overline{\text{CKSTOP_OUT}}$	B17	I/O	NV_{DDB}	—
IRQ[3] /$\overline{\text{CKSTOP_IN}}$	A18	I	NV_{DDB}	—
JTAG				
TCK	Y7	I	NV_{DDP_K}	—
TDI	U9	I	NV_{DDP_K}	4
TDO	AC5	O	NV_{DDP_K}	3
TMS	AA6	I	NV_{DDP_K}	4
$\overline{\text{TRST}}$	V8	I	NV_{DDP_K}	4
TEST				
TEST_MODE	AC6	I	NV_{DDP_K}	5
System Control				
$\overline{\text{HRESET}}$	AA9	I/O	NV_{DDP_K}	1
$\overline{\text{PORESET}}$	AA8	I	NV_{DDP_K}	—
$\overline{\text{SRESET}}$	AB7	I/O	NV_{DDP_K}	—
Clocks				
SYS_CLK_IN	AC8	I	NV_{DDP_K}	—
RTC_PIT_CLOCK	AA23	I	NV_{DDJ}	—
MISC				
$\overline{\text{QUIESCE}}$	AA7	O	NV_{DDP_K}	—
THERM0	AC7	I	NV_{DDP_K}	6
ETSEC1				
TSEC1_COL	B20	I	NV_{DDC}	—
TSEC1_CRS	B21	I	NV_{DDC}	—
TSEC1_GTX_CLK	F18	O	NV_{DDC}	3
TSEC1_RX_CLK	A22	I	NV_{DDC}	—
TSEC1_RX_DV	D21	I	NV_{DDC}	—
TSEC1_RXD[3]	C22	I	NV_{DDC}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RXD[2]	C21	I	NV_{DDC}	—
TSEC1_RXD[1]	C20	I	NV_{DDC}	—
TSEC1_RXD[0]	D20	I	NV_{DDC}	—
TSEC1_RX_ER	C23	I	NV_{DDC}	—
TSEC1_TX_CLK/TSEC1_GTX_CLK125	E23	I	NV_{DDC}	—
TSEC1_TXD[3]/CFG_RESET_SOURCE[0]	F22	I/O	NV_{DDC}	—
TSEC1_TXD[2]/CFG_RESET_SOURCE[1]	F21	I/O	NV_{DDC}	—
TSEC1_TXD[1]/CFG_RESET_SOURCE[2]	E21	I/O	NV_{DDC}	—
TSEC1_TXD[0]/CFG_RESET_SOURCE[3]	D22	I/O	NV_{DDC}	—
TSEC1_TX_EN/LBC_PM_REF_10	F20	O	NV_{DDC}	—
TSEC1_TX_ER/LB_POR_CFG_BOOT_ECC	E22	I/O	NV_{DDC}	7
Ethernet Mgmt				
TSEC1_MDC	A20	O	NV_{DDB}	—
TSEC1_MDIO	C19	I/O	NV_{DDB}	2
eSDHC/GTM				
SD_CLK/GPIO_16	D7	O	NV_{DDA}	—
SD_CMD/GPIO_17	G9	I/O	NV_{DDA}	—
$\overline{\text{SD_CD}}$/GTM1_TIN1/GPIO_18	A7	I	NV_{DDA}	—
SD_WP/$\overline{\text{GTM1_TGATE1}}$/GPIO_19	D8	I	NV_{DDA}	—
SD_DAT[0]/$\overline{\text{GTM1_TOUT1}}$/GPIO_20	C8	I/O	NV_{DDA}	—
SD_DAT[1]/$\overline{\text{GTM1_TOUT2}}$/GPIO_21	B8	I/O	NV_{DDA}	—
SD_DAT[2]/GTM1_TIN2/GPIO_22	A8	I/O	NV_{DDA}	—
SD_DAT[3]/$\overline{\text{GTM1_TGATE2}}$/GPIO_23	B9	I/O	NV_{DDA}	—
SPI				
SPIMOSI/MSRCID4/LSRCID4	AB5	I/O	NV_{DDP_K}	—
SPIMISO/MDVAL/LDVAL	Y6	I/O	NV_{DDP_K}	—
SPICLK	AA5	I/O	NV_{DDP_K}	—
SPISEL	AB4	I	NV_{DDP_K}	—
GPIO/ETSEC2				
GPIO[0]/TSEC2_COL	G21	I/O	NV_{DDF}	—
GPIO[1]/TSEC2_TX_ER	K23	I/O	NV_{DDF}	—
GPIO[2]/TSEC2_GTX_CLK	H18	I/O	NV_{DDF}	—
GPIO[3]/TSEC2_RX_CLK	G23	I/O	NV_{DDF}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO[4]/TSEC2_RX_DV	J18	I/O	NV_{DDF}	—
GPIO[5]/TSEC2_RXD3	J20	I/O	NV_{DDF}	—
GPIO[6]/TSEC2_RXD2	H22	I/O	NV_{DDF}	—
GPIO[7]/TSEC2_RXD1	H21	I/O	NV_{DDF}	—
GPIO[8]/TSEC2_RXD0	H20	I/O	NV_{DDF}	—
GPIO[9]/TSEC2_RX_ER	J21	I/O	NV_{DDF}	—
GPIO[10]/TSEC2_TX_CLK/TSEC2_GTX_CLK125	J23	I/O	NV_{DDF}	—
GPIO[11]/TSEC2_TXD3	K22	I/O	NV_{DDF}	—
GPIO[12]/TSEC2_TXD2	K20	I/O	NV_{DDF}	—
GPIO[13]/TSEC2_TXD1	K18	I/O	NV_{DDF}	—
GPIO[14]/TSEC2_TXD0	J17	I/O	NV_{DDF}	—
GPIO[15]/TSEC2_TX_EN	K21	I/O	NV_{DDF}	—
USB/IEEE1588/GTM				
USBDR_PWR_FAULT	P20	I	NV_{DDH}	—
USBDR_CLK	R23	I	NV_{DDH}	—
USBDR_DIR	R21	I	NV_{DDH}	—
USBDR_NXT	P18	I	NV_{DDH}	—
USBDR_TXDRXD0	T22	I/O	NV_{DDH}	—
USBDR_TXDRXD1	T21	I/O	NV_{DDH}	—
USBDR_TXDRXD2	U23	I/O	NV_{DDH}	—
USBDR_TXDRXD3	U22	I/O	NV_{DDH}	—
USBDR_TXDRXD4	T20	I/O	NV_{DDH}	—
USBDR_TXDRXD5	R18	I/O	NV_{DDH}	—
USBDR_TXDRXD6	V23	I/O	NV_{DDH}	—
USBDR_TXDRXD7	V22	I/O	NV_{DDH}	—
USBDR_PCTL0	R17	O	NV_{DDH}	—
USBDR_PCTL1	U20	O	NV_{DDH}	—
USBDR_STP	V21	O	NV_{DDH}	—
TSEC_TMR_CLK/ GPIO[8]	W23	I	NV_{DDH}	—
$\overline{\text{GTM1_TOUT3}}$/ GPIO[9]	T18	O	NV_{DDH}	—
$\overline{\text{GTM1_TOUT4}}$/ GPIO[10]	V20	O	NV_{DDH}	—
TSEC_TMR_TRIG1/ GPIO[11]	W21	I	NV_{DDH}	—
TSEC_TMR_TRIG2/ GPIO[12]	Y21	I	NV_{DDH}	—
TSEC_TMR_GCLK	L17	O	NV_{DDG}	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC_TMR_PP1	L18	O	NV_{DDG}	—
TSEC_TMR_PP2	L21	O	NV_{DDG}	—
TSEC_TMR_PP3/ GPIO[13]	L22	O	NV_{DDG}	—
TSEC_TMR_ALARM1	L23	O	NV_{DDG}	—
TSEC_TMR_ALARM2/ GPIO[14]	M23	O	NV_{DDG}	—
GPIO[7]	M22	O	—	—
TSEC2_CRS	M21	O	NV_{DDG}	—
TSEC2_TMR_RX_ESFD/ GPIO[1]	M18	O	NV_{DDG}	—
TSEC2_TMR_TX_ESFD/GPIO[2]	M20	O	NV_{DDG}	—
TSEC1_TMR_RX_ESFD/GPIO[3]	N23	O	NV_{DDG}	—
TSEC1_TMR_TX_ESFD/ GPIO[4]	N21	O	NV_{DDG}	—
$\overline{\text{GTM1_TGATE3}}$	N20	I	NV_{DDG}	—
GTM1_TIN4	N18	I	NV_{DDG}	—
$\overline{\text{GTM1_TGATE4}}$/ GPIO[15]	P23	I	NV_{DDG}	—
GTM1_TIN3	P22	I	NV_{DDG}	—
GPIO[5]	N17	I	NV_{DDH}	—
GPIO[6]	P21	I	NV_{DDH}	—
Power and Ground Supplies				
AV_{DD1}	R6	I	—	—
AV_{DD2}	V10	I	—	—
NC, No Connection	Y23, B11, B16, D16	—	—	—
V_{DD}	H8, H9, H10, H14, H15, H16, J8, J16, K8, K16, L8, L16, M8, M16, N8, N16, P8, P16, R8, R16, T8, T9, T10, T11, T12, T13, T14, T15, T16	I	—	—

Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
VSS	A2, A21, B1, B19, B23, C4, C16, D6, D19, E3, F8, F15, F17, F23, G7, G8, G10, G15, G16, G17, G20, H2, H6, H7, H17, H23, J7, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, K15, L1, L7, L9, L10, L11, L12, L13, L14, L15, L20, M4, M9, M10, M11, M12, M13, M14, M15, N9, N10, N11, N12, N13, N14, N15, P6, P7, P9, P10, P11, P12, P13, P14, P15, R2, R7, R9, R10, R11, R12, R13, R14, R15, R22, T6, T7, U8, U17, U21, V2, V7, V9, V11, W20, Y8, Y15, AA4, AB1, AB6, AB12, AB19, AC2, AC9, AC23	I	—	—
NV_{DDA}	B7, B10, C7, D9, F9	I	—	—
NV_{DDB}	A16, A19, C18	I	—	—
NV_{DDC}	A23, B22, D23, E20, G18	I	—	—
NV_{DDF}	G22, J22, K17	I	—	—
NV_{DDG}	M17, N22	I	—	—
NV_{DDH}	P17, R20, T17, T23, W22, Y22	I	—	—
NV_{DDJ}	AB23, AA22	I	—	—
NV_{DDP_K}	U10, U14, Y5, Y18, AA11, AB8, AB16, AB22, AC4, AC13	I	—	—
GV_{DD}	A1, A6, B3, D1, F1, F6, G4, J1, J4, K7, N1, N7, T1, T4, U7, Y3, AC1	I	—	—
XPADVDD	D15, F10, F14	I	—	—
XPADVSS	A10, B15, D14, G13, G14, H12	I	—	—

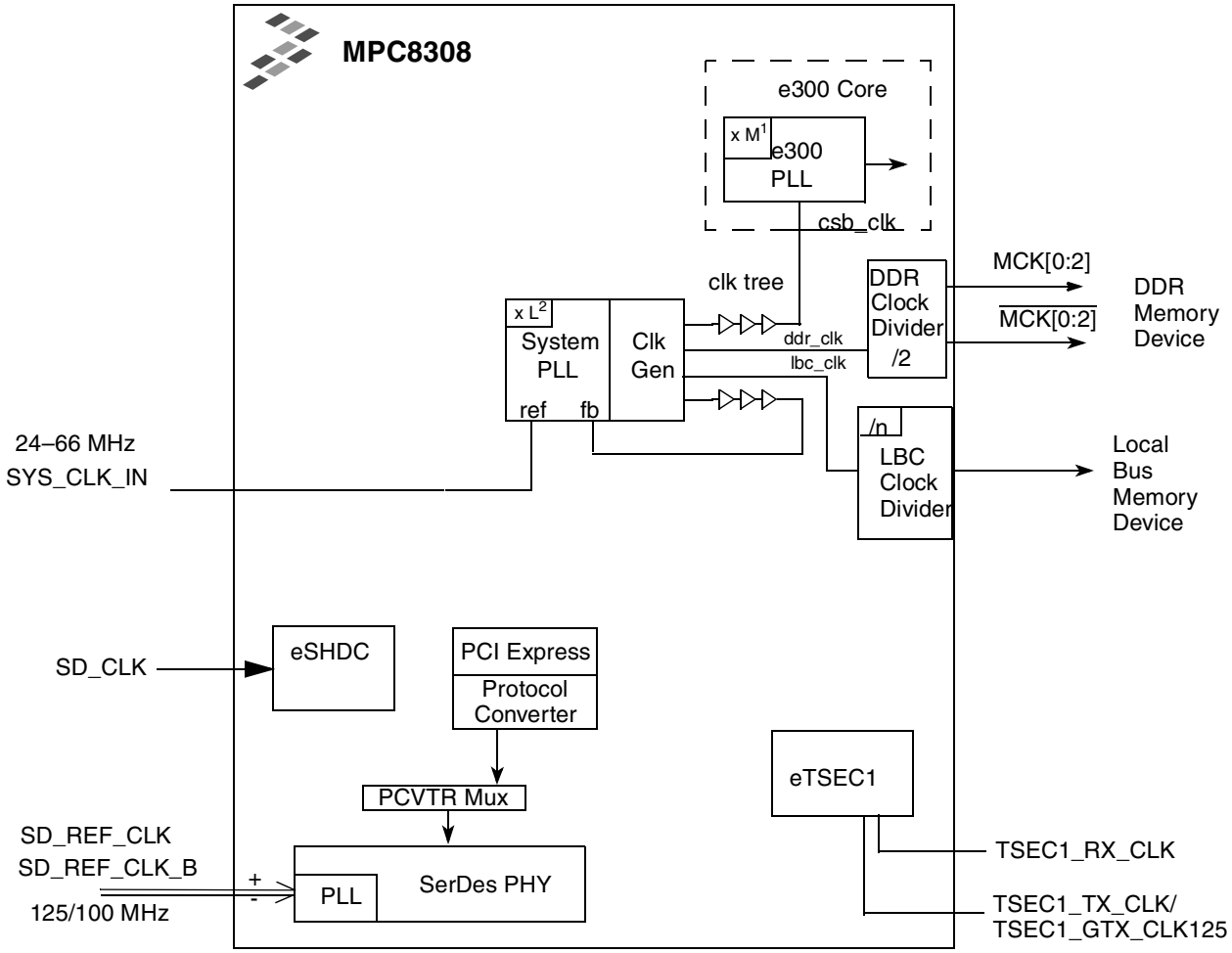
Table 53. MPC8308 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
XCOREVDD	A14, B12, C13	I	—	—
XCOREVSS	A12, B14, C11, D11, D13, G11, H11, H13	I	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. This pin has weak internal pull-up that is always enabled. 5. This pin must always be tied to VSS.
6. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
7. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a buffer released to high impedance is needed.
8. This pin has weak internal pull-down that is always enabled

21 Clocking

Figure 53 shows the internal distribution of clocks within the device.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4, 5 and 6. Value is decided by RCWLR[SPMF].

Figure 53. MPC8308 Clock Subsystem

The following external clock sources are utilized on the MPC8308:

- System clock (SYS_CLK_IN)
- Ethernet Clock (TSEC1_RX_CLK/TSEC1_TX_CLK/TSEC1_GTX_CLK125 for eTSEC)
- SerDes PHY clock
- eSHDC clock (SD_CLK)

  For more information, see the SerDes chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

All clock inputs can be supplied using an external canned oscillator, a clock generation chip, or some other source that provides a standard CMOS square wave input.

21.1 System Clock Domains

The primary clock input (SYS_CLK_IN) frequency is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus interface unit (*lbc_clk*)

The *csb_clk* frequency is derived as follows:

csb_clk = [SYS_CLK_IN] × SPMF

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset Clock Configuration chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK0:2). The LBC clock divider ratio is controlled by LCCR[CLKDIV]. For more information, see the Reset Clock Configuration chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory-mapped register after the device comes out of reset. Table 54 specifies which units have a configurable clock frequency. For more information, see Reset Clock Configuration chapter in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

Table 54. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1,eTSEC2	*csb_clk/3*	Off, *csb_clk, csb_clk/2, csb_clk/3*
I^2C	*csb_clk*	Off, *csb_clk,csb_clk*/2, *csb_clk*/3
DMA complex	*csb_clk*	Off, *csb_clk,csb_clk/2,csb_clk/3*
PCIEXP	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
eSDHC	*csb_clk*	Off*, csb_clk, csb_clk/2, csb_clk/3*
USB	*csb_clk*	Off*, csb_clk, csb_clk/2, csb_clk/3*

NOTE

The clock ratios of these units must be set before they are accessed.

Table 55 provides the operating frequencies for the device under recommended operating conditions (Table 2).

Table 55. Operating Frequencies for MPC8308

Characteristic[1]	Maximum Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*0*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK0, and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCCR[CLKDIV]) which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

21.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Ratio

RCWL[SPMF]	csb_clk : SYS_CLK_IN
0000	Reserved
0001	Reserved
0010	2 : 1
0011	3 : 1
0100	4 : 1
0101	5 : 1
0110–1111	Reserved

As described in Section 21, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (SYS_CLK_IN) and the internal

coherent system bus clock (*csb_clk*). Table 57 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN ratios.

Table 57. CSB Frequency Options

SPMF *csb_clk* :Input Clock Ratio		Input Clock Frequency (MHz)		
		25	33.33	66.67
0010	2:1			133
0100	4:1		133	
0101	5:1	125		

21.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 58 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 58 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 58. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk: csb_clk* Ratio[1]	VCO Divider (VCOD)[2]
0–1	2–5	6		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4

Table 58. e300 Core PLL Configuration (continued)

RCWL[COREPLL]			*core_clk: csb_clk* Ratio[1]	VCO Divider (VCOD)[2]
0–1	2–5	6		
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Notes:

1 For any *core_clk:csb_clk* ratios, the *core_clk* must not exceed its maximum operating frequency of 333 MHz.
2 Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

22 Thermal

This section describes the thermal specifications of the device.

22.1 Thermal Characteristics

Table 59 provides the package thermal characteristics for the 473, 19 × 19 mm MAPBGA.

Table 59. Package Thermal Characteristics for MAPBGA

Characteristic	Board Type	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	42	°C/W	1,2
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	27	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	35	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	17	°C/W	4
Junction to Case	—	$R_{\theta JC}$	9	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Table 59. Package Thermal Characteristics for MAPBGA (continued)

Characteristic	Board Type	Symbol	Value	Unit	Notes

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying

the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the device

23.1 System Clocking

The device includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 21.2, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.3, “Core PLL Configuration.”

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} for core PLL and AV_{DD2} for the platform PLL). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low-pass filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 54, one to each of the two AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs’ resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 54 shows the PLL power supply filter circuits.

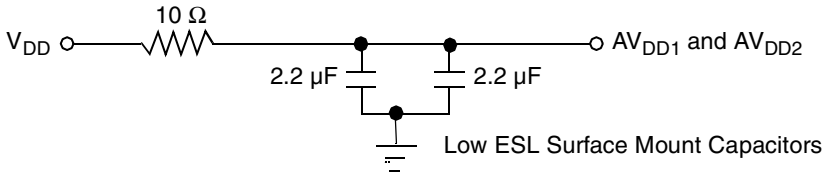


Figure 54. PLL Power Supply Filter Circuit

23.3 Decoupling Recommendations

Due to large address and data buses and high-operating frequencies, the device can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8308 system, and the MPC8308 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, NV_{DD}, GV_{DD}, and LV_{DD} pin of the device.

These decoupling capacitors should receive their power from separate V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, and V_{SS} power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, NV_{DD}, GV_{DD}, LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are in the range of 100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, and LV_{DD} as required. Unused active high inputs should be connected to VSS. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, AV_{DD1}, AV_{DD2}, GV_{DD}, LV_{DD}, and V_{SS} pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push–pull single-ended driver type (open drain for I^2C, MDIO, and HRESET).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (Figure 55). The output impedance is the average of two components: the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

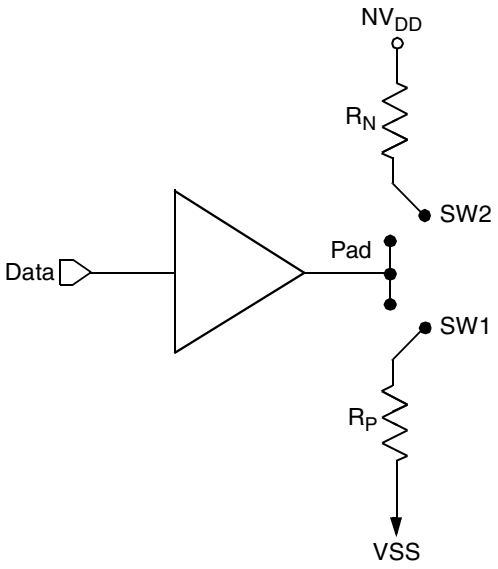


Figure 55. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 60 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal NV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	Ω
R_P	42 Target	20 Target	Z_0	Ω

Note: Nominal supply voltages. See Table 2, T_j = 105°C.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 KΩ on certain output pins (see customer-visible configuration pins). These pins are generally used as output-only pins in normal operation.

While $\overline{\text{PORESET}}$ is asserted, these pins are treated as inputs. The value presented on these pins while $\overline{\text{PORESET}}$ is asserted is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

23.7 Pull-Up Resistor Requirements

The device requires high-resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C, Ethernet management MDIO, $\overline{\text{HRESET}}$ and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 56. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion that give unpredictable results.

24 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 24.1, "Part Numbers Fully Addressed by This Document."

24.1 Part Numbers Fully Addressed by This Document

Table 61 provides the Freescale part numbering nomenclature for the MPC8308 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed. Each part number also contains a revision code which refers to the die mask revision number.

Table 61. Part Numbering Nomenclature

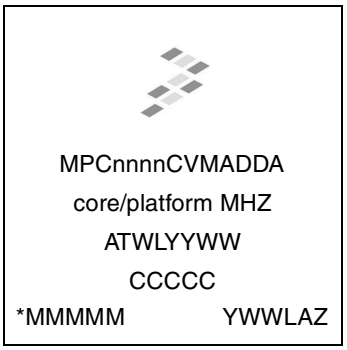
MPC	*nnnn*	*C*	*VM*	*AD*	*D*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR Frequency**	**Revision Level**
MPC	8308	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free 473 MAPBGA	AD = 266 MHz AF = 333 MHz AG = 400MHz	D = 266 MHz	Contact local Freescale sales office

Notes:

1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 20, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

24.2 Part Marking

Parts are marked as in the example shown in Figure 56.



Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 56. Freescale Part Marking for PBGA Devices

Table 62 shows the SVR settings.

Table 62. SVR Settings

Device	Package	SVR
MPC8308	MAPBGA	0x8101 _0110

Note: PVR = 8085_0020 for the device.

25 Document Revision History

Table 63 provides a revision history for this hardware specification.

Table 63. Document Revision History

Revision	Date	Substantive Change(s)
Rev 1	07/2010	• In "Table 4," TA = 105 replaced with TJ = 105 • In "Table 8," fSYS_CLK_IN (Max) = 66 replaced with 66.67 and tSYS_CLK_IN (Min) = 15.15 replaced with 15 • In "Table 53," TSEC1_TMR_RX_ESFD replaced with TSEC2_TMR_RX_ESFD TSEC1_TMR_TX_ESFD replaced with TSEC2_TMR_TX_ESFD TSEC0_TMR_RX_ESFD replaced with TSEC1_TMR_RX_ESFD TSEC0_TMR_TX_ESFD replaced with TSEC1_TMR_TX_ESFD • In "Table 56," rows from 1000 to 1111 removed
Rev 0	05/2010	Initial release

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