MPC823ETS/D
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PowerPC™

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Technical Summary

MPC823e Mobile Computing Microprocessor

The MPC823e microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of electronic products. It particularly excels in low-power, portable, image capture and personal communication products. It is a version of the MPC823 microprocessor that provides enhanced performance with larger data and instruction caches. Like the MPC823, it has a universal serial bus (USB) interface and video display controller, as well as the existing LCD controller of the MPC823 (Rev A) device.

The MPC823e microprocessor integrates a high-performance embedded PowerPC™ core with a communication processor module that uses a specialized RISC processor for imaging and communication. The communication processor module can perform embedded signal processing functions for image compression and decompression. It also supports seven serial channels—two serial communication controllers, two serial management controllers, one I^2C® port, one USB channel, and one serial peripheral interface.

This two-processor architecture consumes power more efficiently than traditional architectures because the communication processor module frees the core from peripheral tasks like imaging and communication.

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Key Features

The following list summarizes key features of the MPC823e:

- Embedded PowerPC Core Provides 99MIPS (Using Dhrystone 2.1) or 172K Dhrystones 2.1 at 75MHz
  - — Single-Issue, 32-Bit Version of the PowerPC Core (Fully Compatible with the PowerPC Architecture Definition) with 32 x 32-Bit Fixed-Point Registers
  - — Low Power Consumption, 3.3V I/O Boundary with Microprocessor Core, Caches, Memory Management, and I/O in Operation
  - — Performs Branch Folding, Branch Prediction with Conditional Prefetch, without Conditional Execution
  - — 8K Data Cache and 16K Instruction Cache
  - — Instruction Cache is Four-Way, Set Associative and the Data Cache is Two-Way, Set-Associative, Physical Address, 4-Word Line Burst, LRU Replacement Algorithm, Lockable Online Granularity
  - — Memory Management Units with 32-Entry Translation Lookaside Buffers (TLBs) and Fully Associative Instruction and Data TLBs
  - — Memory Management Units Support Multiple Page Sizes of 4K, 16K, 512K and 8M (1K Protection Granularity at the 4K Page Size); 16 Virtual Address Spaces and 16 Protection Groups
- Advanced On-Chip Emulation Debug Mode
- Data Bus Dynamic Bus Sizing for 8-,16-, and 32-Bit Buses
  - — Supports Traditional 68K Big-Endian, Traditional x86 Little-Endian, and PowerPC Little-Endian Memory Systems
  - — Twenty-Six External Address Lines
- Completely Static Design (0–75MHz Operation)
  - — External Bus Division Factor (EBDF) Should be Divided by 2 for Frequencies Greater than 50MHz
- Communication Processor Module
  - — Interfaces to PowerPC Core through On-Chip Dual-Access RAM and Virtual (Serial) DMA Channels on a Dedicated DMA Accelerator
  - — Programmable Memory-to-Memory and Memory-to-I/O (including Flyby) DMA Provided by Virtual DMA Support
  - — CPM Provides 75+MIPS @ 75MHz in Parallel with PowerPC Core
  - — Protocols Supported by ROM or Download Microcode and the Hardware Serial Communication Controllers Include, but are not Limited to, the Digital Portions of:
    - – Ethernet/IEEE 802.3 (CS/CDMA)
    - – HDLC/SDLC and HDLC Bus
    - – AppleTalk®
    - – Universal Asynchronous Receiver Transmitter (UART)
    - – Synchronous UART (USART)
    - – Totally Transparent Mode With/Without CRC
    - – Asynchronous HDLC
    - – IrDA Version 1.1 Serial Infrared (SCC2 only)
    - – Basic Rate ISDN (BRI) in Conjunction with Serial Management Controller Channels
    - – Primary Rate ISDN

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  - 16 x 16-Bit Multiply-Accumulate (MAC) Hardware
    - One Operation Per Clock
    - Two Clock Latency and One Clock Blockage
    - Operates Concurrently with Other Instructions
    - Uses DMA Controller to Burst Data Directly into Register File without Interacting with the PowerPC Core
  - 8K Dual-Port RAM
  - Twelve Serial DMA (SDMA) Channels
  - 32-Bit, Harvard Architecture, Scalar RISC Microcontroller
  - Communication-Specific Commands
  - Supports Continuous-Mode Transmission and Reception on All Serial Channels
  - Each Serial Channel has Externally Accessible Pins
- Four Baud Rate Generators
  - Independent and Can be Connected to a Serial Communication Controller or Serial Management Controller
  - Allows Changes During Operation
  - Autobaud Support Option
- Two Serial Communication Controllers (SCCs)
  - Ethernet/IEEE 802.3 Support (10Mbps and Full-Duplex Operation)
  - GeoPort Support
  - HDLC Bus Implements an HDLC-Based Local Area Network
  - Universal Asynchronous Receiver Transmitter
  - Synchronous UART
  - Serial Infrared (IrDA) Supporting a Maximum of 4Mbps (SCC2 Only)
  - Totally Transparent. Frame-Based with Optional Cyclical Redundancy Check
  - Maximum Serial Data Rate of 35Mbps
- One Dedicated High-Speed Serial Channel for the Universal Serial Bus (USB)
  - Supports USB Host/Slave Modes at a Maximum of 12Mbps with Four USB Endpoints
- Two Serial Management Controllers (SMCs) with Externally Accessible Pins
  - UART
  - Transparent
  - General Circuit Interface (GCI) Controller
  - Can Be Connected to the Time-Division Multiplexed (TDM) Channel
- One Serial Peripheral Interface
  - Supports Master and Slave Modes
  - Supports Multimaster Operation on the Same Bus
- One I^2C Port
  - Supports Master and Slave Modes
  - Supports Multimaster Environments
  - Supports High-Speed Operation
  - Supports 7-Bit Addressing

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- Serial Interface with the Two Time-Slot Assigners
  - — Allows Serial Communication Controllers and Serial Management Controllers to be Used in Multiplexed and/or Nonmultiplexed Operation
  - — Supports T1, CEPT, PCM Highway, ISDN Basic Rate, ISDN Primary Rate, User-Defined
  - — 1- or 8-Bit Resolution
  - — Allows Independent Transmit and Receive Routing, Frame Syncs, and Clocking
  - — Allows Dynamic Changes
  - — Can be Internally Connected to Four Serial Channels
- General-Purpose Timers
  - — Four 16-Bit Timers or Two 32-Bit Timers
  - — Gate Mode Can Enable/Disable Counting
  - — Interrupt can be Masked on Reference Match and Event Capture
- Interrupts
  - — Seven External Interrupt Request (IRQ) Lines
  - — One Nonmaskable Interrupt
  - — Twelve Port Pins with Interrupt Capability
  - — Ten Internal Interrupt Sources
  - — Programmable Highest Priority Request
- Memory Controller (Eight Banks)
  - — Can be Programmed to Support Almost any Memory Interface
  - — Each Bank Can be a Chip-Select or $\overline{\text{RAS}}$ to Support a DRAM Bank
  - — A Maximum of 30 Wait States per Memory Bank Can be Programmed
  - — Glueless Interface to DRAM Single In-Line Memory Modules, Static RAM, Electrically Programmable Read-Only Memory, Flash EPROM, or Synchronous DRAM
  - — Four $\overline{\text{CAS}}$ Lines, Four $\overline{\text{WE}}$ Lines, and One $\overline{\text{OE}}$ Line
  - — Boot Chip-Select Available at Reset (Options for 8-, 16-, or 32-Bit Memory)
  - — Variable Block Sizes—32K to 256M
  - — Selectable Write Protection
  - — On-Chip Bus Arbitration Supports External Bus Master
  - — Special Features for Burst Mode Support
- System Integration Unit
  - — Hardware Bus Monitor
  - — Spurious Interrupt Monitor
  - — Software Watchdog Timer
  - — Periodic Interrupt Timer
  - — Low-Power Stop Mode
  - — Clock Synthesizer
  - — PowerPC Decrementer and Timebase
  - — Real-Time Clock
  - — Reset Controller
  - — IEEE 1149.1 Test Access Port (JTAG)

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- Video/LCD Controller
  - — Video Controller
    - – Supports Digital NTSC/PAL Video Encoders and Digital TFT
    - – Sequential RGB, 4:4:4, and 4:2:2 YC_rC_b (CCIR 601) Digital Component Video Formats
    - – CCIR-656 Compatible 8-Bit Interface Port
    - – Horizontal Sync, Vertical Sync, Field and Blanking Timing
    - – Generation with Half-Clock Resolution and Programmable Polarity
    - – Supports Interlace/Noninterlace Scanning Methods
    - – Programmable Display Active Area
    - – Programmable Background Color for Inactive Area
    - – Glueless Interface for Most Digital Video Encoders
    - – Hardware Horizontal Scrolling
    - – Uses Burst Read DMA Cycles for Maximum Bus Performance
    - – Panel Voltage Control Adjustments for Contrast Set with On-Chip Timers
    - – End-of-Frame Interrupt Generation
  - — LCD Controller
    - – Supports Digital TFT and Passive LCD Panels
    - – Horizontal Sync, Vertical Sync, Field and Blanking Timing
    - – Generation with Half-Clock Resolution and Programmable Polarity
    - – 1-, 2-, or 4-Bit Per Pixel Grayscale Mode Using Advanced Frame Rate Control Algorithm
    - – Four or Eight Bits Per Pixel Color Mode
    - – 4-, 8-, 9-, or 12-Bit Parallel Output to LCD Displays
    - – Programmable Display Active Area
    - – Non-Split or Vertically Split Screen Support
    - – Uses Burst Read DMA Cycles for Maximum Bus Performance
    - – End-of-Frame Interrupt Generation
    - – Data for Splits—2+2 or 4+4 Parallel Bits (x+x Refers to x Bits Each for Lower and Upper Screens in Parallel)
    - – Built-In Color RAM with 256 12-Bit Entries
    - – Programmable Wait Time Between Lines and Frames
    - – Panel Voltage Control Adjustments for Contrast Set with On-Chip Timers
    - – Programmable Polarity for All LCD Interface Signals
- Single-Socket PCMCIA-ATA Interface
  - — Master Interface, Release 2.1 Compliant
  - — Single PCMCIA Socket
  - — Eight Memory or I/O Windows Available
  - — Eight General-Purpose I/O Pins and Two General-Purpose Output-Only Pins are Available when the PCMCIA Controller is Not in Operation

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- Low-Power Support Modes
  - — Normal High–All Units are Fully Powered at High Clock Frequency
  - — Normal Low–All Units are Fully Powered at Low Clock Frequency
  - — Doze–Core Functional Units are Disabled, except Timebase, Decrementer, PLL, Memory Controller, Real-Time Clock, LCD, and Communication Processor Module.
  - — Sleep–All Units are Disabled, except Real-Time Clock, Periodic Interrupt Timer, Timebase, and Decrementer. PLL is Active for Fast Wake-Up.
  - — Deep Sleep–All Units are Disabled including PLL, but not the Real-Time Clock and Periodic Interrupt Timer, Timebase, and Decrementer.
  - — Power-Down—All Units are Disabled Including PLL, but not the Real-Time Clock and Periodic Interrupt Timer, Timebase, and Decrementer. Saves More Power than Other Modes. The State of Certain Registers may be Preserved.
  - — Can be Dynamically Shifted Between High-Frequency and Low-Frequency Operation
- Development Capabilities and Interface
  - — Program Flow Tracking
    - – Instruction Show Cycle
    - – Data Show Cycle
    - – Branching
    - – Exception Traps
  - — Watchpoints and Breakpoints
    - – Four Hardware Breakpoints
    - – Five Watchpoint Sources
  - — Simple Hardware Interface
    - – High-Speed Data Transfer
    - – Internal Status Pins
    - – Freeze Indication
  - — Rich Control Register Set
- 3.3V Operation with 5V TTL Compatibility for the General-Purpose I/O Port Pins and 3.3V for All Others
- 256-Pin Plastic Ball Grid Array (BGA) Packaging

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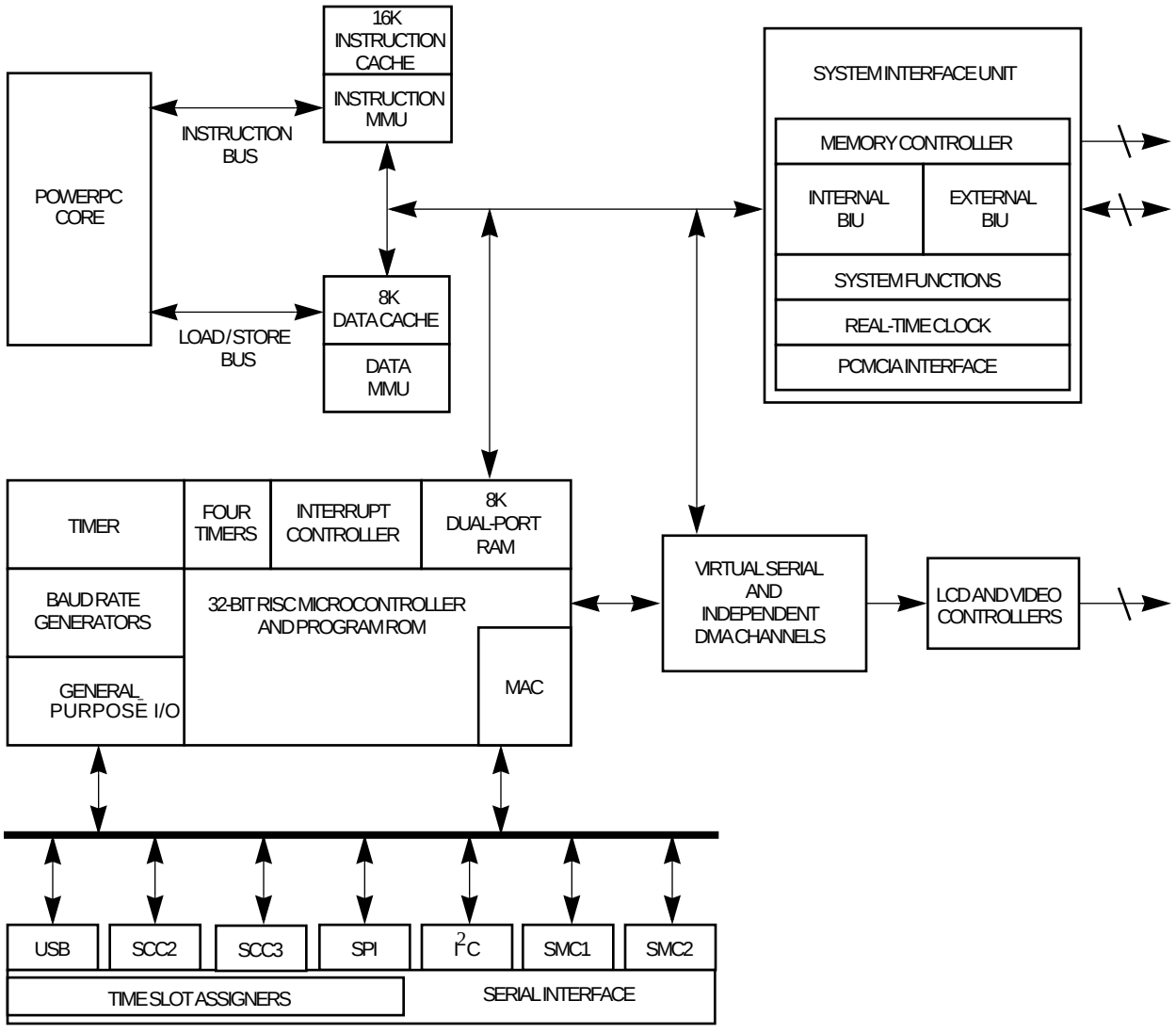
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Architecture

The MPC823e microprocessor uses a dual-processor architecture design approach with large data and instruction caches to provide high-performance using a general-purpose RISC integer processor and a special-purpose 32-bit scalar RISC communication processor module. The peripherals are uniquely designed for communication requirements and can provide embedded signal processing functions for communication and user interface enhancements and the I/O support needed for high-speed digital communication.

The MPC823e is comprised of four main modules that interface with the 32-bit internal bus:

- The embedded PowerPC core
- The system interface unit
- The communication processor module
- LCD controller



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Embedded PowerPC Core

The PowerPC core complies with standard PowerPC architecture. It has a fully static design that consists of an integer block, hardware multiplier/divider block and a load/store block. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. Its interface to the internal and external buses is 32 bits. The core uses a two-instruction load/store queue, four-instruction prefetch queue, and a six-instruction history buffer. It performs branch folding and branch prediction with conditional prefetch, but without conditional execution. With single bus cycles, the core can operate on 32-bit external operands and with critical-word-first in multiple bus cycles. The PowerPC integer block supports 32 x 32-bit fixed-point general-purpose registers and can execute one integer instruction per clock cycle.

The PowerPC core is integrated with the memory management units, an instruction cache, and a data cache. The memory management units provide 32-entry, fully associative instruction and data TLBs, with multiple page sizes of 4K (1K protection), 16K, 512K, and 8M. They support 16 virtual address spaces and 16 protection groups. Special registers are available to support software tablewalk and update.

The instruction cache is 16K, four-way, set-associative with physical addressing. It allows single-cycle accesses on hit with no added latency for miss. It is four words per line and supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. The data cache is 8K, two-way, set-associative with physical addressing. It allows single-cycle accesses on hit with one added clock latency for miss. It has four words per line and supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical data and can be programmed to support copyback or writethrough mode via the memory management unit. The cache-inhibit mode can be programmed per MMU page. The PowerPC core, with its instruction and data caches, can deliver approximately 99MIPS at 75MHz (using Dhrystone 2.1) or 172K Dhrystones, based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

Communication Processor Module

The communication processor module contains features that allow the MPC823 microprocessor to excel in imaging, personal communication, and low-power applications. These features are divided into three categories:

- DSP processing
- Communication processing
- Twelve serial DMA channels and two independent DMA channels

The MPC823e embedded DSP function allows the communication processor module to execute imaging algorithms in parallel with the PowerPC core to achieve maximum performance with very little power. The DSP can execute one 16x16 MAC on every clock cycle. It has preprogrammed filtering functions like FIR, MOD, DEMOD, IIR, and downloadable imaging functions for JPEG image compression and decompression.

The robust communication features of the MPC823e are provided by the communication processor module. These features include a RISC microcontroller with multiply accumulate hardware, two serial communication controllers, two serial management controllers, one dedicated serial channel for the Universal Serial Bus, one inter-integrated circuit port, one serial peripheral interface, an 8K dual-port RAM, interrupt controller, two time-slot assigners, and four independent baud rate generators.

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Twelve serial DMA channels support the SCCs, SMCs, USB channel, SPI, and I^2C controllers. The independent DMAs give you two channels for general-purpose DMA usage. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC microcontroller is the only block that can access the IDMA registers directly. The CPU can only access them indirectly via a buffer descriptor.

System Interface Unit

The system interface unit supports traditional 68K big-endian memory systems, traditional x86 little-endian memory systems, and PowerPC little-endian memory systems. It also provides power management functions, reset control, a PowerPC decrementer, timebase, and real-time clock. Although the PowerPC core is a 32-bit device internally, it can be configured to operate with an 8-, 16-, or 32-bit data bus. Regardless of the system bus size, dynamic bus sizing is supported, which allows 8-, 16-, and 32-bit peripherals and memory to coexist on a 32-bit system bus.

The memory controller supports as many as eight memory banks with glueless interfaces to DRAM, SRAM, EPROM, Flash EPROM, SDRAM, EDO and other peripherals with two-clock initial access to external SRAM and bursting support. It provides variable block sizes between 32K and 256M. The memory controller has 0 to 20 wait states for each bank of memory and can use address-type matching to qualify each memory bank access. It provides four byte-enable signals for varying width devices, one output-enable signal, and one boot chip-select that is available at reset.

The DRAM interface supports 8-, 16-, and 32-bit ports and uses a programmable state machine to support almost any memory interface. Memory banks can be defined in depths of 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, or 64M for all port sizes. In addition, the memory depth can be defined as 64K and 128K for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC823e supports a glueless interface to one bank of DRAM, while external buffers are required for additional memory banks. The refresh unit provides $\overline{CAS}$ before $\overline{RAS}$, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking for a maximum of seven refresh cycles.

Video/LCD Controller

The MPC823e has a dual-purpose video/LCD controller that shares common dual-port memory. However, only one of the controllers can be run at a time.

The video controller can be used to drive a digital NTSC/PAL encoder or a wide variety of digital LCD panels. The frame buffer is stored in system memory in the form of an orthogonal matrix—rows and columns. The 24-bit color data is organized as pixel components whether it is sequential RGB or YC_rC_b. Each pixel component is represented by a byte. The video controller uses a dedicated DMA channel to read the display data from the frame buffer and drive it to the video interface. It also generates the required timing signals, such as horizontal sync, vertical sync, field, and blanking.

The LCD controller provides extremely versatile LCD support for 8-bit color, monochrome or 4/16-level grayscale, color TFT (12 bits, 4x3 RGB), and passive color (xSTN) 4/8 bit data. The controller supports 4- or 8-bit single-scan, 2+2 bit dual-scan, or 4+4 bit dual-scan. It is programmable for frame rate, number of pixels per line, and number of lines per frame. The panel voltage is programmable through the duty cycle for contrast adjustments implemented in the communication processor module program. Display data is stored in memory space and is transferred into the controller using the DMA channel.

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PCMCIA-ATA Controller

The PCMCIA-ATA interface is a master controller that is compliant with Version 2.1 of the PCMCIA standard. The interface supports one independent PCMCIA socket with the required external transceivers or buffers. It provides eight memory or I/O windows that can be allocated to the socket. If the PCMCIA port is not being used as a card interface, it can provide eight general-purpose pins and two output-only pins with interrupt capability.

Power Management

The MPC823e microprocessor supports a wide range of power management features, including normal high, normal low, doze, sleep, deep-sleep, and power-down modes. In normal high mode, the MPC823e is fully powered with all internal units operating at the full speed of the processor. Normal low mode is the same as normal high, except it operates at a much lower frequency. There is a doze mode determined by a clock divider that allows the operating system to reduce the operational frequency of the processor.

Doze mode disables core functional units except the timebase, decrementer, PLL, memory controller, real-time clock, LCD controller, and communication processor module. Sleep mode is a lower power mode that disables everything except the real-time clock, timebase, decrementer, and periodic interrupt timer, thus leaving the PLL active for quick wake-up. The deep-sleep mode then disables the PLL for lower power, but slower wake-up. Power-down mode disables all logic in the processor, except the minimum logic required to restart the device. It saves the most power, but requires the longest wake-up time.

System Debug Support

The MPC823e microprocessor contains an advanced debug interface that provides superior debug capabilities without any loss of speed. It supports six watchpoint pins that can be combined with eight internal comparators, four of which operate on the effective address of the address bus. The other four comparators are split—two comparators operate on the effective address on the data bus and two comparators operate on the data on the data bus. The MPC823 microprocessor can compare using the =, π, <, and > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

Applications

The MPC823e microprocessor is specifically designed to be a general-purpose, low-cost entry point to the Motorola embedded PowerPC Family for systems in which advanced GUIs, communications, and high-level real-time operating systems are used. The device excels in applications that require the performance of a single-issue PowerPC core with an ample amount of data and instruction cache. It provides all the basic features of glueless memory connections along with highly functional serial connectivity, a graphical LCD, and a video display controller. The MPC823e excels in low-power and portable applications because of its extensive power-down modes and low normal operation current.

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Order Information

The following table contains the package type and operating frequencies of the MPC823e.

Package Type	Frequency	Temperature	Order Number
256 lead PBGA 23x23 1.27mm pitch	66 MHz 75 MHz	0°C to 95°C* 0°C to 95°C*	XPC823EZT66B XPC823EZT75B
256 lead PBGA 23x23 1.27mm pitch	66 MHz	-40°C to 95°C**	XPC823CZT66B

* TA = 0° C to Tj = +95° C
** TA = -40° C to Tj = +95° C

The documents listed in the table below contain detailed information on the MPC823e and MPC823 microprocessors. All MPC823 documentation applies to the MPC823e with the exception of the data and instruction cache sections of the user's manual. You can obtain these documents from the Motorola Literature Distribution Center or from our website at www.mot.com/mpc823.

Document Title	Order Number	Contents
MPC823 User's Manual	MPC823UM/D	Detailed information for MPC823 design
MPC823 CD	CDMPC823/D	MPC823 User's Manual in PDF
MPC823 Pocket Reference Guide	MPC823RG/D	Quick reference to content of the MPC823 User's Manual
MPC823 Electrical Specifications	MPC823LE/D	Electrical specifications for the MPC823
MPC823 Literature Package	MPC823PAK/D	MPC823 User's Manual, Pocket Reference Guide, Electrical Specifications, and CD
MPC823e Reference Manual	MPC823ERM/D	Not yet available
MPC823e CD	CDMPC823E/D	Not yet available
MPC823e Pocket Reference Guide	MPC823ERG/D	Not yet available
MPC823e Electrical Specifications	MPC823ELE/D	Not yet available
MPC823e Literature Package	MPC823EPAK/D	Not yet available
PowerPC Microprocessor Family: The Programming Environments for 32-Bit Microprocessors	MPCFPE32B/AD	PowerPC instruction set
PowerPC Resource Guide	BR1724/D	Independent vendor listing of supporting software and development tools

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INTERNET: http://motorola.com/sps

Technical Information: Motorola Inc. SPS Customer Support Center 1-800-521-6274; electronic mail address: crc@wmkmail.sps.mot.com.

Document Comments: FAX (512) 895-2638, Attn: RISC Applications Engineering.

World Wide Web Addresses: www.motorola.com
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