MP9151

20V, 4A Synchronous Step-Down Coverter

The Future of Analog IC Technology

DESCRIPTION

The MP9151 is a synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 4A continuous output current over a wide input supply range with excellent load and line regulation. The MP9151 has synchronous mode operation for higher efficiency over output current load range.

Current mode operation provides fast transient response and eases loop stabilization. Full protection features include OCP and thermal shut down.

The MP9151 requires a minimum number of readily available standard external components and is available in a space saving 2mm x 3mm 14-pin QFN package.

FEATURES

- Wide 4.5V to 20V Operating Input Range
- 4A Output Current
- Low Rds(ON) Internal Power MOSFETs
- Programmable Switching Frequency from 300kHz to 1.6MHz
- EN ON/OFF Control
- Internal Power Save Mode
- Power Good Indicator
- External Soft Start
- OCP and Thermal Shutdown
- Available in 14-pin QFN2x3 Package

APPLICATIONS

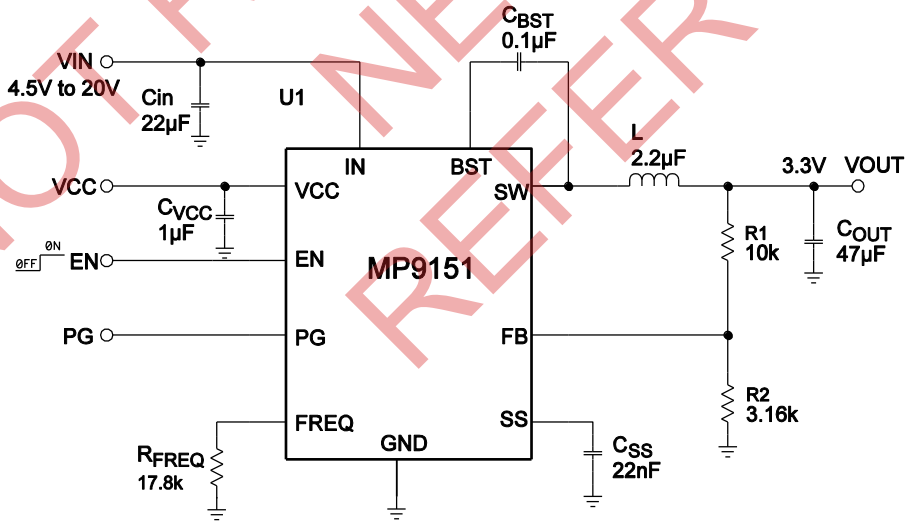
- DSL Modems
- Cable Modems
- Set Top Boxes

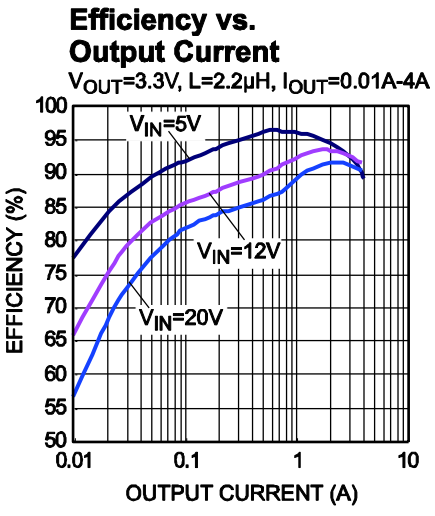
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TYPICAL APPLICATION





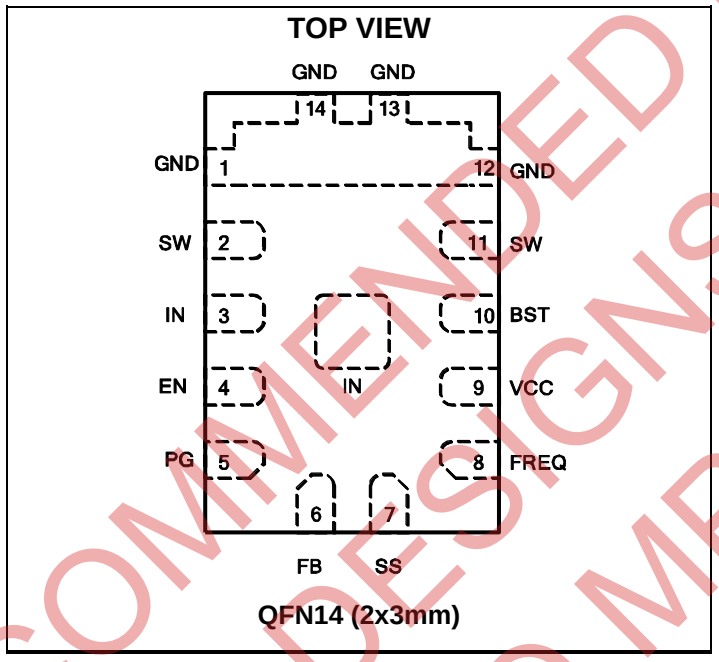
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP9151GD*	QFN14 (2x3mm)	AEM

* For Tape & Reel, add suffix –Z (eg. MP9151GD–Z); .

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 22V
V_{SW} ..... -0.3V to 23V
V_{BST} ..... V_{SW} + 6V
All Other Pins..... -0.3V to 6.5 V (2)
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Continuous Power Dissipation (T_A = +25°C) (3)
2x3 QFN14 ..... 1.8W

Recommended Operating Conditions (4)

Supply Voltage V_{IN}..... 4.5V to 20V
Output Voltage V_{OUT}..... 0.8V to V_{IN} x 95%
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN14 (2x3mm) ..... 70 ..... 15 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Please refer to Page 10, Enable Control section, For absolute maximum rating of EN pin.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		10	15	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V		0.7		mA
HS Switch On Resistance	HS_{RDS-ON}			60		mΩ
LS Switch On Resistance	LS_{RDS-ON}			30		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
Current Limit	I_{LIMIT}	Duty=40%	6	7		A
Oscillator Frequency	F_{SW}	Rset=17.8kΩ	560	800	1040	kHz
Fold-back Frequency	F_{FB}	V_{FB} = 100mV		0.25		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB} = 700mV, f_{SW}=800kHz	90	95		%
Minimum On Time (6)	T_{ON_MIN}			40		ns
Feedback Voltage	V_{FB}		779	795	811	mV
Feedback Current	I_{FB}	V_{FB} = 800mV		10	50	nA
EN Input Low Voltage	VIL_{EN}		0.9	1.12	1.3	V
EN Input High Voltage	VIH_{EN}		1.3	1.55	1.9	V
EN pin pull-up Current	I_{EN}			2		μA
Power Good Rising Threshold	PG_H	FB respect to the regulation		90		%
Power Good Falling Threshold	PG_L			80		%
Power Good Sink Current Capability	VPG_L	Sink 1mA			0.1	V
V_{IN} Under Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.85	4.1	4.35	V
V_{IN} Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			850		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		Icc=5mA		1		%
Thermal Shutdown (6)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (6)	T_{SD-HYS}			30		°C
Soft Start Current	I_{SS}			8		μA

Note:

6) Guaranteed by design.

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PIN FUNCTIONS

QFN 2X3mm Pin #	Name	Description
1, 12, 13, 14	GND	Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors. Connect exposed pad to GND plane for proper thermal performance.
2, 11	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
3, Center Pad	IN	Supply Voltage. The MP9151 operates from a +4.5V to +20V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
4	EN	Enable. EN=1 to enable the MP9151. The EN pin sources 2.3μA current. Place a capacitor from EN to GND for delayed start-up.
5	PG	Power Good Indicator. An external pull-up resistor is needed across PG pin and VCC.
6	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 100mV.
7	SS	Soft Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
8	FREQ	Switching Frequency Program Input. Connect a resistor from this pin to ground to set the switching frequency.
9	VCC	Bias Supply. Decouple with 1μF capacitor.
10	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.

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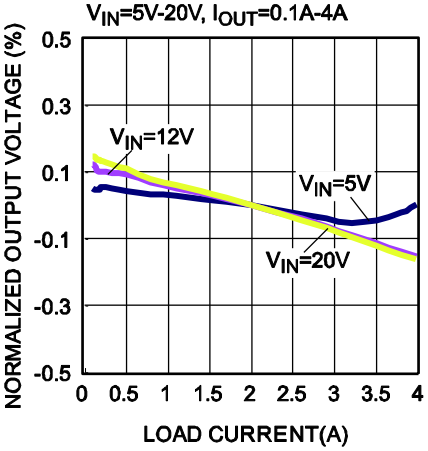
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TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, f_{SW}=800kHz, T_A = +25°C, unless otherwise noted.

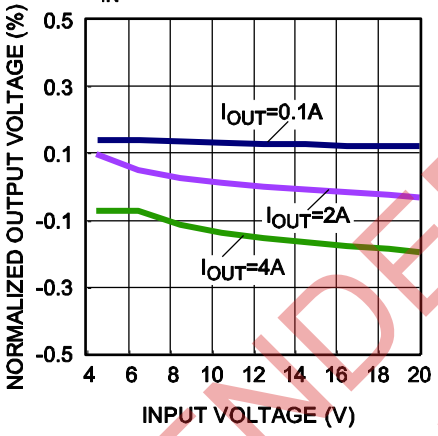
Load Regulation

V_{IN}=5V-20V, I_{OUT}=0.1A-4A

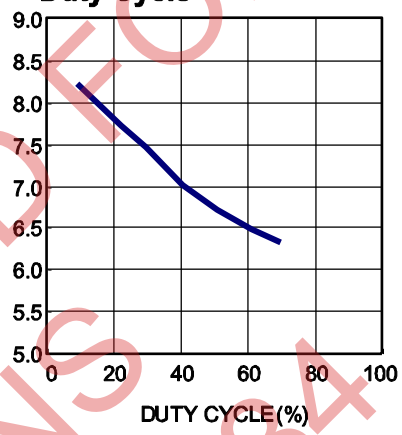


Line Regulation

V_{IN}=4.5V-20V

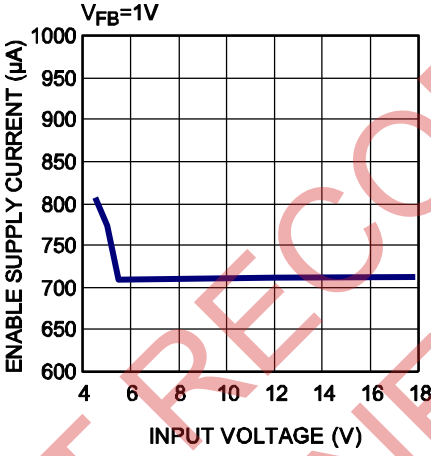


Current Limit vs. Duty Cycle



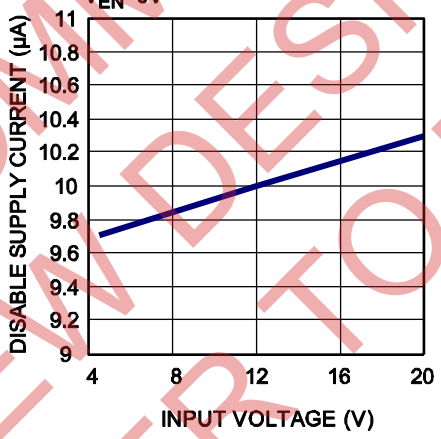
Enabled Supply Current vs. Input Voltage

V_{FB}=1V

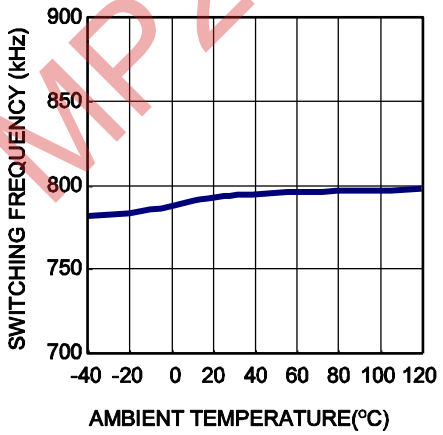


Disabled Supply Current vs. Input Voltage

V_{EN}=0V



Switching Frequency vs. Ambient Temperature



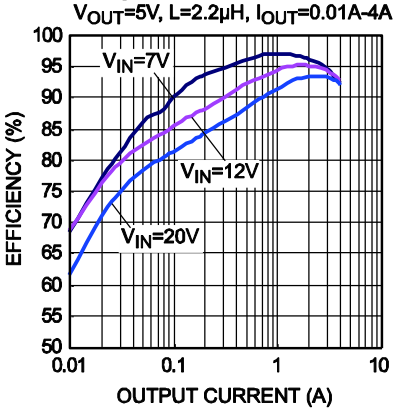
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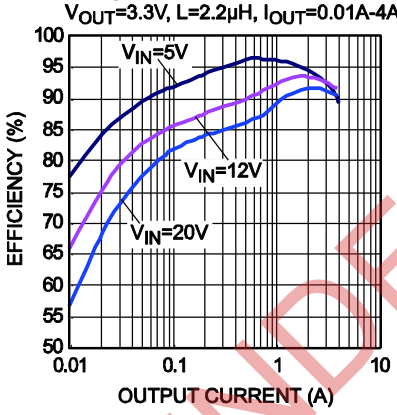
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, f_{SW}=800kHz, T_A = +25ºC, unless otherwise noted.

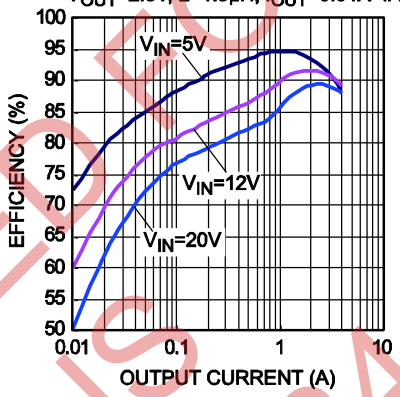
Efficiency vs. Output Current
V_{OUT}=5V, L=2.2µH, I_{OUT}=0.01A-4A



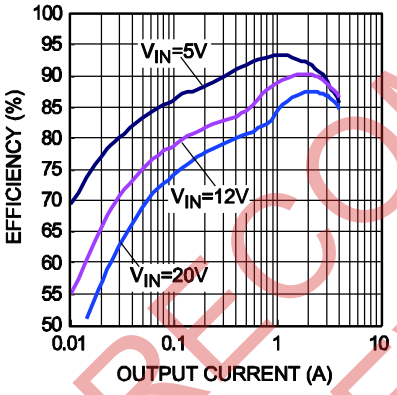
Efficiency vs. Output Current
V_{OUT}=3.3V, L=2.2µH, I_{OUT}=0.01A-4A



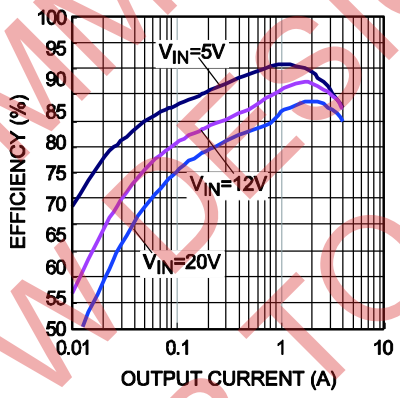
Efficiency vs. Output Current
V_{OUT}=2.5V, L=1.5µH, I_{OUT}=0.01A-4A



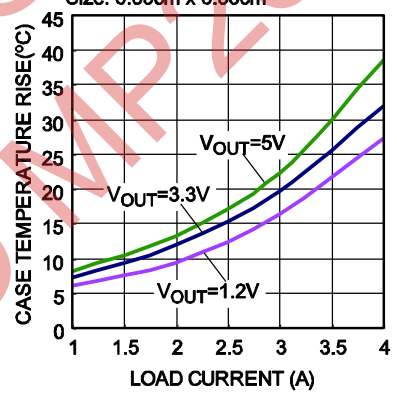
Efficiency vs. Output Current
V_{OUT}=1.8V, L=1.5µH, I_{OUT}=0.01A-4A



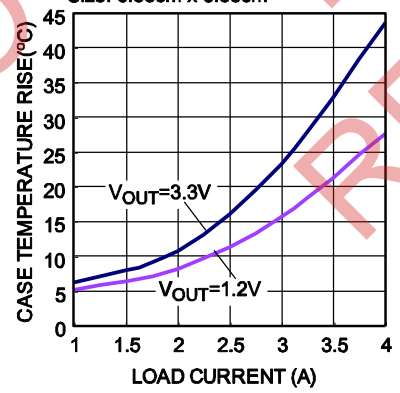
Efficiency vs. Output Current
V_{OUT}=1.2V, L=1µH, I_{OUT}=0.01A-4A



Case Temperature Rise vs. Output Current
V_{IN}=12V, I_{OUT}=1A-4A, 4 Layers PCB, Size: 6.35cm x 6.35cm



Case Temperature Rise vs. Output Current
V_{IN}=5V, I_{OUT}=1A-4A, 4 Layers PCB, Size: 6.35cm x 6.35cm



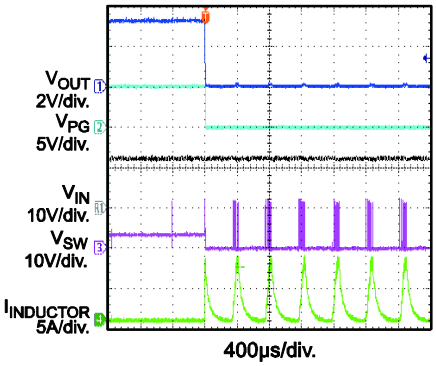
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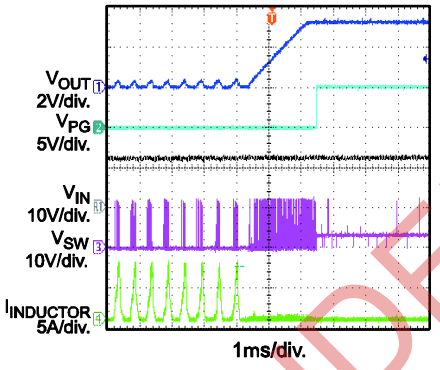
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, f_{SW}=800kHz, T_A = +25ºC, unless otherwise noted.

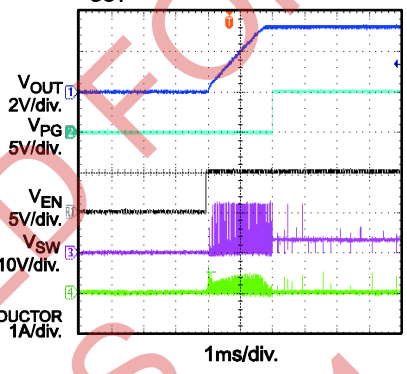
Short Entry
I_{OUT} = 0A



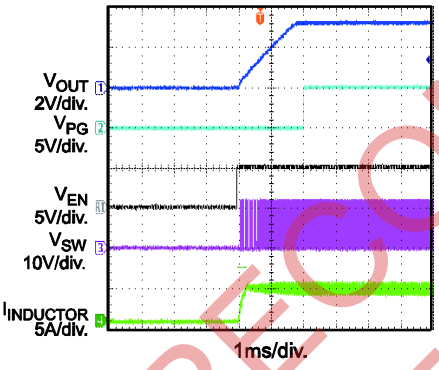
Short Recovery
I_{OUT} = 0A



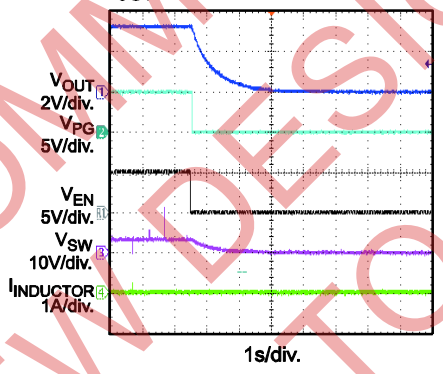
Startup Through Enable
I_{OUT} = 0A



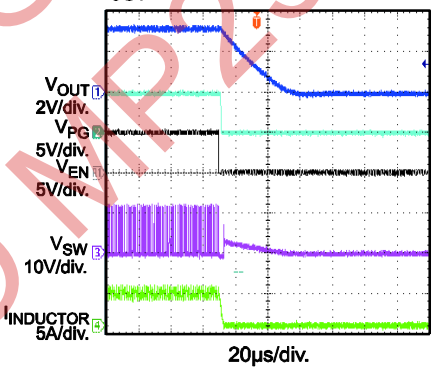
Startup Through Enable
I_{OUT} = 4A



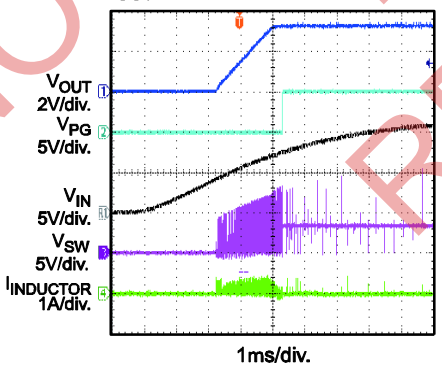
Shutdown Through Enable
I_{OUT} = 0A



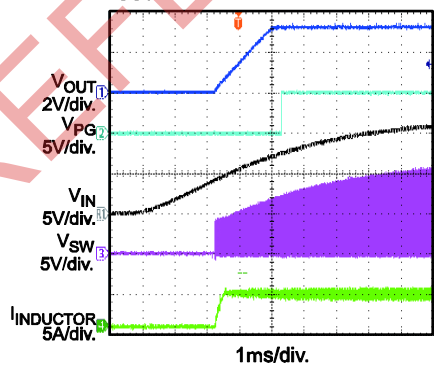
Shutdown Through Enable
I_{OUT} = 4A



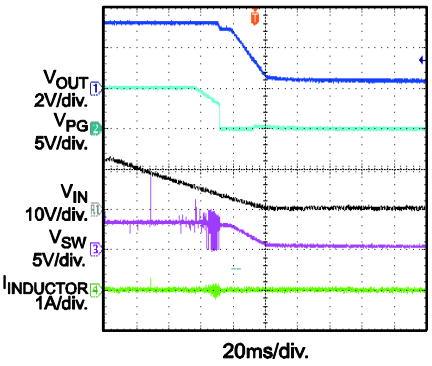
Startup Through Input Voltage
I_{OUT} = 0A



Startup Through Input Voltage
I_{OUT} = 4A



Shutdown Through Input Voltage
I_{OUT} = 0A



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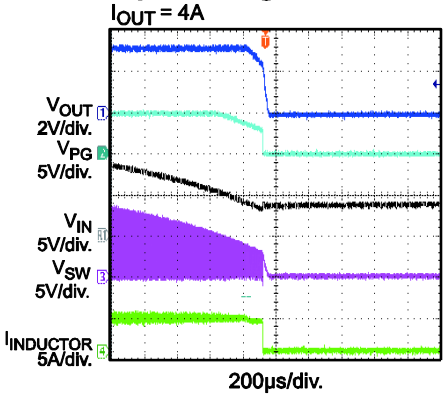
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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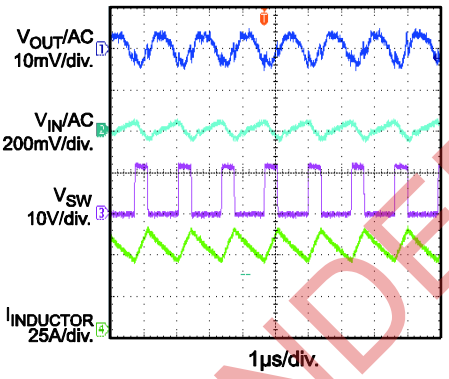
Shutdown Through Input Voltage

I_{OUT} = 4A



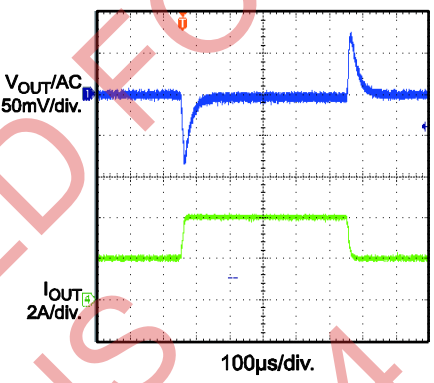
Input / Output Ripple

I_{OUT} = 4A



Load Transient Reponse

I_{OUT} = 2A-4A



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FUNCTION BLOCK DIAGRAM

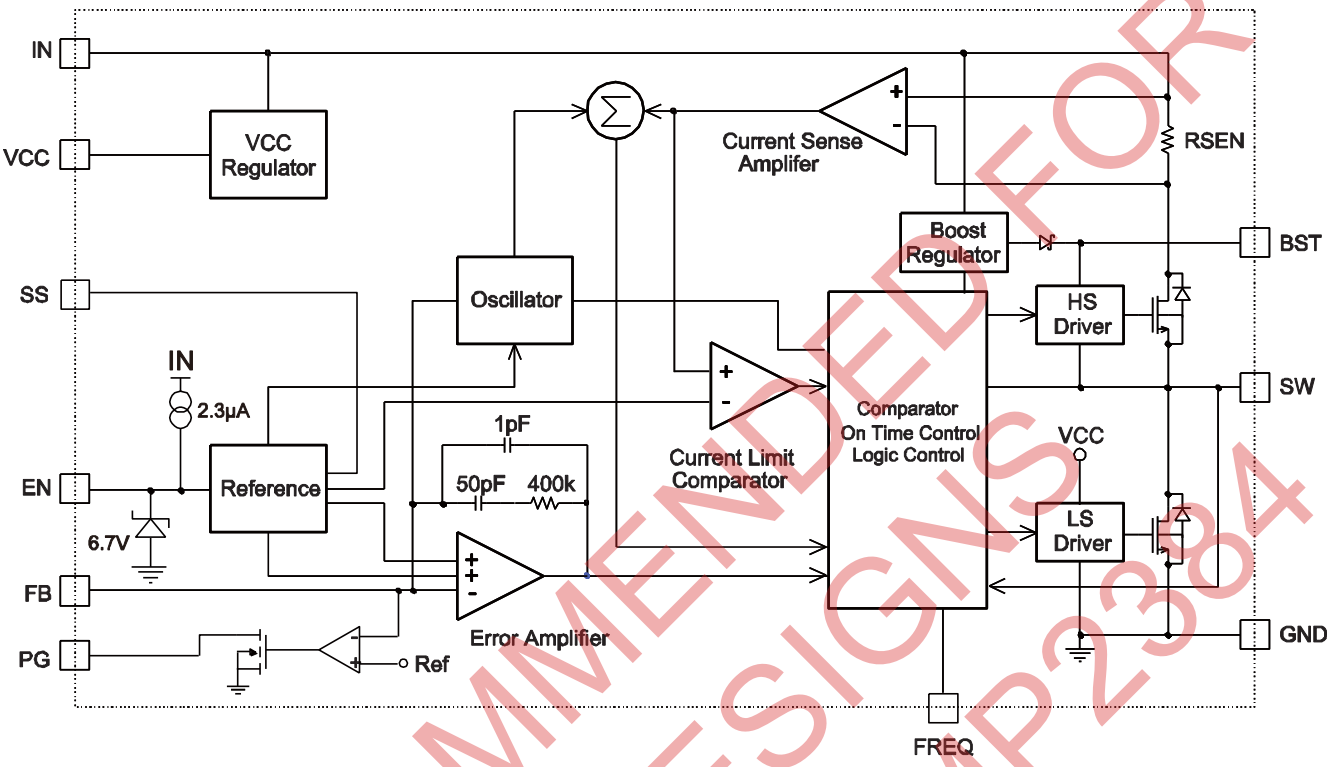


Figure 1: Block Function Diagram

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OPERATION

The MP9151 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve more than 4A continuous output current over a wide input supply range with excellent load and line regulation.

The MP9151 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 95% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.795V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, a 1uF ceramic capacitor for decoupling purpose is required.

Enable Control

The MP9151 has a dedicated enable control pin (EN): pulling it high enables the IC, pulling it low disables it. Float EN for automatic start up. EN must be pulled low to disable the part.

The EN pin is clamped internally using a 6.7V series-Zener-diode as shown in Figure 2 Connect the EN input pin through a pullup resistor to any voltage connected to the VIN pin such that the pullup resistor limits the EN input current to less than 100μA.

For example, connecting 12V to VIN, $R_{PULLUP} \geq (12V - 6.7V)/100\mu A = 53k\Omega$.

Connecting the EN pin is directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to below 6V to prevent damage to the Zener diode.

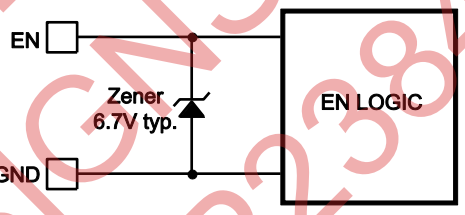


Figure 2: Zener Diode between EN and GND

The EN pin also features an internal 2.3μA current source. Connect a capacitor to the EN pin for delayed startup. When VIN exceeds the input UVLO, an internal 2.3μA current source charges the external capacitor. The external capacitor connects to the non-inverting input of a comparator. The part is enabled once the capacitor voltage exceeds the 1.5V internal reference voltage.

Power Good Indicator

The MP9151 has an open drain pin for power good indicator. When FB pin is higher than 90% of regulation voltage, 0.795V, PG pin is pulled up to VCC by the external resistor. If FB pin voltage drop down to 80% of the regulation voltage, PG pin is pulled down to ground by an internal MOS FET.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP9151 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.1V while its falling threshold is a consistent 3.25V.

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External Soft-Start

The soft start time can be adjusted by connecting a capacitor from this pin to ground. When the soft-start period starts, an internal 8μA current source begins charging the external capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.795V. At this point the reference voltage takes over at the no inverting error amplifier input. The soft-start time can be calculated as follows:

$$t_{SS}(ms) = \frac{0.795V \times C_{SS}(nF)}{8\mu A}$$

If the output of the MP9151 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Save Mode for Light Load Condition

The MP9151 has AAM (Advanced Asynchronous Modulation) power save mode for light load. The AAM voltage is set at 0.4V internally. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} is higher than V_{AAM}.

Under the light load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}, during this time, the internal clock is blocked, thus the MP9151 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

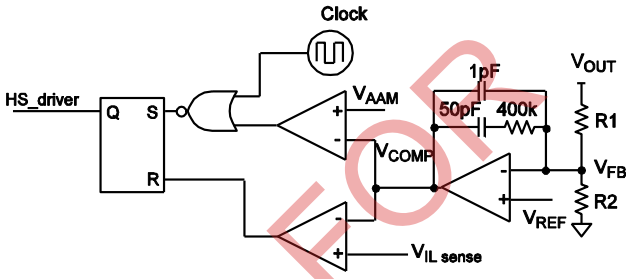


Figure 3: **Simplified AAM Control Logic**

When the load current is light, the inductor peak current set internally is about 630mA and the load current threshold exit AAM is about 0.3A for V_{IN}=12V, V_{OUT}=3.3V, and L=2.2μH.

Over-Current-Protection

The MP9151 has hiccup over current limit when the inductor current peak value exceeds the set current limit threshold.

When output voltage drops below 70% of the reference, and inductor current exceeds the current limit at the meantime, MP9151 will be hiccup. This is especially useful to ensure system safety under fault condition.

The hiccup function is disabled during soft-start duration.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 120°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1 and C2 (Figure 4). If (V_{IN}-V_{SW}) is more than 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4.

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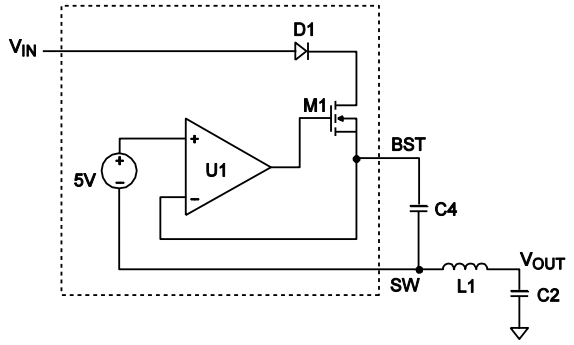


Figure 4: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 10kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.795V} - 1}$$

The T-type network is highly recommended when V_{OUT} is low, as Figure 5 shows.

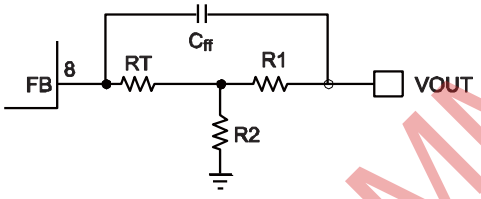


Figure 5: T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	C_{ff} (pF)	L (µH)
1	2.61 (1%)	10 (1%)	47	33	1
1.2	5.1 (1%)	10 (1%)	39	33	1
1.8	10 (1%)	7.87 (1%)	5.1	56	1.5
2.5	10 (1%)	4.64 (1%)	5.1	56	1.5
3.3	10 (1%)	3.16 (1%)	0	56	2.2
5	10 (1%)	1.91 (1%)	0	56	2.2

Selecting the Inductor

A 1µH to 22µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Setting the Switching Frequency

An external resistor, R_{FREQ}, from the FREQ pin to GND sets the MP9151 oscillating frequency from 300kHz to 1.6MHz. The value of R_{FREQ} can be calculated from:

$$R_{FREQ}(k\Omega) = \frac{28000}{f_s(kHz)^{1.1}}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

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The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP9151 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 6.

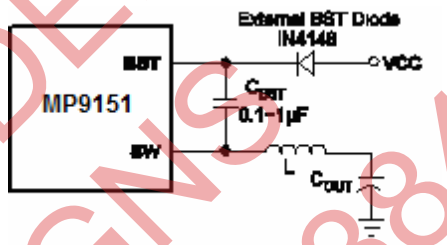


Figure 6: Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

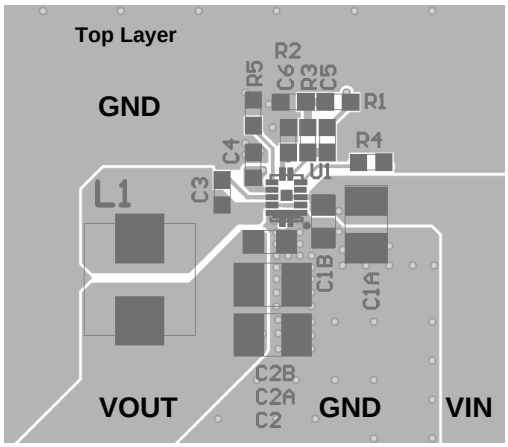
PC Board Layout

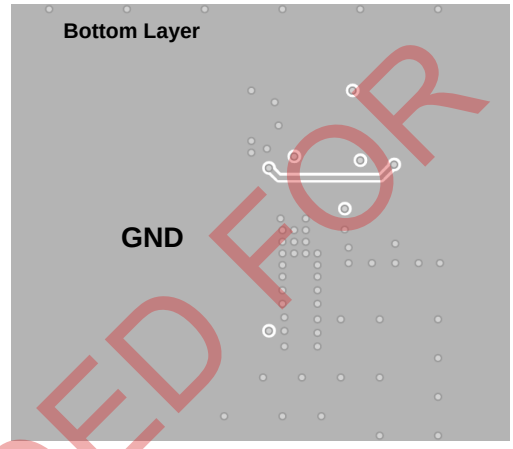
This PCB board layout is referring to the schematic in Figure 7.

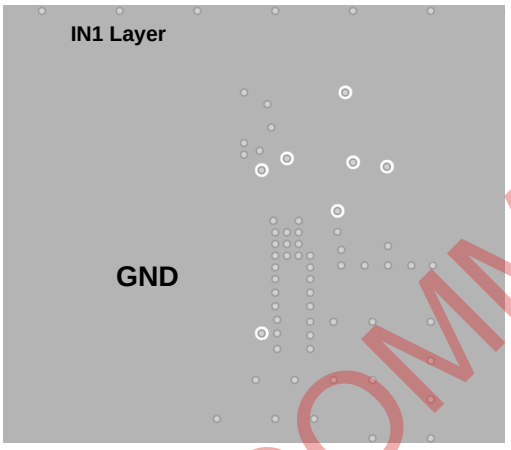
Place the high-current paths (GND, IN and SW) very close to the device with short, direct and wide traces. The input decoupling capacitor needs to be placed as close as possible to the IN and GND pins. The VCC decoupling capacitor needs to be placed as close as possible to the VCC pin and multiple VIAs should be used on both the ground side of the VCC decoupling capacitor and the GND pins to connect to the inner and bottom ground plane. Place the external feedback resistors next to the FB pin. Keep the switching node SW short and away from the feedback network.

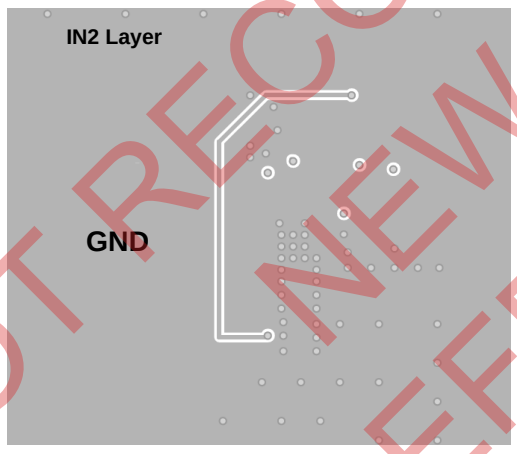
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Design Example

Below is a design example following the application guidelines for the specifications:

Table 1: Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	4A

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

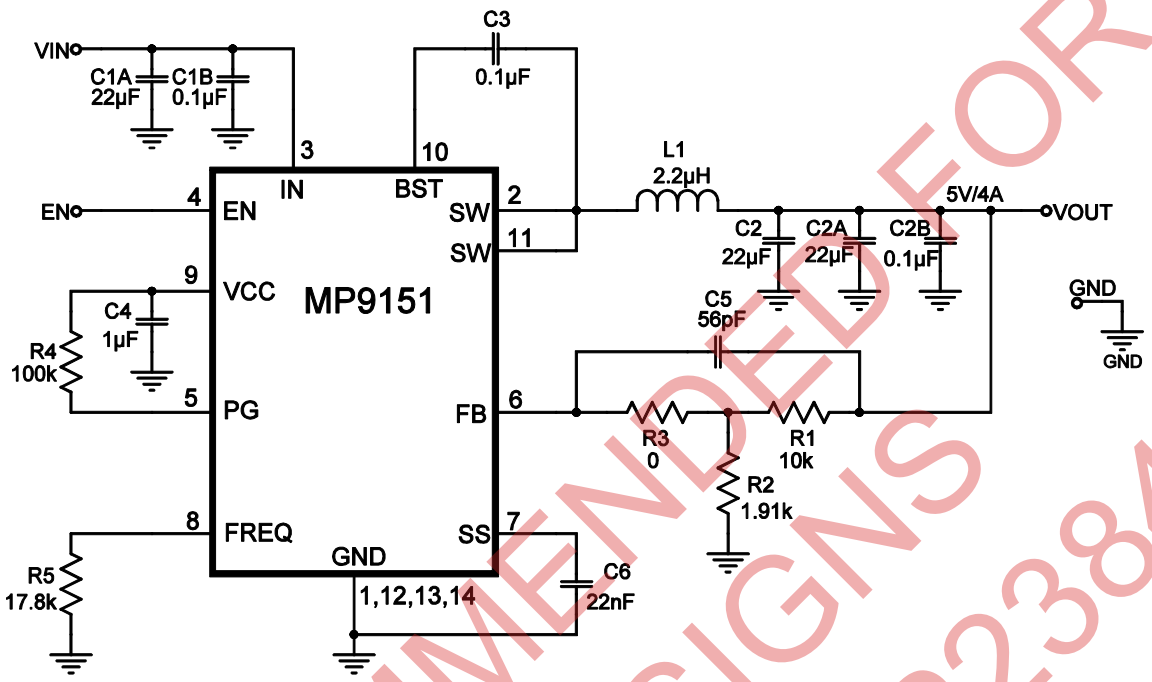


Figure 7: 800kHz, 12V$_{IN}$, 5V/4A Output

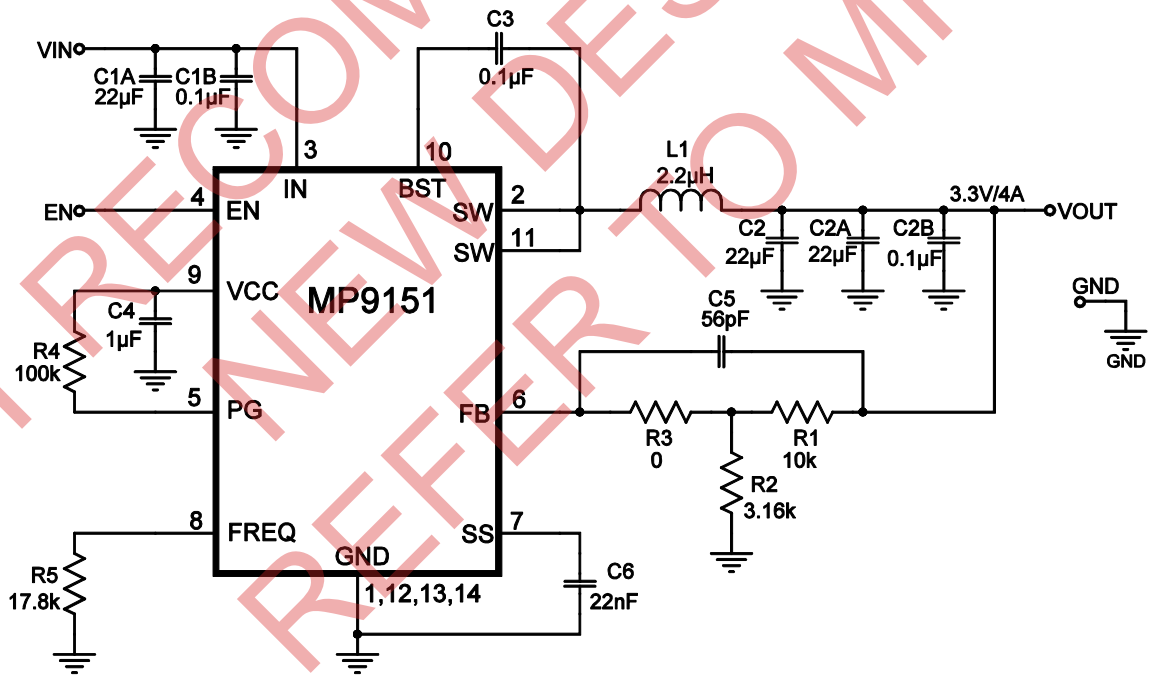


Figure 8: 800kHz, 12V$_{IN}$, 3.3V/4A Output

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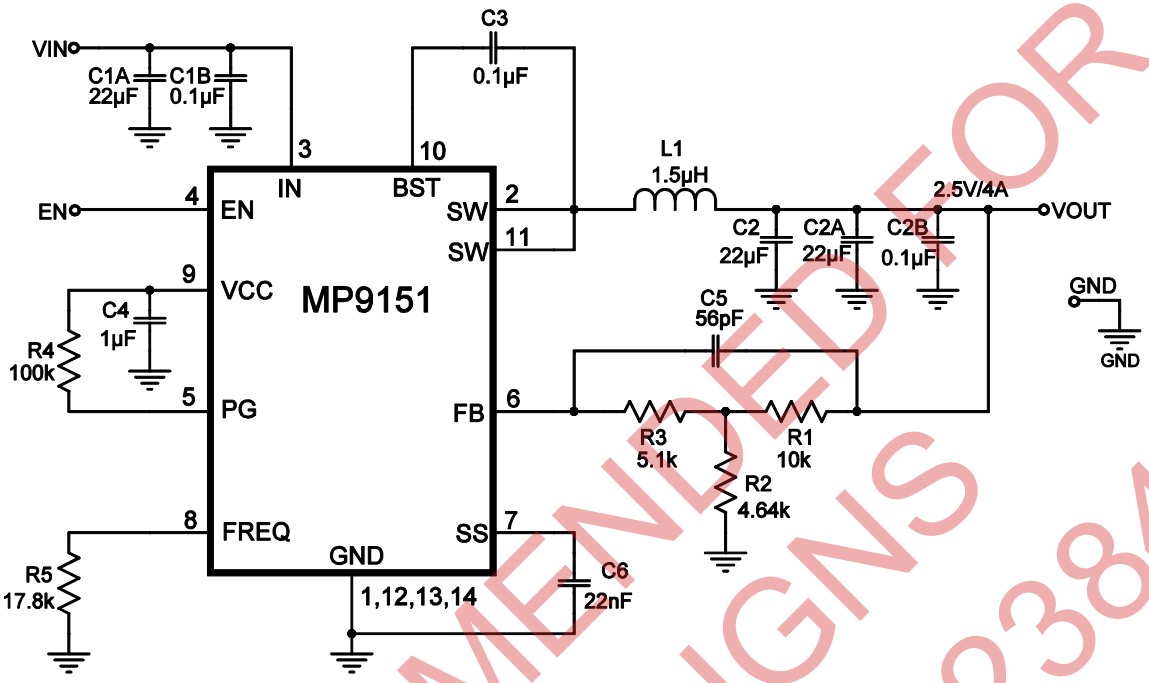


Figure 9: 800kHz, 12V_{IN}, 2.5V/4A Output

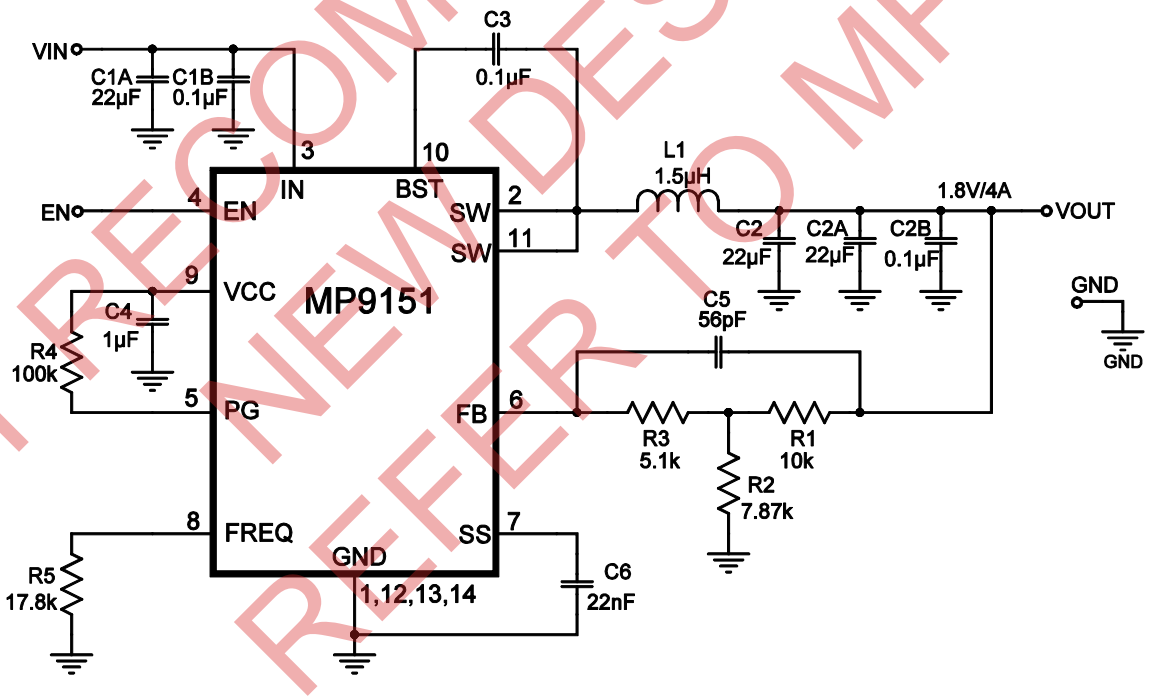


Figure 10: 800kHz, 12V_{IN}, 1.8V/4A Output

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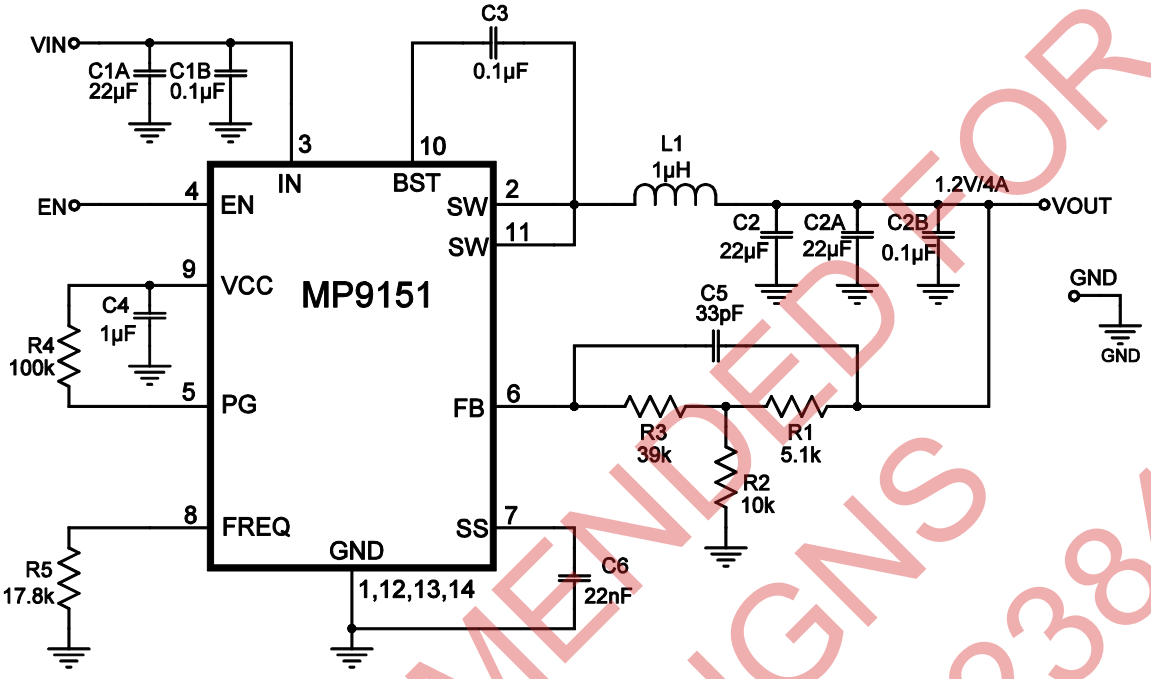


Figure 11: 800kHz, 12V_{IN}, 1.2V/4A Output

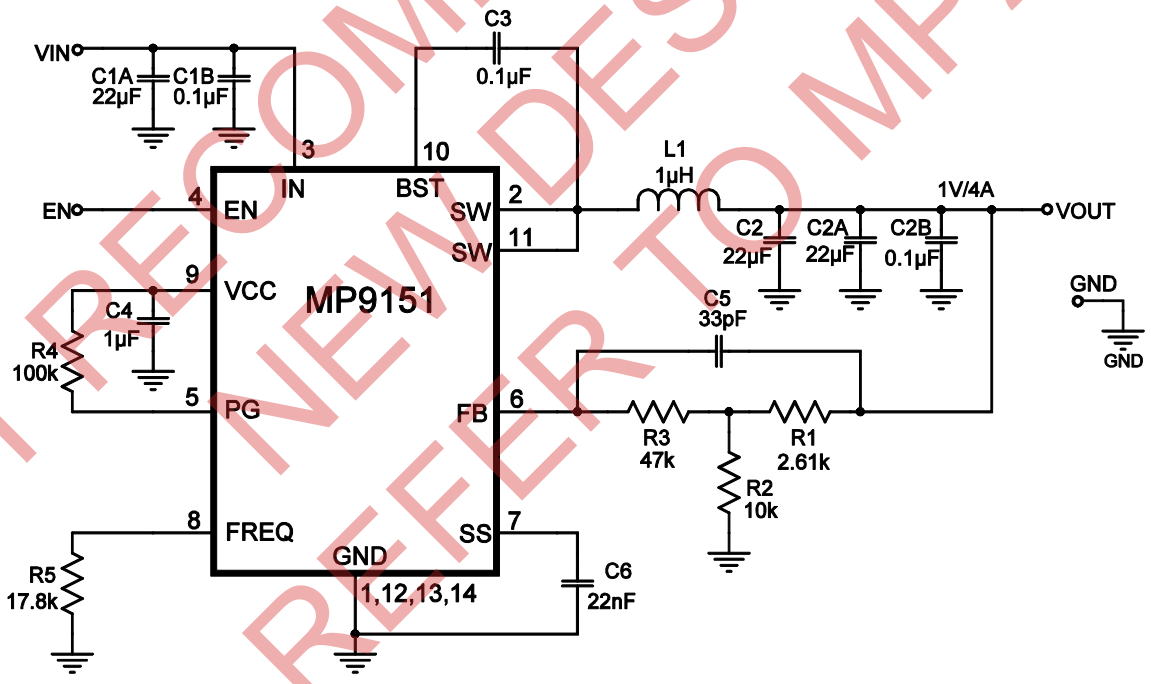
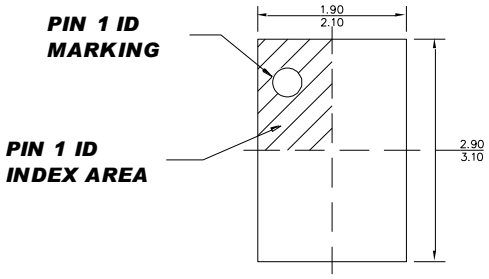


Figure 12: 800kHz, 12V_{IN}, 1V/4A Output

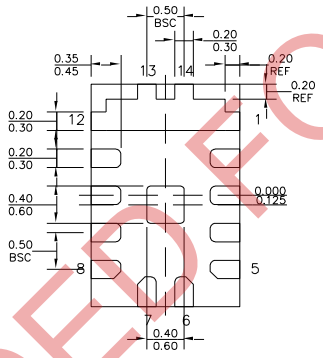
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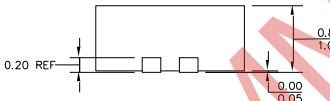
PACKAGE INFORMATION



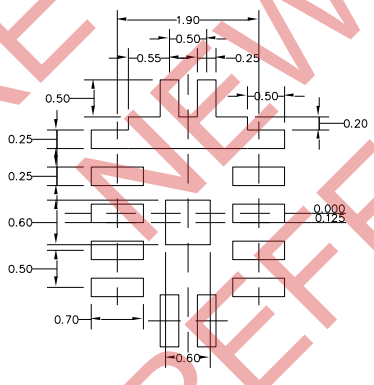
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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