MP8715

100% Duty Cycle Synchronous 4A, 21V, 500kHz Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP8715 is a 500 kHz fixed-frequency PWM synchronous step-down regulator. MP8715 operates from a 4.5V to 21V input and generates an output voltage form 0.8V to V_{IN} with 100% duty cycle operation.

The MP8715 integrates a 120mΩ high-side switch and a 50mΩ synchronous rectifier for high efficiency without an external Schottky diode. It offers a very compact solution to achieve 4A continuous output current over a wide input supply range with excellent load and line regulation.

External soft start and power good indication meet flexible design requirement.

The MP8715 is available in a space saving 8-pin SOIC package with an exposed pad and 3mmx4mm 14-pin QFN package.

FEATURES

- 4A Output Current
- Wide 4.5V to 21V Input Operation Range
- 100% Duty Cycle Support
- 120mΩ/50mΩ Internal Power MOSFET
- All Ceramic Capacitor Design
- Up to 95% Efficiency
- 500kHz Fixed Switching Frequency
- Adjustable Output from 0.8V to Vin
- External Soft-Start
- Frequency Synchronization Input
- Power OK Indicator
- Internal Compensation
- Over Current Hiccup and Thermal Protection
- Available in 8-pin SOIC Package with an Exposed Pad and 14-pin QFN3x4 package

APPLICATIONS

- Cable eMTAs
- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Printers and LCD TVs
- Digital Set Top Boxes
- Network and Telecom Equipment
- Point of Load Regulators

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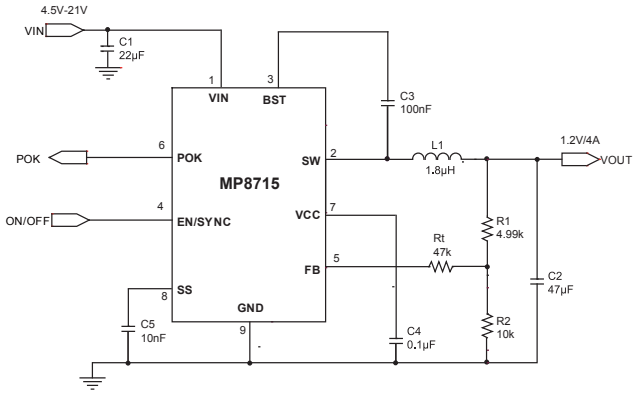
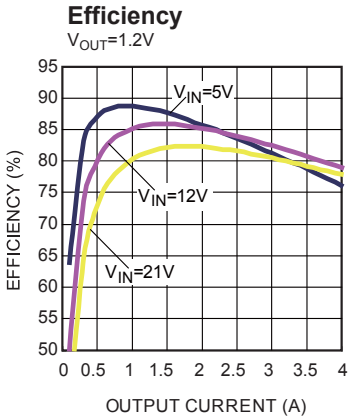
TYPICAL APPLICATION



SOIC8E Package



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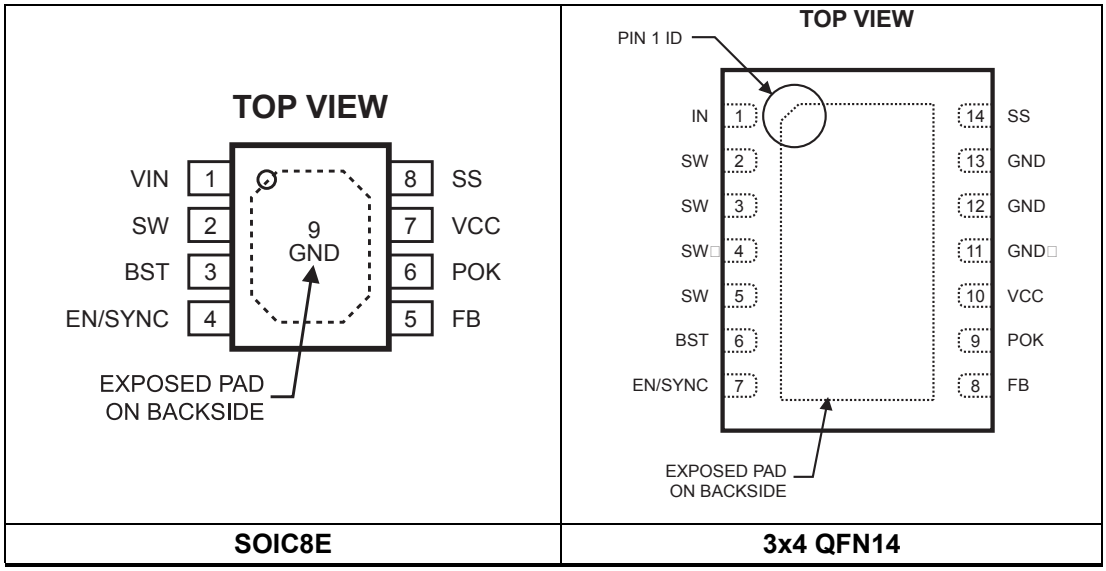
ORDERING INFORMATION

Part Number	Package	Top Marking
MP8715DN*	SOIC8E	MP8715
MP8715DL**	3x4 QFN14	MP8715

* For Tape & Reel, add suffix –Z (e.g. MP8715DN–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP8715DN–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP8715DL–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP8715DL–LF–Z)

PACKAGE REFERENCE



SOIC8E	3x4 QFN14

ABSOLUTE MAXIMUM RATINGS (1)

VIN……-0.3V to 23V
SW…… ……-0.3V (-5V for <10ns) to 23V
FB, SS……..…….. ……–0.3V to +6.5V
EN/SYNC, POK, VCC.... ……–0.3V to +6.5V
BST to SW .....–0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8E..... 2.5W
3x4 QFN14 ..... 2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature .....–65°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} .....4.5V to 21V
Output Voltage V_{OUT}.....0.8V to V_{IN}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
SOIC8E (Exposed Pad).....	50.....	10 ..	°C/W
3x4 QFN14.....	.....48.....	11 ..	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.66		mA
Shutdown Current	I_{IN}	V_{EN} = 0V			1	μA
IN Undervoltage Lockout Threshold	$INUV_{Vth}$	Rising Edge	3.8	4.0	4.2	V
IN Undervoltage Lockout Hysteresis	$INUV_{HYS}$			880		mV
VCC Regulator	V_{CC}			5.1		V
VCC Load Regulation		I_{CC}=5mA		5		%
Regulated FB Voltage	V_{FB}	T_A = +25°C	0.789	0.805	0.821	V
FB Input Current	I_{FB}	V_{FB} = 0.85V		±50		nA
EN Rising Threshold	V_{EN_RISING}	T_A = +25°C	1.05		1.6	
EN Threshold Hysteresis	V_{EN_HYS}			350		mV
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0V		0		μA
EN Turn Off Delay	EN_{Td-Off}			5		μs
Soft-start current	I_{SS}	V_{SS}=0		5		μA
High-Side Switch On-Resistance	HS_{RDS-ON}			120		mΩ
Low-Side Switch On-Resistance	LS_{RDS-ON}			50		mΩ
SW Leakage Current	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
BST Under Voltage Lockout Threshold	$BSTUV_{Vth}$			2.8		V
High-Side Switch Current Limit (5)	HSI_{LIMIT}	Sourcing	5	7		A
Low-Side Switch Current Limit	LSI_{LIMIT}	Sinking		2		A
Oscillator Frequency	f_{SW}		400	500	600	kHz
Fold-back frequency	f_{FB}			0.25		f_{SW}
Minimum On Time	T_{ON-Min}			70		ns
Maximum Duty Cycle	D_{Max}			100		%
Sync Frequency Range	f_{SYNC}		0.3		2	MHz

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power OK Rising Threshold	POK_{VthLH}			0.90		V_{FB}
Power OK Falling Threshold	POK_{thHL}			0.85		V_{FB}
POK Output Voltage Low	I_{POK_L}	I_{SINK} = 5mA			0.4	V
POK Leakage Current	I_{POK_LEAK}	V_{PG}=3.3V			10	nA
Internal Charge Pump Current	I_{Charge_Pump}			90		µA
Thermal Shutdown Threshold	T_{SD}	Rising		150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note:

5) Guaranteed by design

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PIN FUNCTIONS

SOIC8E Pin#	3x4 QFN14 Pin #	Name	Description
1	1	VIN	Supply Voltage. The MP8715 operates from a +4.5V to +21V input rail. C1 is required to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	2,3,4,5	SW	Switch Output. It is the source of high-side power device.
3	6	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver. An on-chip regulator and charge pump are both used to charge up the external boot-strap capacitor.
4	7	EN/SYNC	EN=1 to enable the MP8715. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN with 100KΩ resistor.
5	8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV.
6	9	POK	Power good signal. When FB is less than 90% of 0.8V, POK is low. It is an open-drain output. Use a high value pull-up resistor externally to pull it up to system power supply.
7	10	VCC	Bias Supply. It's the internal regulator output. Decouple with 0.1μF capacitor.
8	14	SS	Connect to an external capacitor used for Soft-Start.
9	11,12,13, Exposed Pad	GND	Ground (Exposed Pad, also serves as thermal pad)

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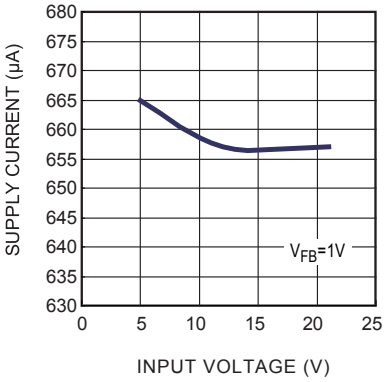
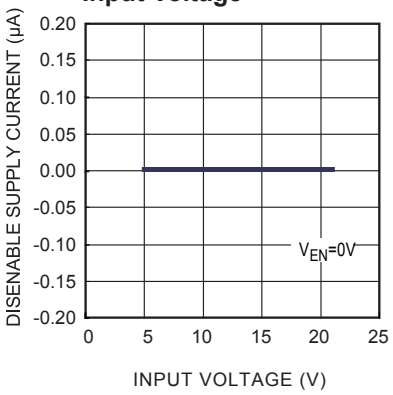
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=1.2V, L=1.8µH, T_A=+25°C, unless otherwise noted.

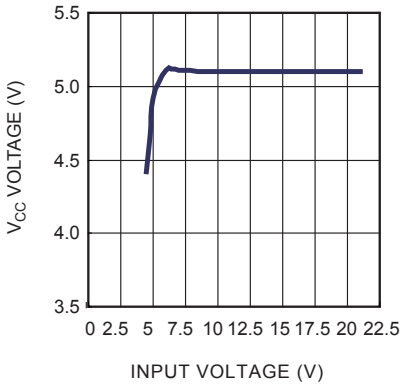
Enabled Supply Current vs. Input Voltage



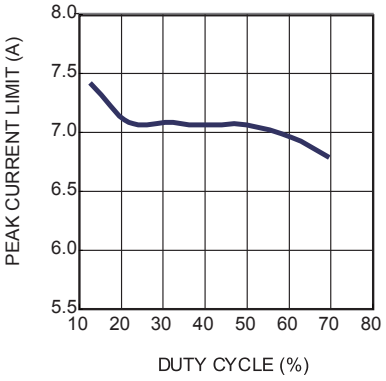
Disabled Supply Current vs. Input Voltage



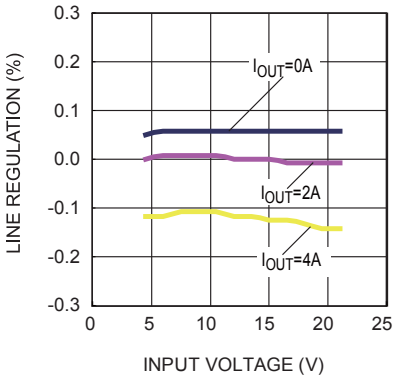
Vcc Regulator Line Regulation



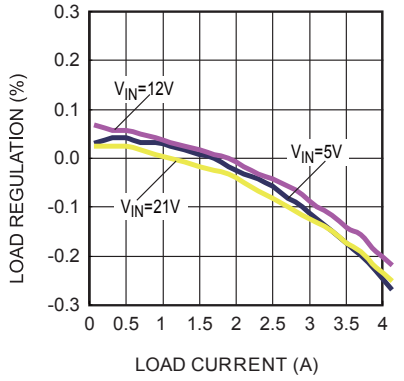
Peak Current vs. Duty Cycle



Line Regulation

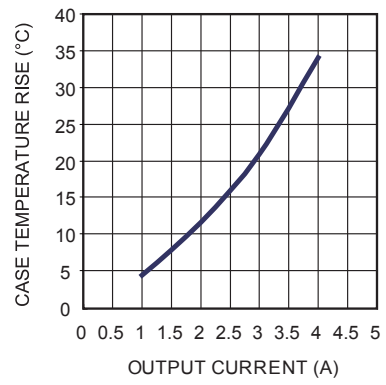


Load Regulation



Case Temperature Rise

V_{OUT}=5V



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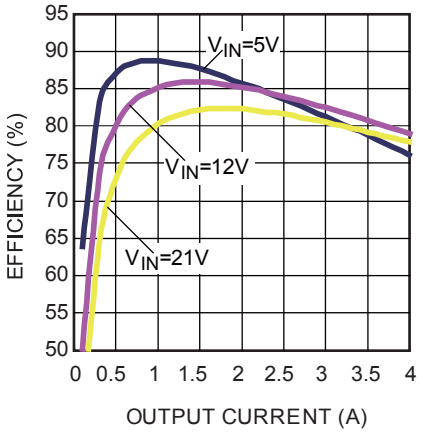
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A=+25°C, unless otherwise noted.

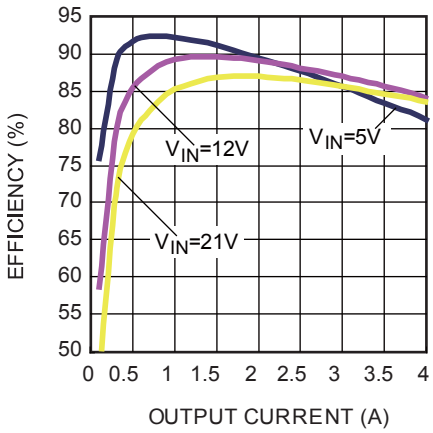
Efficiency

V_{OUT}=1.2V



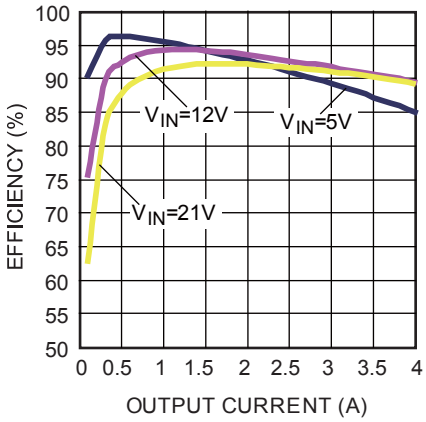
Efficiency

V_{OUT}=1.8V



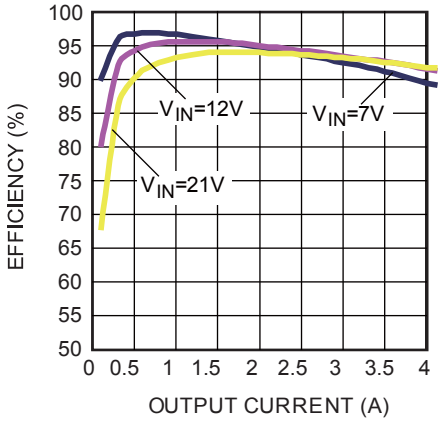
Efficiency

V_{OUT}=3.3V



Efficiency

V_{OUT}=5V



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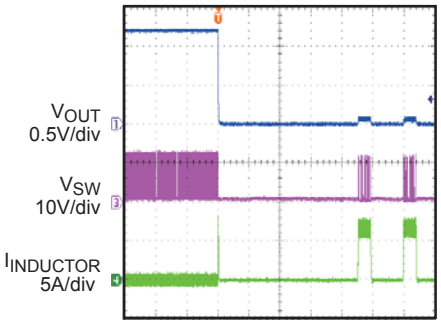
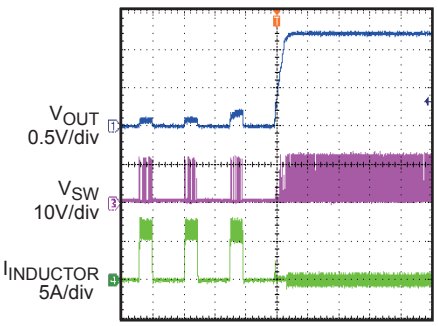
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=1.8µH, T_A=+25°C, unless otherwise noted.

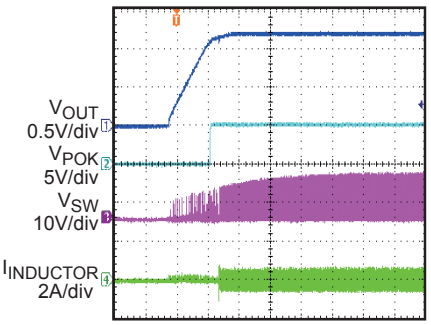
Short Entry



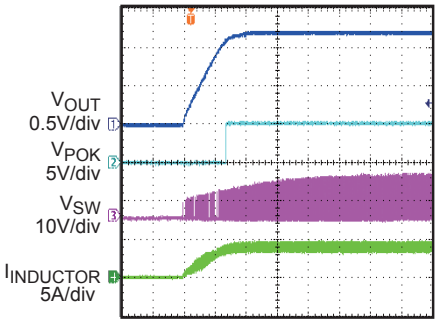
Short Recovery



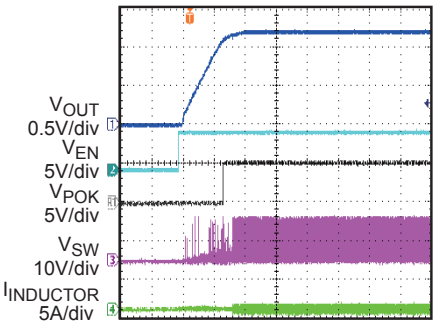
Power up without Load



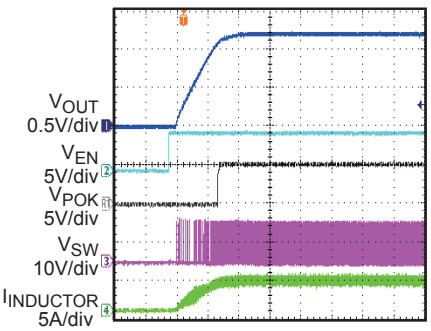
Power up with 4A Load



Enable Startup without Load

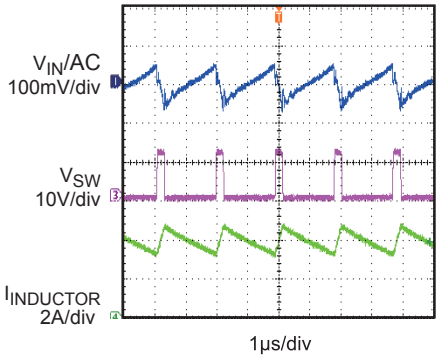


Enable Startup with 4A Load



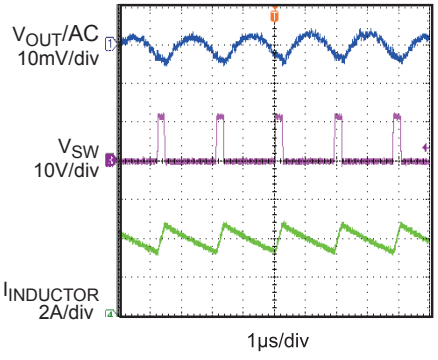
Input Ripple Voltage

I_{OUT}=4A



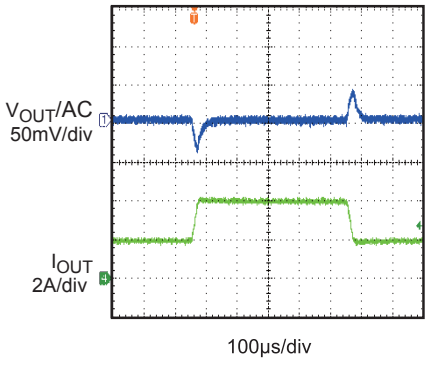
Output Ripple Voltage

I_{OUT}=4A



Load Transient Response

I_{OUT}=2A to 4A



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BLOCK DIAGRAM

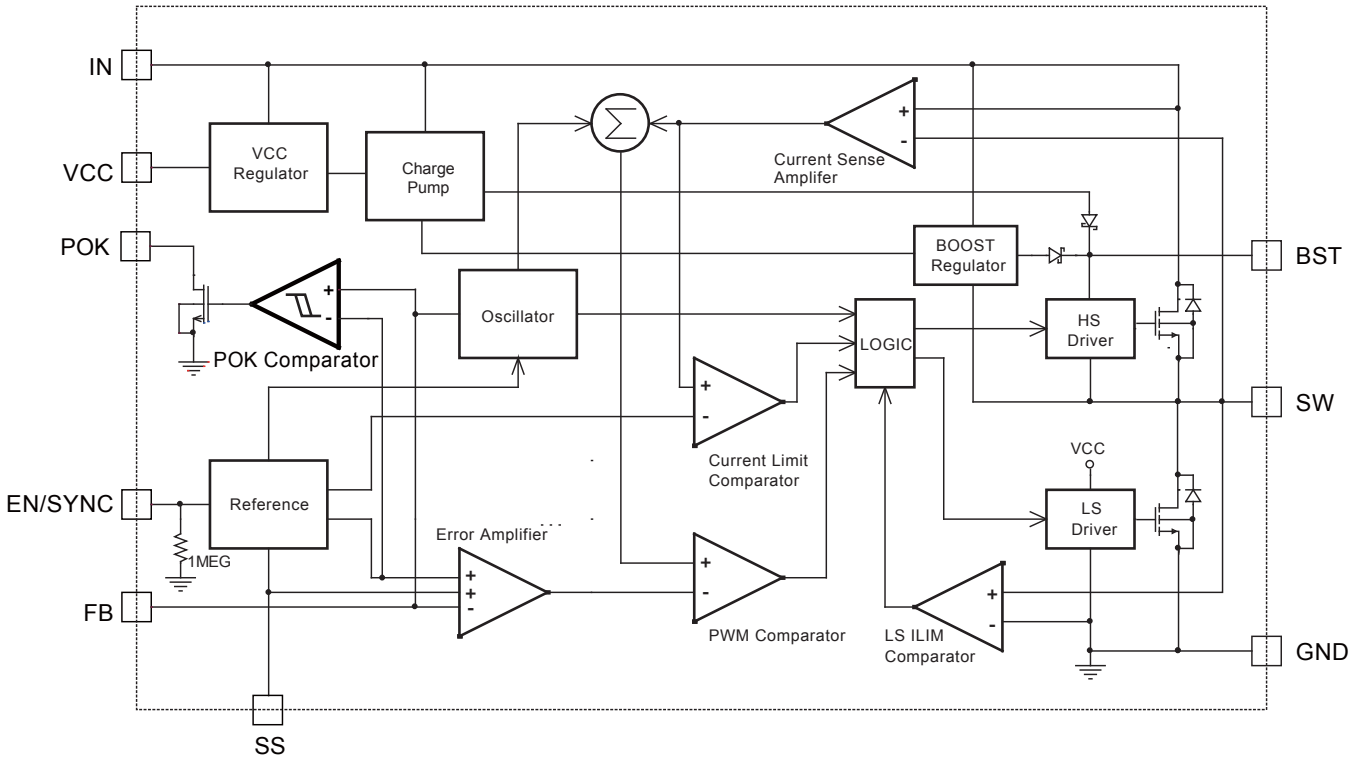

Figure 1—Functional Block Diagram

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OPERATION

The MP8715 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 4A continuous output current over a wide input supply range with excellent load and line regulation.

The MP8715 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in whole of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will work at 100% duty cycle.

Internal Regulator

Most of the internal circuitries are powered from the 5.1V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.1V, the output of the regulator is in full regulation. When VIN is lower than 5.1V, the output decreases, a 0.1uF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.805V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable/Sync Control

EN/Sync is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive it low to turn it off. There is an internal 1MEG resistor from EN/Sync to GND thus EN/Sync can be floated to shut down the chip.

1) Enabled by external logic H/L signal

The chip starts up once the enable signal goes higher than EN/SYNC input high voltage (2V), and is shut down when the signal is lower than EN/SYNC input low voltage (0.4V). To disable the chip, EN must be pulled low for at least 5μs. The input is compatible with both CMOS and TTL.

2) Enabled by Vin through voltage divider.

Connect EN with Vin through a resistive voltage divider for automatic startup as the figure 2 shows.

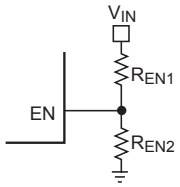

Figure 2—Enable Divider Circuit

Choose the value of the pull-up resistor R_{EN1} and pull-down resistor R_{EN2} to reset the automatic start-up voltage:

$$V_{IN_START} = V_{EN_RISING} \cdot \frac{(R_{EN1} + R_{EN2} \,||\, 1M\Omega)}{R_{EN2} \,||\, 1M\Omega}$$

Where V_{EN_RISING} is 1.12V

$$V_{IN_STOP} = V_{EN\text{-}FALLING} \cdot \frac{(R_{EN1} + R_{EN2} \,||\, 1M\Omega)}{R_{EN2} \,||\, 1M\Omega}$$

Where $V_{EN_FALLING}$ is 0.9V

The startup sequence is as below using the EN divider. $V_{CC\text{-}Rising}$ is the VCC UVLO rising threshold which is about 4.0V.

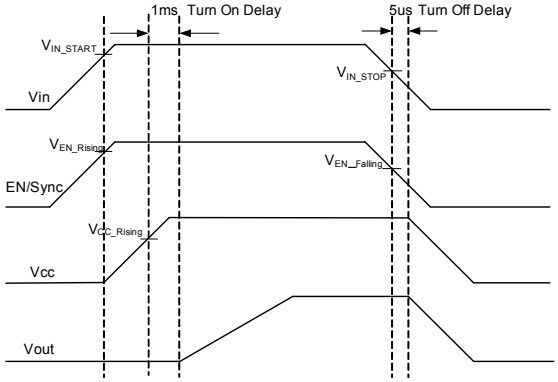

Figure 3—Startup Sequence Using EN Divider

3) Synchronized by External Sync Clock Signal

The chip can be synchronized to external clock range from 300kHz up to 2MHz through this pin 2ms right after output voltage is set, with the

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internal clock rising edge synchronized to the external clock rising edge.

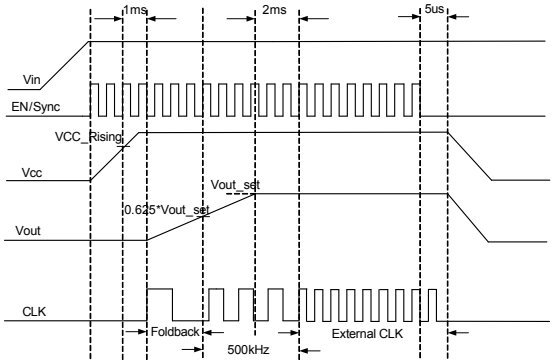

Figure 4—Startup Sequence Using External Sync Clock Signal

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP8715 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.1V.

Power OK Indicator

When the FB is below 0.85VFB, the POK pin will be internally pulled low. When the FB is above 0.9VFB , the POK becomes an open-drain output. If POK function is not used, it can be left open.

External Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 3.5V. When it is lower than the internal FB reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time can be set by external decoupled cap. The soft-start time can be calculated as below:

$$t_{SS}(ms) = \frac{Vref(V) \times C_5(nF)}{5\mu A}$$

To reduce the susceptibility to noise, do not leave SS pin open. Use a capacitor with small value if you do not need soft function.

Over-Current-Protection and Hiccup

The MP8715 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the MP8715 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP8715 exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.5V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, D2, M3, C4, L1 and C2 (Figure 5). If (VIN-VSW) is more than 5V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

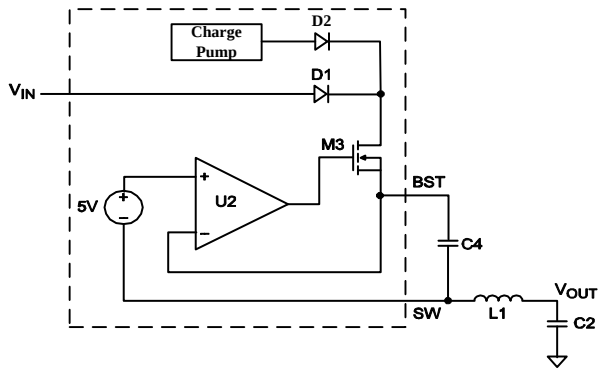

Figure 5—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The

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reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

The T-type network is highly recommended when Vo is low, as Figure 6 shows.

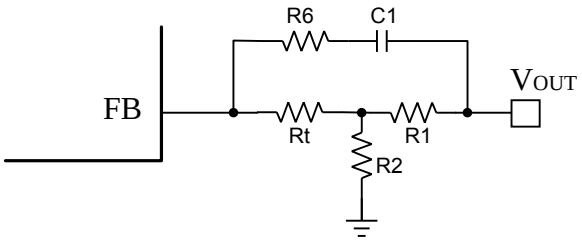

Figure 6— T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	R6 (kΩ)	C1 (pF)	L (μH)	C_{OUT} (μF)
1.05	4.99	16.5	47	0	15	1.8	22×2
1.2	4.99	10.2	47	0	15	1.8	22×2
1.5	4.99	5.76	47	0	15	2.2	22×2
1.8	4.99	4.02	33	0	15	2.2	22×2
2.5	40.2	19.1	10	0	27	3.3	22×2
3.3	40.2	13	4.99	0	33	3.3	22×2
5	40.2	7.68	3	0	47	4.7	22×2

Note:
The above feedback resistor table applies to a specific load capacitor condition as shown in the table 1. Other capacitive loading conditions will require different values.

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor ripple current to be approximately 30% if the maximum load current, 4A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close

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to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8715 can be optimized for a wide range of capacitance and ESR values.

PCB Layout

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure 7, 8 for references. 4 layer PCB is recommended.

1) Keep the connection of input ground and GND pin as short and wide as possible.
2) Keep the connection of input capacitor and IN pin as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.
6) Adding RC snubber circuit from IN pin to SW pin can reduce SW spikes.

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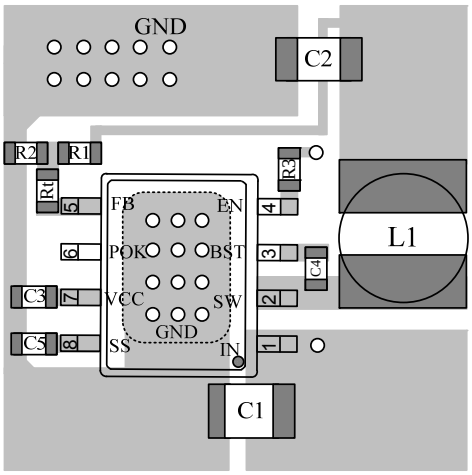
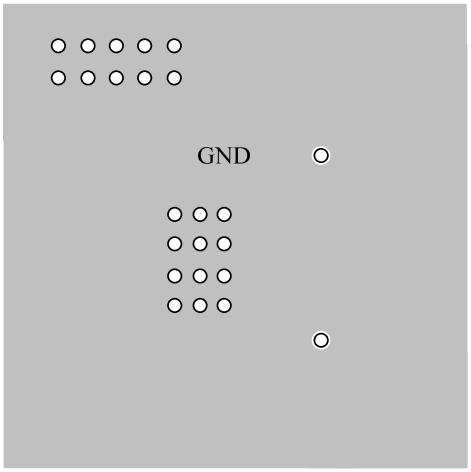
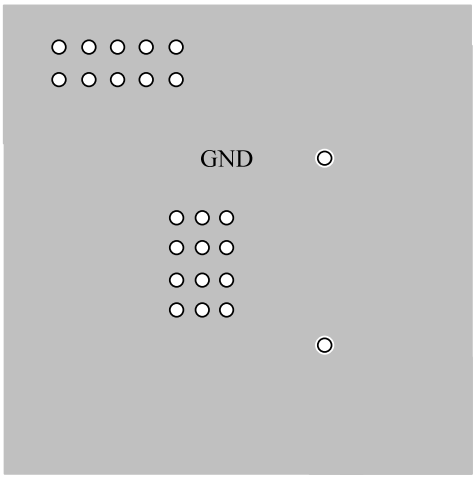


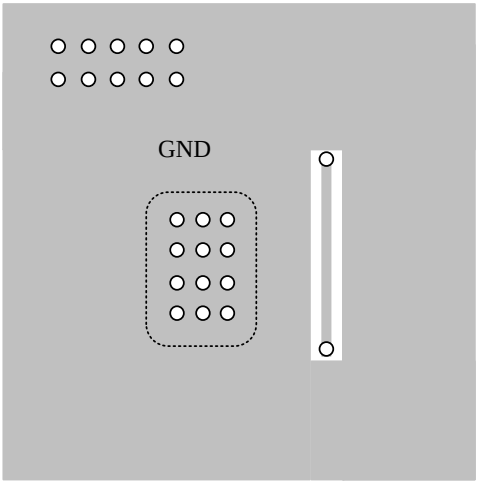
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure 7—MP8715DN Layout Guide

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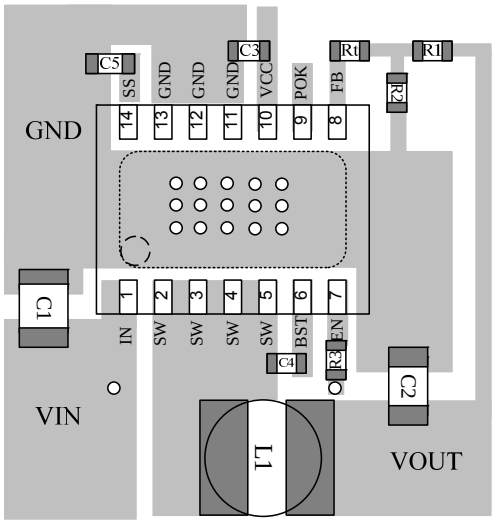
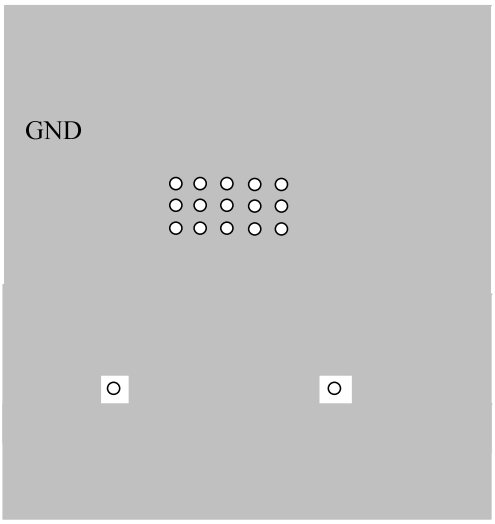
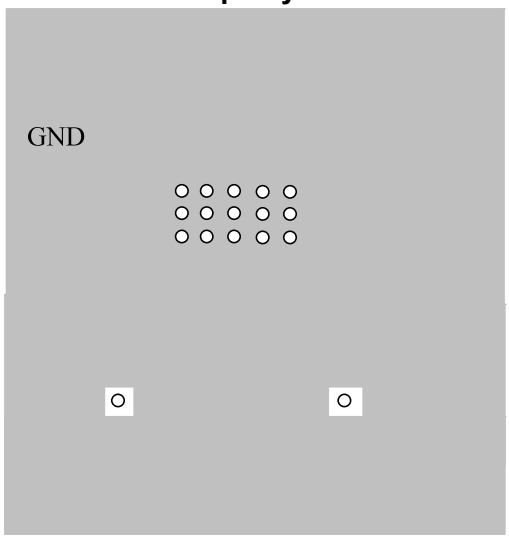


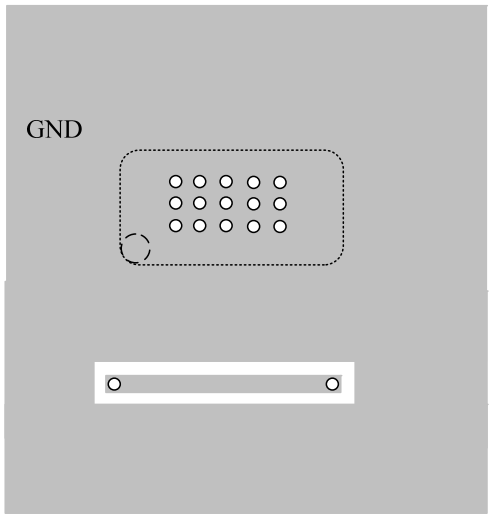
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure 8—MP8715DL Layout Guide

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TYPICAL APPLICATION CIRCUITS (SOIC8E Package)

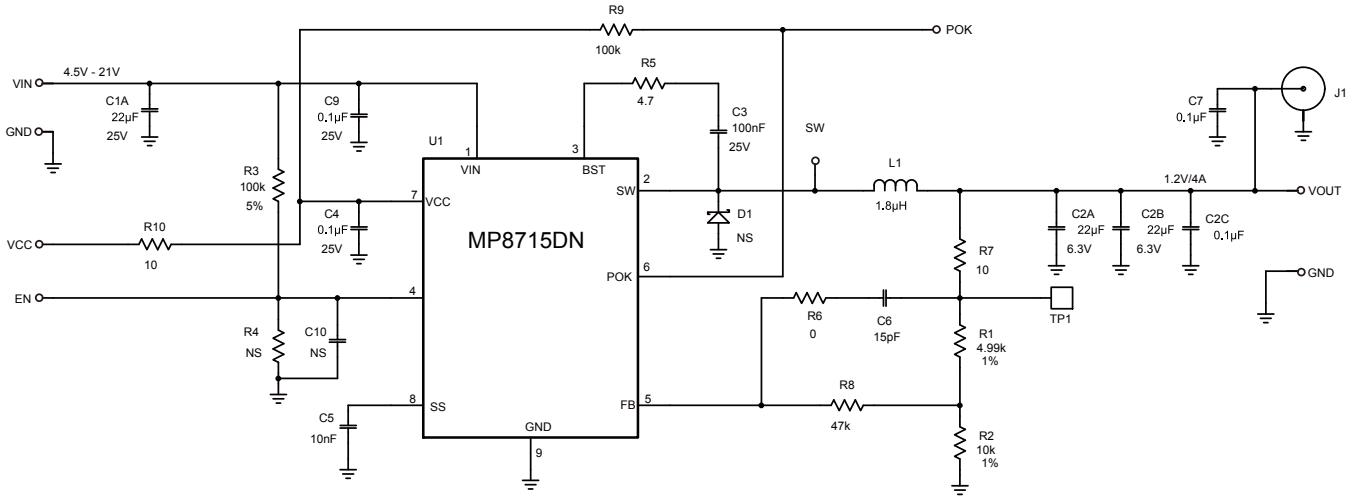

Figure 9— 1.2V Output Typical Application Schematic

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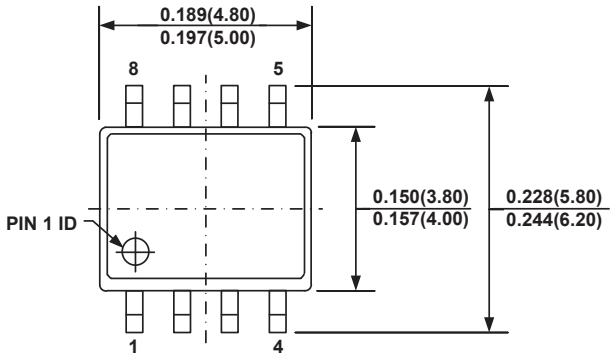
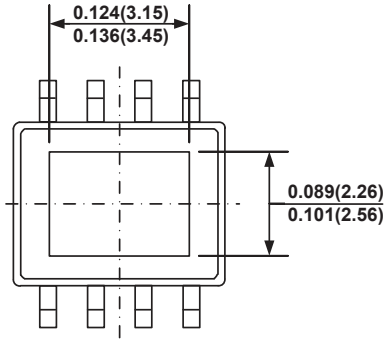
PACKAGE INFORMATION

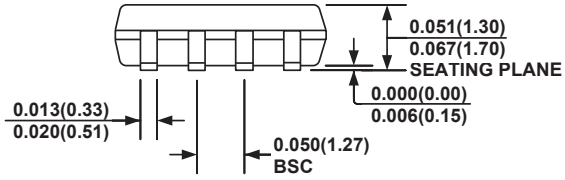
SOIC8E (Exposed Pad)



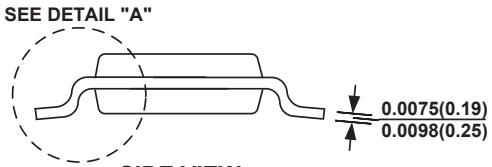
TOP VIEW



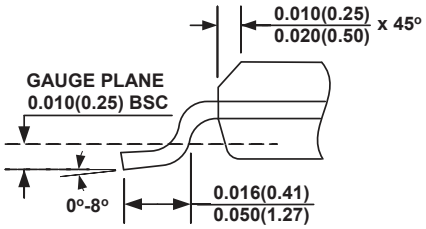
BOTTOM VIEW



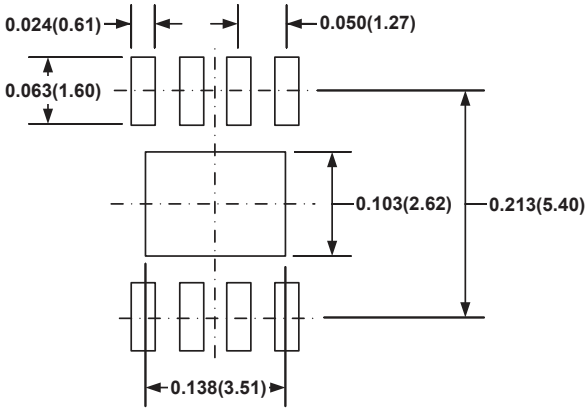
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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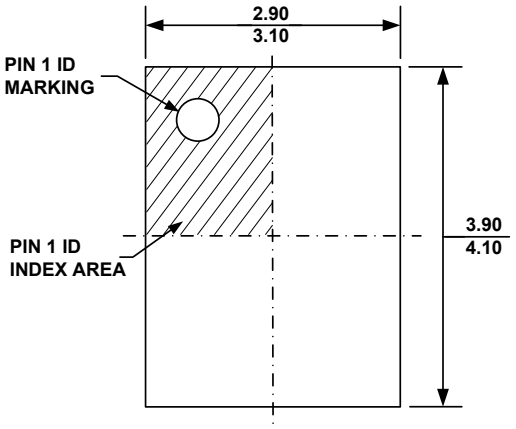
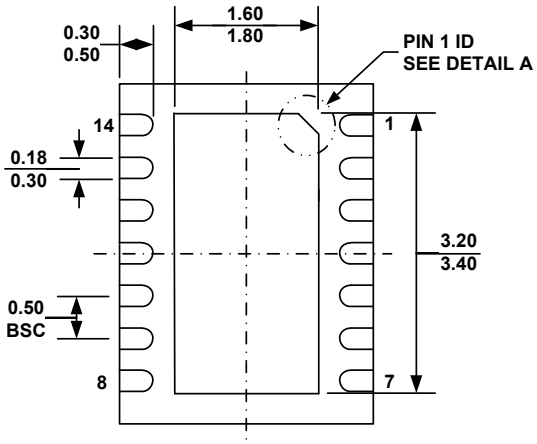
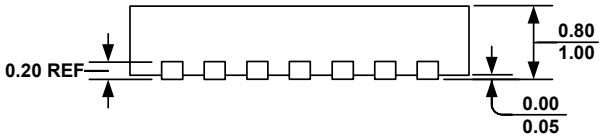
3mm x 4mm QFN14



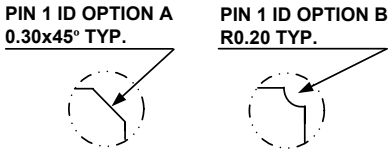
TOP VIEW



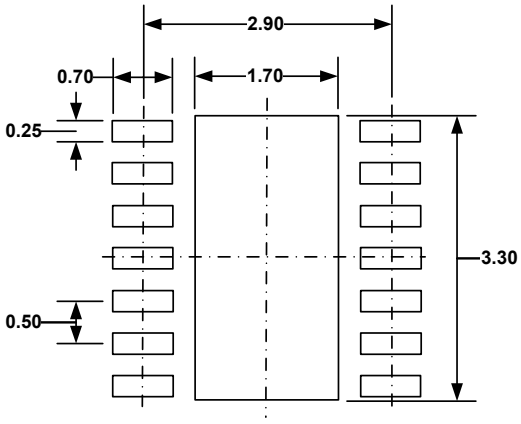
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE.

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