MP7626

Microprocessor Compatible
Buffered Multiplying 16-Bit
Digital-to-Analog Converter

FEATURES

- **Four Quadrant Multiplication**
- **16-Bit Monotonicity**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Single-Buffered or Transparent Data inputs**
- **Decoded DAC Approach**
- **Latch-Up Free**
- **8-Bit Bus Version: MP7636A**

APPLICATIONS

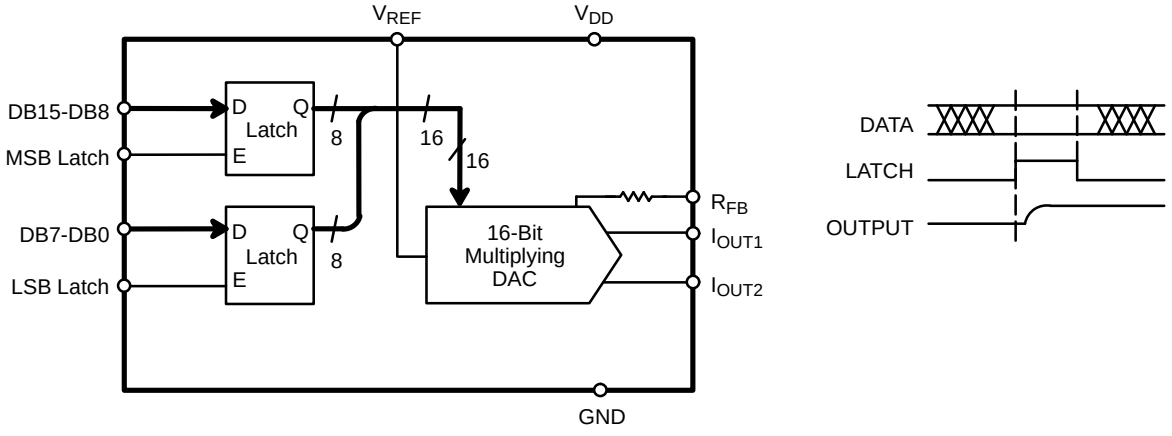
- **Digitally Programmable References**
- **Programmable Audio Attenuator**
- **High Accuracy Process Control Systems**
- **Automatic Test Equipment**
- **Easy Interface to 8 and 16-Bit Microprocessor Buses**

GENERAL DESCRIPTION

The MP7626 is a CMOS 16-bit Digital-to-Analog Converter (DAC) that is manufactured using advanced thin film resistors on a double metal CMOS process. It incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 16 bit differential non-linearity is achieved with minimal trimming.

Two 8-bit latches (MSB latch and LSB latch) hold the 16-bit data which are converted by the DAC. A 16-bit bus can load both latches in one cycle. An 8-bit bus loads one latch at a time. By making the latches transparent (MSB latch = LSB latch = High) the DAC will continuously convert the BIT1 - BIT16 inputs.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



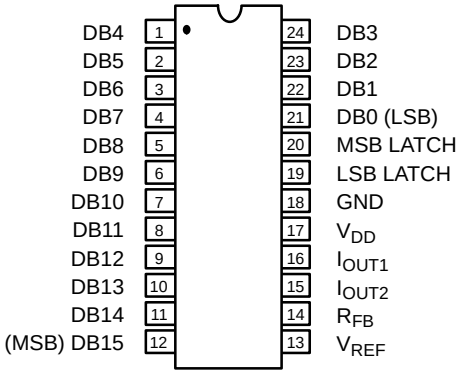
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7626JN	±4	±4	±0.1
Plastic Dip	–40 to +85°C	MP7626KN	±2	±2	±0.1
PLCC	–40 to +85°C	MP7626JP	±4	±4	±0.1
PLCC	–40 to +85°C	MP7626KP	±2	±2	±0.1
Ceramic Dip	–40 to +85°C	MP7626JD*	±4	±4	±0.1
Ceramic Dip	–40 to +85°C	MP7626KD*	±2	±2	±0.1

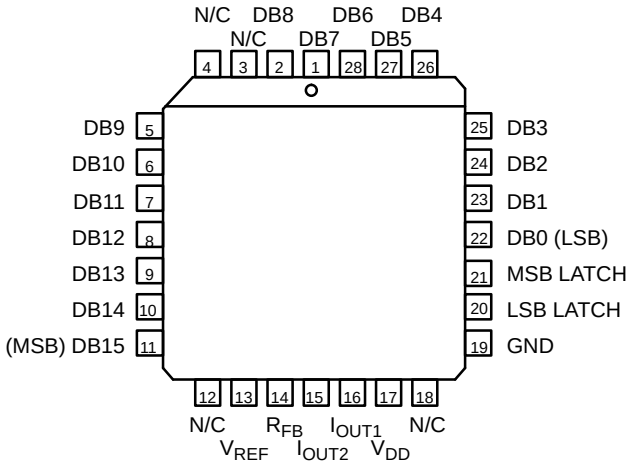
*Recommend using MP7626KN or JN

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin PDIP, CDIP (0.600")
N24, D24, C24



28 Pin PLCC
P28

PIN OUT DEFINITIONS

DIP	PLCC	NAME	DESCRIPTION
1	26	DB4	Data Input Bit 4
2	27	DB5	Data Input Bit 5
3	28	DB6	Data Input Bit 6
4	1	DB7	Data Input Bit 7
5	2	DB8	Data Input Bit 8
6	5	DB9	Data Input Bit 9
7	6	DB10	Data Input Bit 10
8	7	DB11	Data Input Bit 11
9	8	DB12	Data Input Bit 12
10	9	DB13	Data Input Bit 13
11	10	DB14	Data Input Bit 14
12	11	DB15	Data Input Bit 15 (MSB)

DIP	PLCC	NAME	DESCRIPTION
13	13	V_{REF}	Reference Input Voltage
14	14	R_{FB}	Internal Feedback Resistor Pin
15	15	I_{OUT2}	Current Output 2
16	16	I_{OUT1}	Current Output 1
17	17	V_{DD}	Power Supply
18	19	GND	Ground
19	20	LSB	LSB Latch Enable
20	21	MSB	MSB Latch Enable
21	22	DB0	Data Input Bit 0 (LSB)
22	23	DB1	Data Input Bit 1
23	24	DB2	Data Input Bit 2
24	25	DB3	Data Input Bit 3

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	16			16		Bits	
Relative Accuracy	INL						LSB	Best Fit Straight Line Spec.
J				±4		±4		(Max INL – Min INL) / 2
K				±2		±2		
Differential Non-Linearity	DNL						LSB	
J				±4		±4		
K				±2		±2		
Gain Error	GE			±0.1		±0.1	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10		±200	nA	I_{OUT1}
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S		2				µs	Full Scale Change to 0.1%
AC Feedthrough at I_{OUT1}	F_T		2				mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	2.5		7.5	2.5	7.5	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
Input Capacitance[2]								
Data	C_{IN}		5				pF	
Control	C_{IN}		5				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			280			pF	DAC Inputs all 1's
	C_{OUT1}			120			pF	DAC Inputs all 0's
	C_{OUT2}			100			pF	DAC Inputs all 1's
	C_{OUT2}			240			pF	DAC Inputs all 0's
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	4.5		16.5	5.0	16.5	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Data Valid to Write Set-Up Time	t_{DS}	250					ns	
Write Strobe Width	t_{SW}	125					ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

Supply Voltage . . . . . +17 V_{DC}
Voltage at Any Digital Input . . . . . GND –0.5 to V_{DD} +0.5 V
DC Voltage Applied to I_{OUT1} or I_{OUT2} . . GND –0.5 to +17 V
Voltage at V_{REF}, R_{FB} Inputs . . . . . ±25 V

Storage Temperature Range . . . . . –65°C to 150°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, PLCC 1050mW
Derates above 75°C . . . . . 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

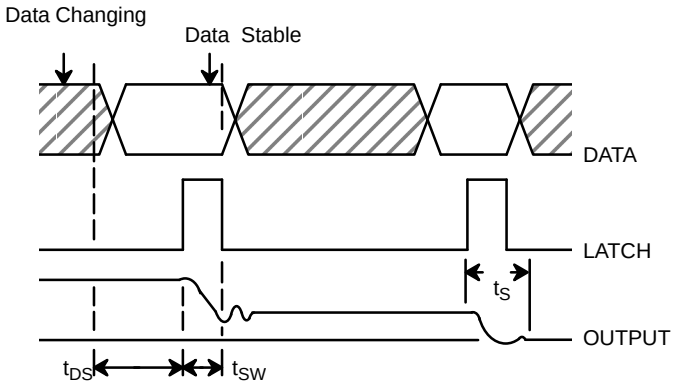
APPLICATION NOTES

Refer to Applications Section for Additional Information

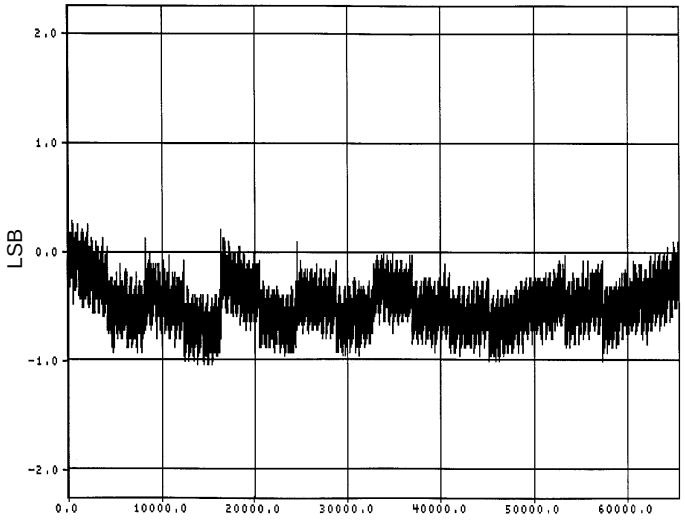
LATCH CONTROL

MSB LATCH	LSB LATCH	FUNCTION
0	0	Data Latched (Held)
1	0	Transfer (DB15-DB8) to DAC
0	1	Transfer (DB7-DB0) to DAC
1	1	Transparent Mode

TIMING DIAGRAM



PERFORMANCE CHARACTERISTICS

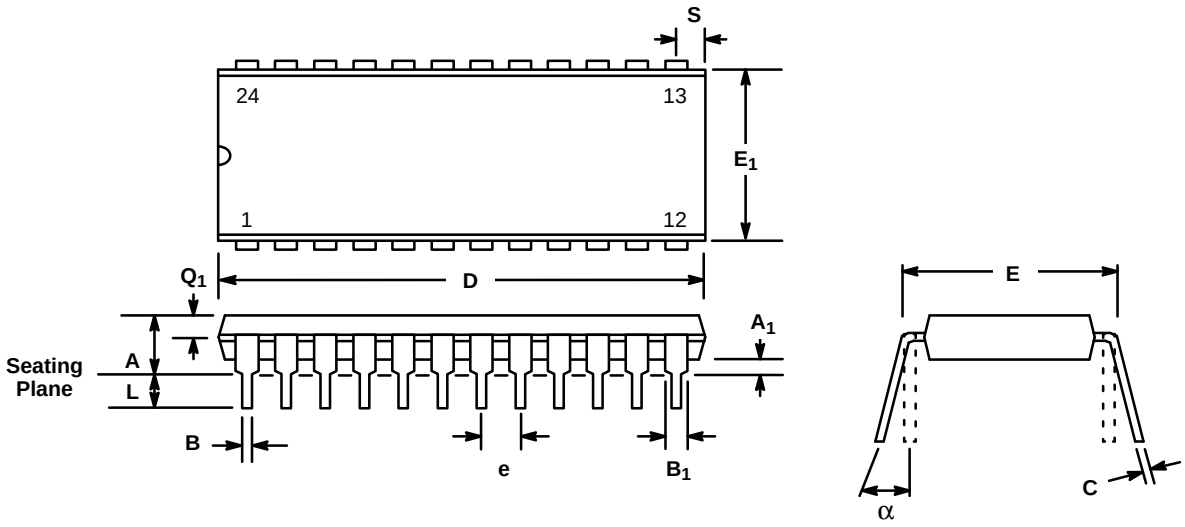


Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

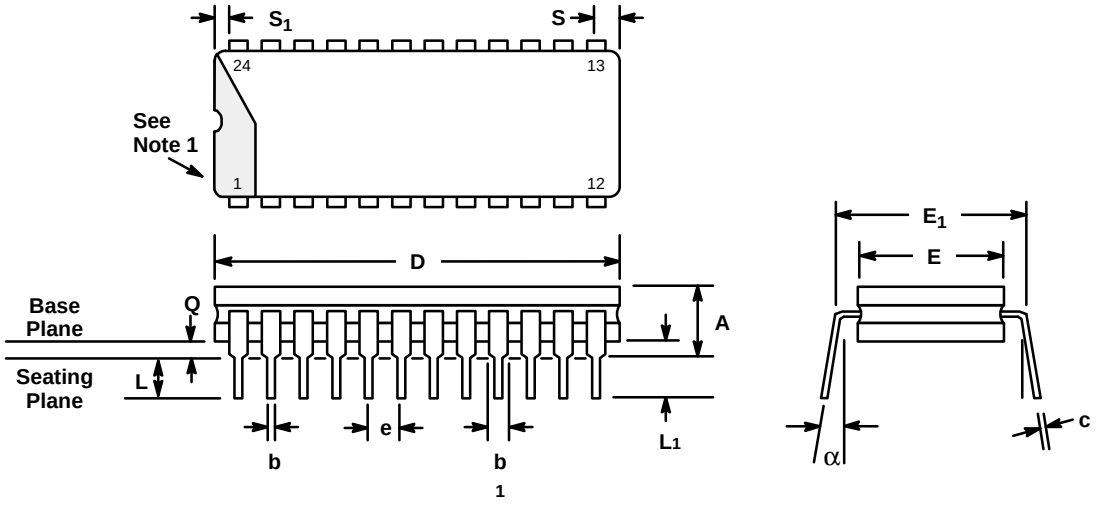
24 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.160	1.290	29.46	32.77
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

24 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D24

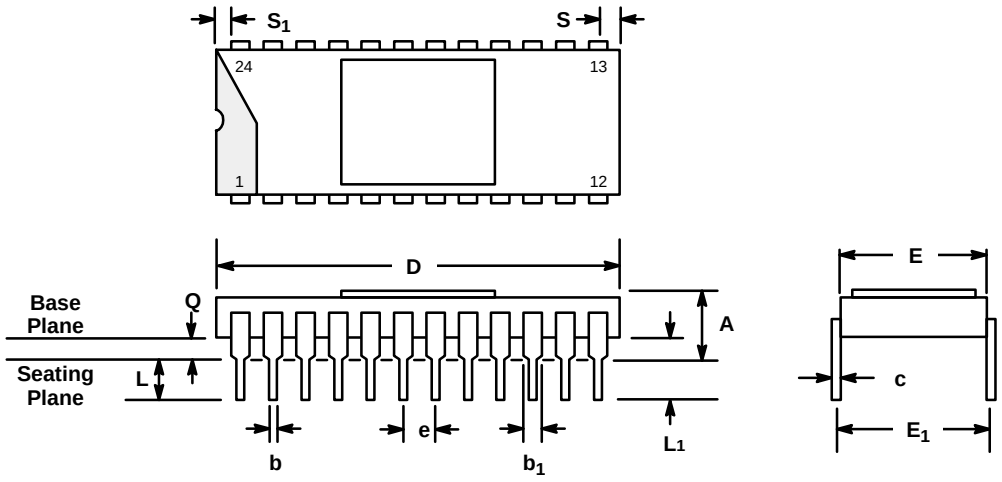


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.381	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

24 LEAD CERAMIC SIDE-BRAZED DUAL-IN-LINE
(600 MIL S/B DIP)
C24

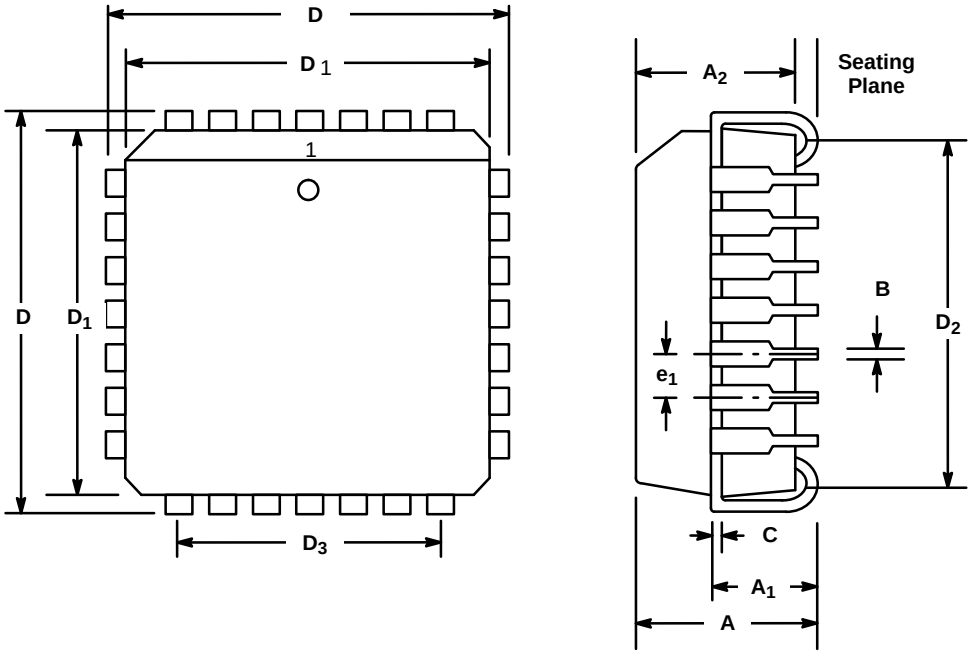


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.381	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. E_1 shall be measured at the centerline of the leads.

28 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P28



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.485	0.495	12.32	12.57
D_1 (1)	0.450	0.454	11.43	11.53
D_2	0.390	0.430	9.91	10.92
D_3	0.300 Ref		7.62 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

Notes

Notes

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