MP6905

Fast Turn-off, Intelligent Rectifier

The Future of Analog IC Technology

DESCRIPTION

The MP6905 is a low-drop, diode-emulator IC with external switch; MP6905 replaces Schottky diodes in high-efficiency, flyback converters. The chip regulates the forward drop of the external switch (about 30mV) and switches it off when the voltage becomes negative. MP6905 has a light-load sleep mode that reduces the quiescent current to <300uA.

MP6905 is available in a compact SOIC-8 package.

FEATURES

- Works with 12V Standard and 5V Logic Level FETS
- Compatible with Energy Star, 1W Standby Requirements
- Fast Turn-off, Total Delay 20ns
- <300uA Quiescent Current at Light-Load Mode
- Supports CCM, DCM and Quasi-Resonant Topologies
- Supports High-side and Low-side Rectification
- Saves Up to 1.5W in a Typical Notebook Adapter
- Available in a SOIC-8 Package

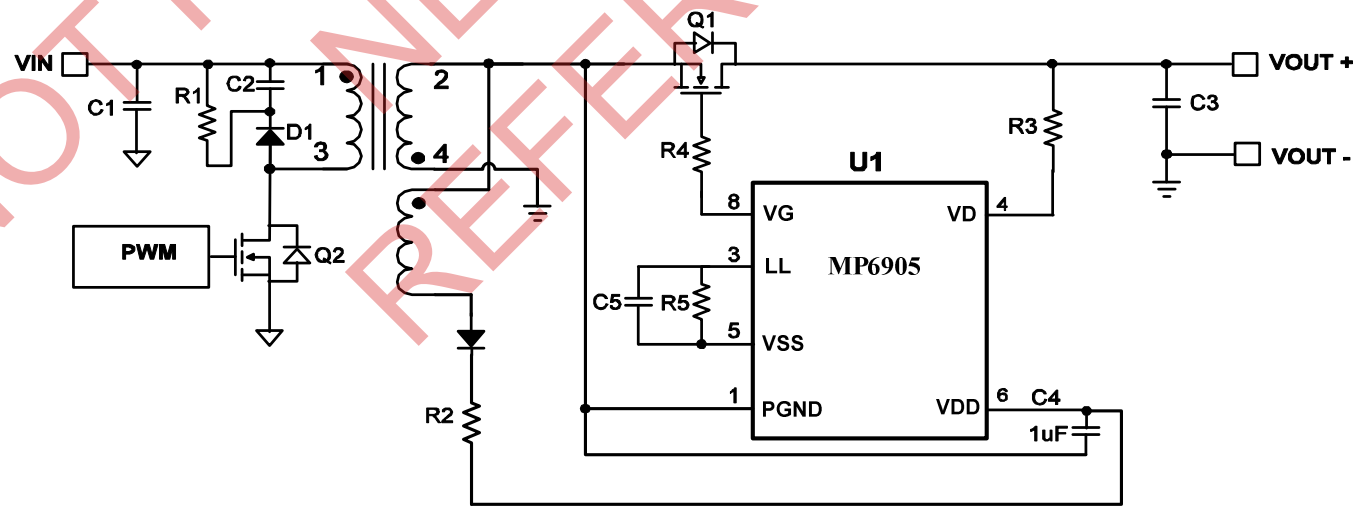
APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP6905GS*	SOIC-8	*See Below*

* For Tape & Reel, RoHS Compliant Packaging, add suffix –Z (e.g. MP6905GS–Z);

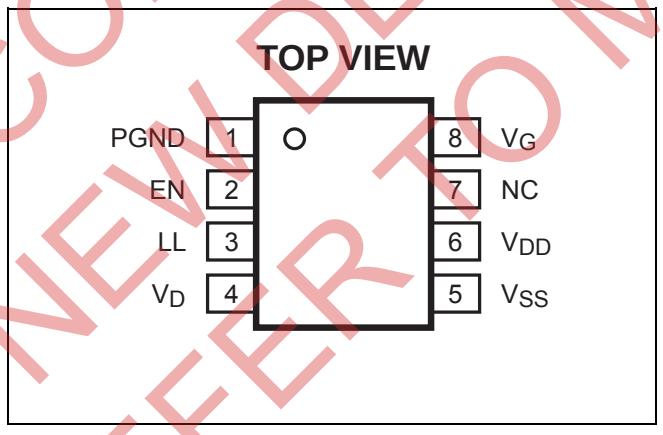
TOP MARKING

MP6905
LLLLLLLL
MPSYWW

MP6905: part number;
LLLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to V_{SS} ..... –0.3V to +27V
PGND to V_{SS} ..... –0.3V to +0.3V
V_G to V_{SS} ..... –0.3V to V_{CC}
V_D to V_{SS} ..... –0.7V to +180V
LL, EN to V_{SS} ..... –0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8 ..... 1.4W
Junction Temperature ..... 150°C
Lead Temperature (Solder) ..... 260°C
Storage Temperature ..... –55°C to +150°C

Recommended Operation Conditions (3)

V_{DD} to V_{SS} ..... 8V to 24V
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8	90	45 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C,unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} Voltage Range			8		24	V
V_{DD} UVLO Rising			5.0	6.0	7.0	V
V_{DD} UVLO Hysteresis			0.8	1	1.25	V
Operating Current	I_{CC}	C_{LOAD}=5nF, F_{SW}=100kHz		8	10	mA
Quiescent Current	I_q	V_{SS}-V_D=0.5V		2	3.6	mA
Shutdown Current		V_{DD} =4V			260	µA
		V_{DD}=20V, EN=0V			500	
Light-Load Mode Current				300	400	µA
Thermal Shutdown (5)				150		°C
Thermal Shutdown Hysteresis (5)				30		°C
Enable UVLO Rising	V_{EN-R}		1.1	1.5	1.9	V
Enable UVLO Hysteresis				0.2	0.4	V
Internal Pull-Up Current On EN				10	15	µA
CONTROL CIRCUITRY SECTION						
V_{SS} –V_D Forward Voltage	V_{fwd}		20	32	44	mV
Turn-On Delay	T_{Don}	C_{LOAD} = 5nF, -20°C≤T_J≤125°C		150	250	ns
		C_{LOAD} = 5nF, -40°C≤T_J<-20°C		250		
	T_{Don}	C_{LOAD} = 10nF, -20°C≤T_J≤125°C		250	350	ns
		C_{LOAD} = 10nF, -40°C≤T_J<-20°C		350		
Input Bias Current On V_D		V_D = 180V			1	µA
Minimum On Time	T_{MIN}	C_{LOAD} = 5nF	0.6	1.2	1.9	µs
Light-Load-Enter Delay	$T_{LL-Delay}$	R_{LL}=100kΩ	70	100	130	µs
Light-Load-Enter Pulse Width	T_{LL}	R_{LL}=100kΩ	1.2	1.9	2.6	µs
Light-Load-Enter Pulse Width Hysteresis	T_{LL-H}	R_{LL}=100kΩ		0.2		µs
Light-Load Resistor Value	R_{LL}		30		300	kΩ
Light-Load Mode Exit-Pulse Width Threshold (V_{DS})	V_{LL-DS}		-380	-250	-120	mV
GATE DRIVER SECTION						
V_G (Low)	V_{G-L}	I_{LOAD}=1mA		0.05	0.1	V
V_G (High)	V_{G-H}	V_{DD} >17V	13	14.8	16.5	V
		V_{DD} <17V		V_{DD}-2.2		
Turn-Off Threshold (V_{SS}-V_D)	V_{off}		-23	-5	13	mV
Turn-Off Propagation Delay		V_D=V_{SS}		15		ns
Turn-Off Total Delay	T_{Doff}	V_D =V_{SS}, C_{LOAD}=5nF, R_{GATE}=0Ω		35	70	ns
	T_{Doff}	V_D =V_{SS}, C_{LOAD}=10nF, R_{GATE}=0Ω		45	70	ns
Pull-Down Impedance				1	2	Ω
Pull-Down Current (5)		3V <V_G<10V		2		A

Notes:

5）Guaranteed by Characterization

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PIN FUNCTIONS

Pin #	Name	Description
1	PGND	Power Ground. The return for the driver switch.
2	EN	Enable (active high)
3	LL	Light-load timing setting. Connect a resistor to set the light-load timing.
4	VD	FET (drain-voltage sense)
5	VSS	Ground, also used as reference for VD.
6	VDD	Supply Voltage
7	NC	No connection
8	VG	Gate drive output

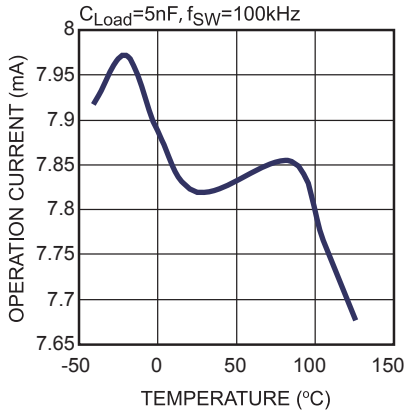
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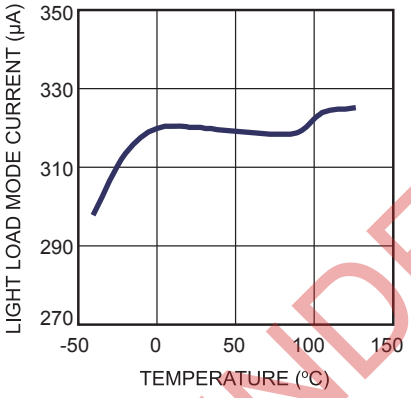
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, unless otherwise noted.

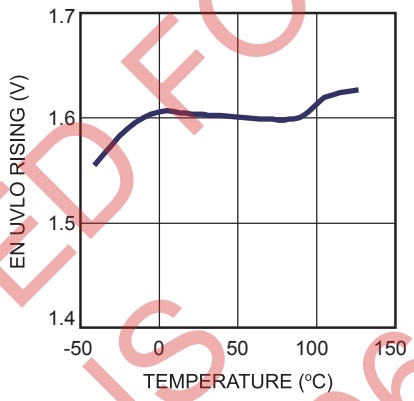
Operation Current vs. Temperature



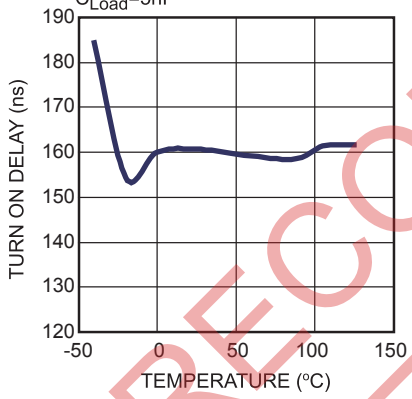
Light-Load Mode Current vs. Temperature



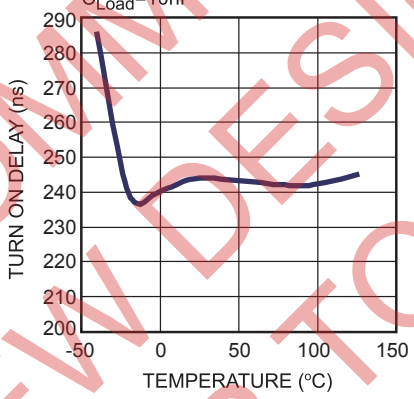
EN UVLO Rising vs. Temperature



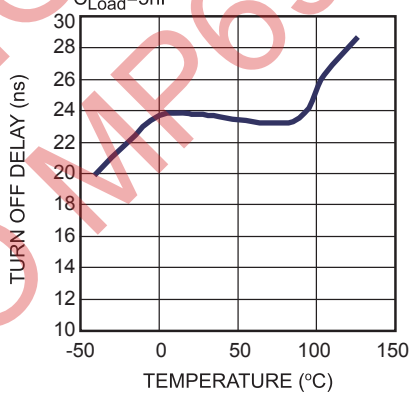
Turn-On Delay vs. Temperature



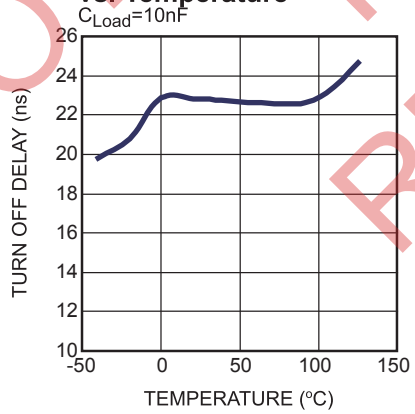
Turn-On Delay vs. Temperature



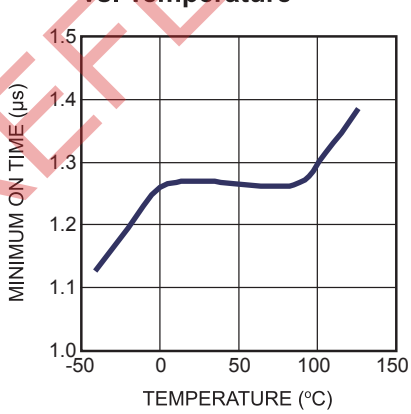
Turn-Off Delay vs. Temperature



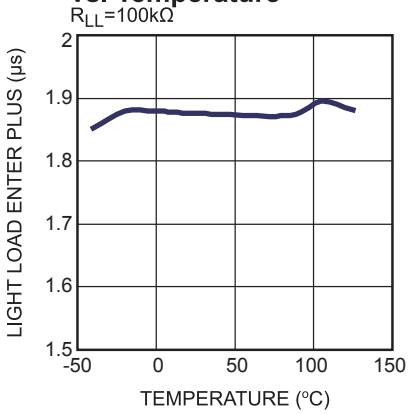
Turn-Off Delay vs. Temperature



Minimum On Time vs. Temperature



Light-Load-Enter Pluse Width vs. Temperature



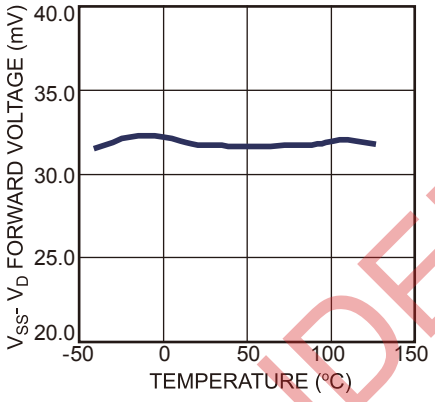
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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V_{SS}-V_D Forward Voltage vs. Temperature



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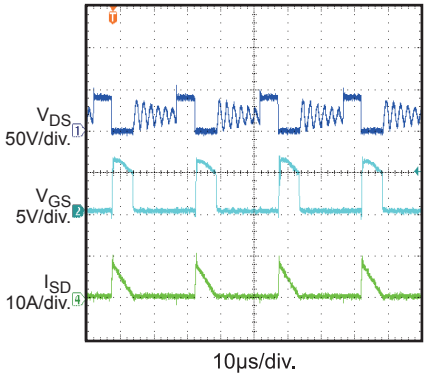
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, unless otherwise noted.

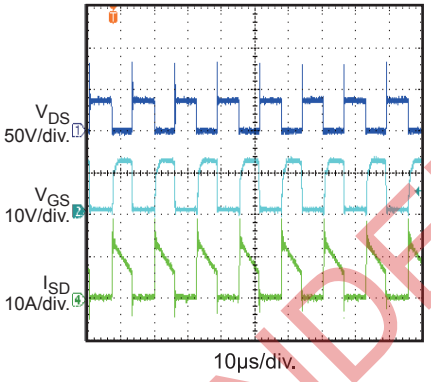
Operation in 90W Flyback Application(6)

V_{IN} = 90Vac, I_{OUT} = 1A



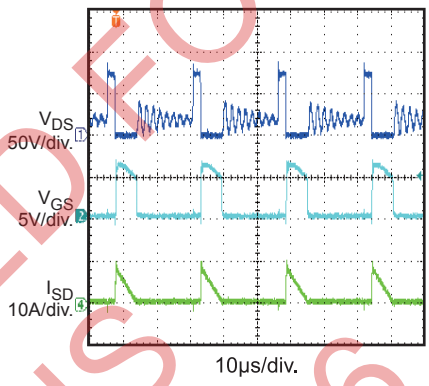
Operation in 90W Adapter Application

V_{IN} = 90Vac, I_{OUT} = 4.7A



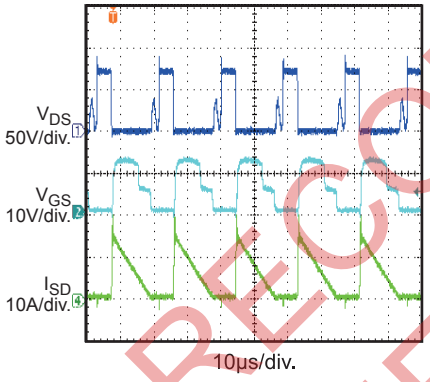
Operation in 90W Flyback Application

V_{IN} = 250Vac, I_{OUT} = 1A



Operation in 90W Adapter Application

V_{IN} = 250Vac, I_{OUT} = 4.7A



Notes:

6）See Figure 14 for the test circuit

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BLOCK DIAGRAM

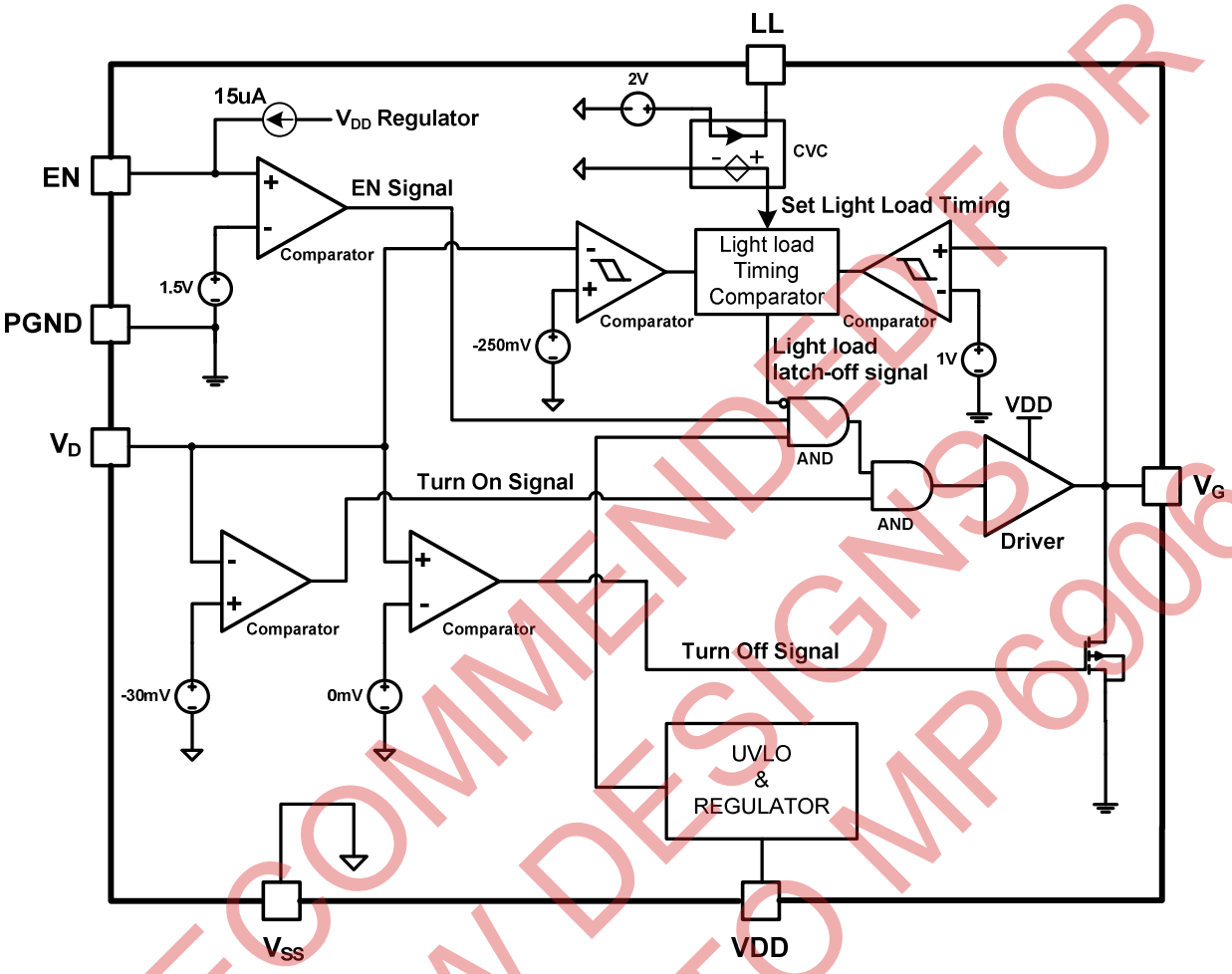


Figure 1:Functional Block Diagram

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OPERATION

The MP6905 operates in CCM, DCM and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is low.

Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on/off, it allows the on/off state to last for an extended period of time. The turn-on blanking time is ~1.6us, which determines the minimum on time. During the turn-on blanking period, the turn-off threshold is blanked.

VD Clamp

V_D can reach up to 180V, which requires a high-voltage JFET at the input. To avoid excessive currents if V_G goes below -0.7V, a small resistor is recommended between V_D and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

If V_{DD} is below the UVLO threshold, the part enters sleep mode, and V_G is pulled down by a 10kΩ resistor.

Enable

If EN is pulled low, the part enters shutdown mode, consuming <100uA shutdown current.

Thermal Shutdown (TSD)

If the junction temperature of the chip exceeds 170°C, the V_G is pulled low and the part stops switching. The part returns to normal functioning after the junction temperature drops to 120°C.

Turn-On Phase

When the switch current flows through the body diode of the MOSFET, it carries a negative V_{DS} (V_D-V_{SS}) across (<-500mV). The V_{DS} is much lower than the turn-on threshold of the control circuitry (-30mV). This turns the MOSFET on after a 200ns turn-on delay (see Figure 2).

When the turn-on threshold (-30mV) is triggered, a blanking time (minimum on time) is added. This causes the turn-off threshold to be blanked. The blanking time helps avoid an error trigger on the turn-off threshold caused by turn-on ringing from the synchronous MOSFET.

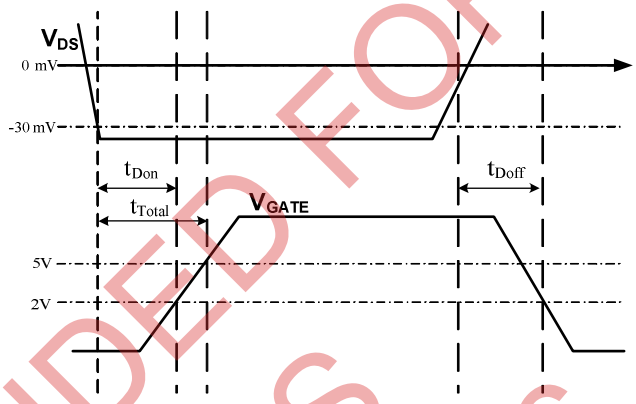


Figure 2:Turn-On and Turn-Off delay

Conducting Phase

When the synchronous MOSFET is turned on, V_{DS} rises (according to its on resistance). If V_{DS} rises above the turn-on threshold (-30mV), the control circuitry stops pulling the gate driver up. This pulls the gate driver down by internal pull-down resistance (10kΩ) to increase the on resistance, easing the rise of V_{DS}. V_{DS} is adjusted to around -30mV even if the current through the MOSFET is small. This function lowers the driver voltage when the synchronous MOSFET is turned off to cause a fast turn-off speed (which is active during turn-on blanking time). Even with a small duty, the gate driver can be turned off.

Turn-off Phase

If V_{DS} rises and triggers the turn-off threshold (0mV), the gate voltage is pulled low by the control circuitry after about 20ns turn-off delay (see Figure 2). As with the turn-on phase, a 200ns blanking time is added when the synchronous MOSFET is turned off to avoid an error trigger.

Figure 3 shows synchronous rectification operation in a heavy-load condition. Due to the high current, the gate driver initially is saturated. After V_{DS} rises above -30mV, the gate driver voltage decreases to adjust the V_{DS} (typically to -30mV).

Figure 4 shows synchronous rectification operation in a light-load condition. Due to the low current, the gate-driver voltage never saturates but decreases when the synchronous MOSFET turns on, adjusting the V_{DS}.

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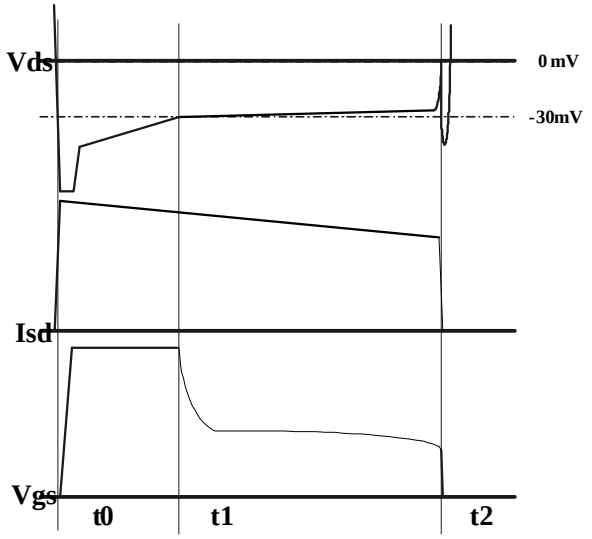


Figure 3:Synchronous Rectification Operation at Heavy Load

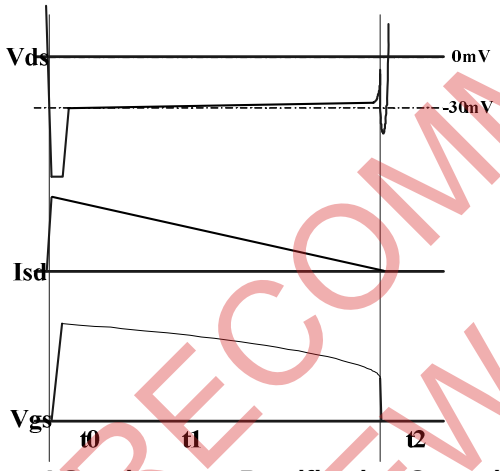


Figure 4:Synchronous Rectification Operation at Light Load

Light-Load Latch-Off Function

The MP6905 gate driver is latched. This reduces power loss in light-load conditions to improve efficiency. The light-load-enter pulse width T_{LL} is set by the resistor connected to LL. When the synchronous MOSFET conducting period is lower than T_{LL} for longer than the light-load-enter delay ($T_{LL\text{-}Delay}$), MP6905 enters light-load mode and latches off the gate driver. The synchronous MOSFET conducting period begins when the gate driver turns on until V_{GS} drops to the light-load mode, enter-pulse width threshold ($V_{LL\text{-}GS}$). During light-load mode, MP6905 monitors the synchronous MOSFET conducting period by sensing V_{DS} (when V_{DS} exceeds the light-load mode exit-pulse width threshold $V_{LL\text{-}DS}$). If it is longer than $T_{LL}+T_{LL\text{-}H}$ ($T_{LL\text{-}H}$ is light-load-enter pulse width hysteresis), the light-load mode finishes and the gate driver is unlatched to restart the synchronous rectification.

SR MOSFET Selection

To achieve higher efficiency, a MOSFET with a small $R_{DS(ON)}$ is preferred. Although a Qg is larger with a smaller $R_{DS(ON)}$, it lowers the turn-on/off speed and leads to greater power loss, including driver power loss. The MP6904 adjusts the V_{DS} to ~-30mV during the driving period when the switching current is low.

A MOSFET with low $R_{DS(ON)}$ is not recommended as the gate driver is pulled low when V_{DS}=-I_{SD}x$R_{DS(ON)}$ exceeds -50mV. This means the MOSFET's $R_{DS(ON)}$ doesn't contribute to conduction loss (P_{CON}=-V_{DS}xI_{SD}≈I_{SD}x30mV).

Figure 5 shows the typical waveform of a QR flyback: Assume a 50% duty cycle where I_{OUT} is the output current.

To efficiently utilize the MOSFET's $R_{DS(ON)}$, the MOSFET should be turned on at least 50% of the SR conduction period:

$$Vds = -Ic \times Ron = -2 \cdot I_{OUT} \times Ron \le -Vfwd$$

Where V_{DS} is the drain-source voltage, and V_{fwd} is the forward voltage threshold (~30mV).

The MOSFET's $R_{DS(ON)}$ should be no lower than ~15/I_{OUT} (mΩ).

For example, for 5A applications, the MOSFET $R_{DS(ON)}$ should be no lower than 3mΩ).

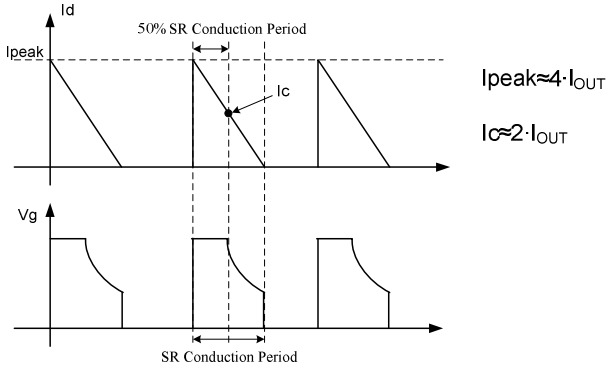


Figure 5:Synchronous Rectification typical Waveforms in QR Flyback

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Typical System Implementations

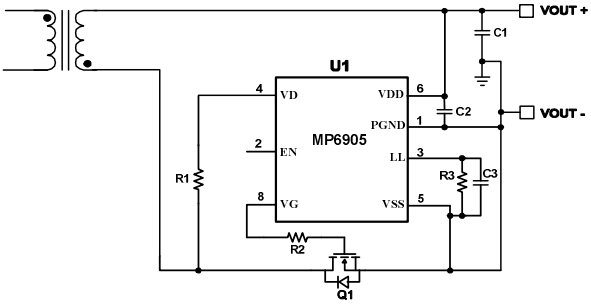


Figure 6:IC Supply derived directly from Output Voltage

Typical system implementation for the IC supply (derived from output voltage) is available in low-side rectification (see Figure 6). The output voltage should be in the V_{DD} range of 8V to 24V.

If output voltage is out of the V_{DD} range (or high-side rectification is used), use an auxiliary winding from the power transformer for the IC supply (see Figures7 and 8).

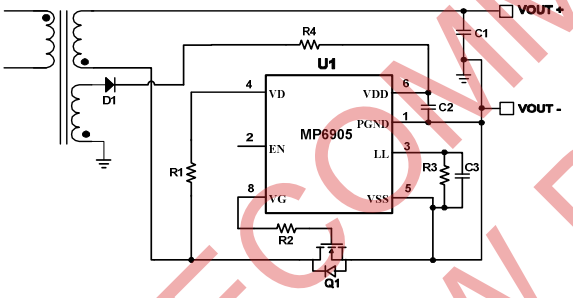


Figure 7: IC Supply Derived from Auxiliary Winding in Low-Side Rectification

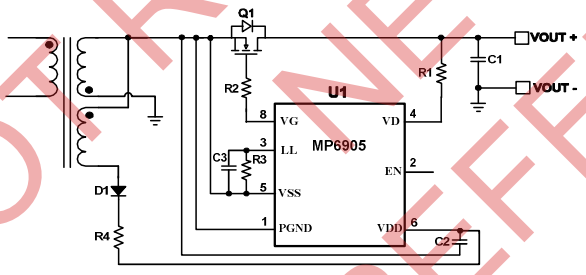


Figure 8: IC Supply Derived from Auxiliary Winding in High-Side Rectification

An additional non-auxiliary winding solution for the IC supply uses an external LDO circuit from the secondary transformer winding (see Figures 9 and 10). However, slightly higher power loss will occur, which dissipates on the LDO circuit, particularly when secondary-winding voltage is high.

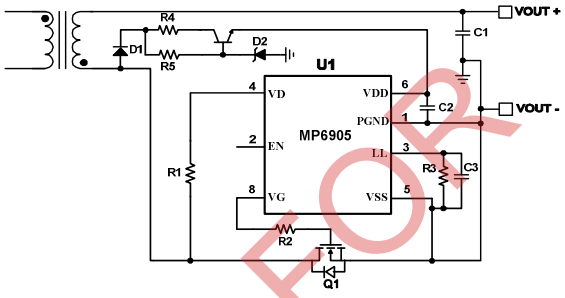


Figure 9: IC Supply Derived from Secondary Winding through External LDO in Low-Side Rectification

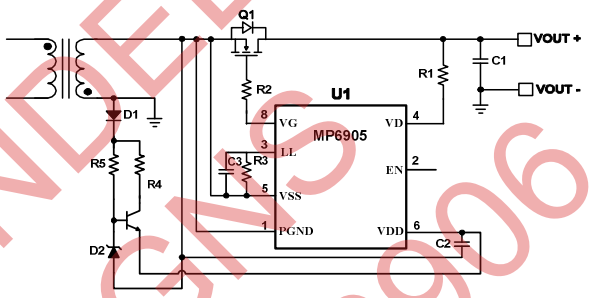


Figure 10: IC Supply Derived from Secondary Winding through External LDO in High-Side Rectification

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LAYOUT GUIDELINES

Sensing for V_D/V_{SS}

The sensing connection (V_D/V_{SS}) should be closed off to the MOSFET (drain/source). Make the sensing loop as small as possible and place the VD resistor close to the VD. Keep the IC out of the power loop to make sure the sensing loop and power loop won't interrupt each other (see Figure 11).

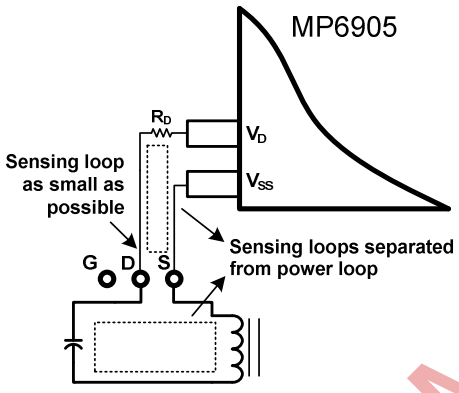


Figure 11:Voltage Sensing for V_D/V_{SS} on MP6905

Sensing for V_D/V_{SS}

A decoupling ceramic capacitor (no smaller than 1uF) from V_{DD} to PGND should be close to the IC for adequate filtering.

Gate-Driver Loop

To minimize the parasitic inductance, the gate-driver loop should be as small as possible. Keep the driver signal far away from the VD sensing trace on the layout.

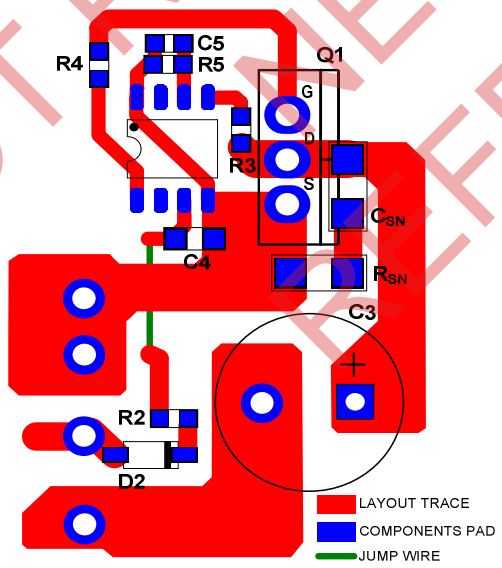


Figure 12: TO220 Package SR FET

Figure12 shows a layout example of a single layer with a through-hole transformer and TO220 package SR FET (see the application circuit on page 1). R_{SN} and C_{SN} provide the RC snubber network for the SR FET.

The sensing loop (V_D/V_{SS} to the SR FET) is minimized and separates from the power loop. The V_{DD} decoupling capacitor (C4) is placed beside the V_{DD}.

Figure 13 shows a layout example of a single layer with a PowerPAK/SO8 package SR FET, which also has a minimized sensing loop and power loop that won't interrupt each other.

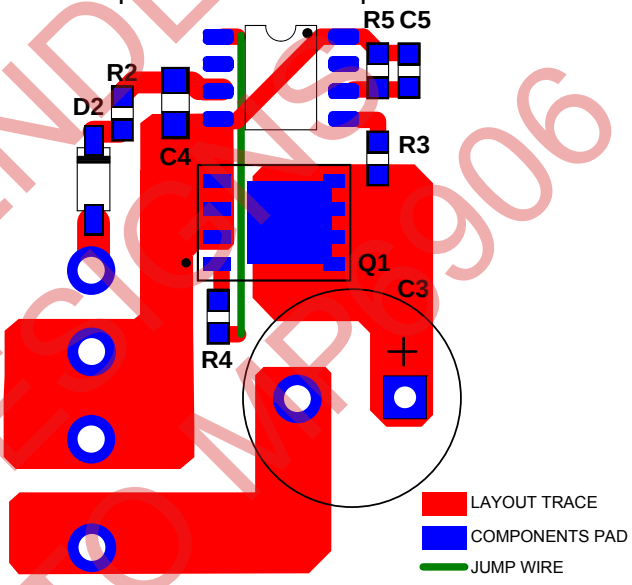


Figure 13: PowerPAK/SO8 Package SR FET

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TYPICAL APPLICATION CIRCUIT

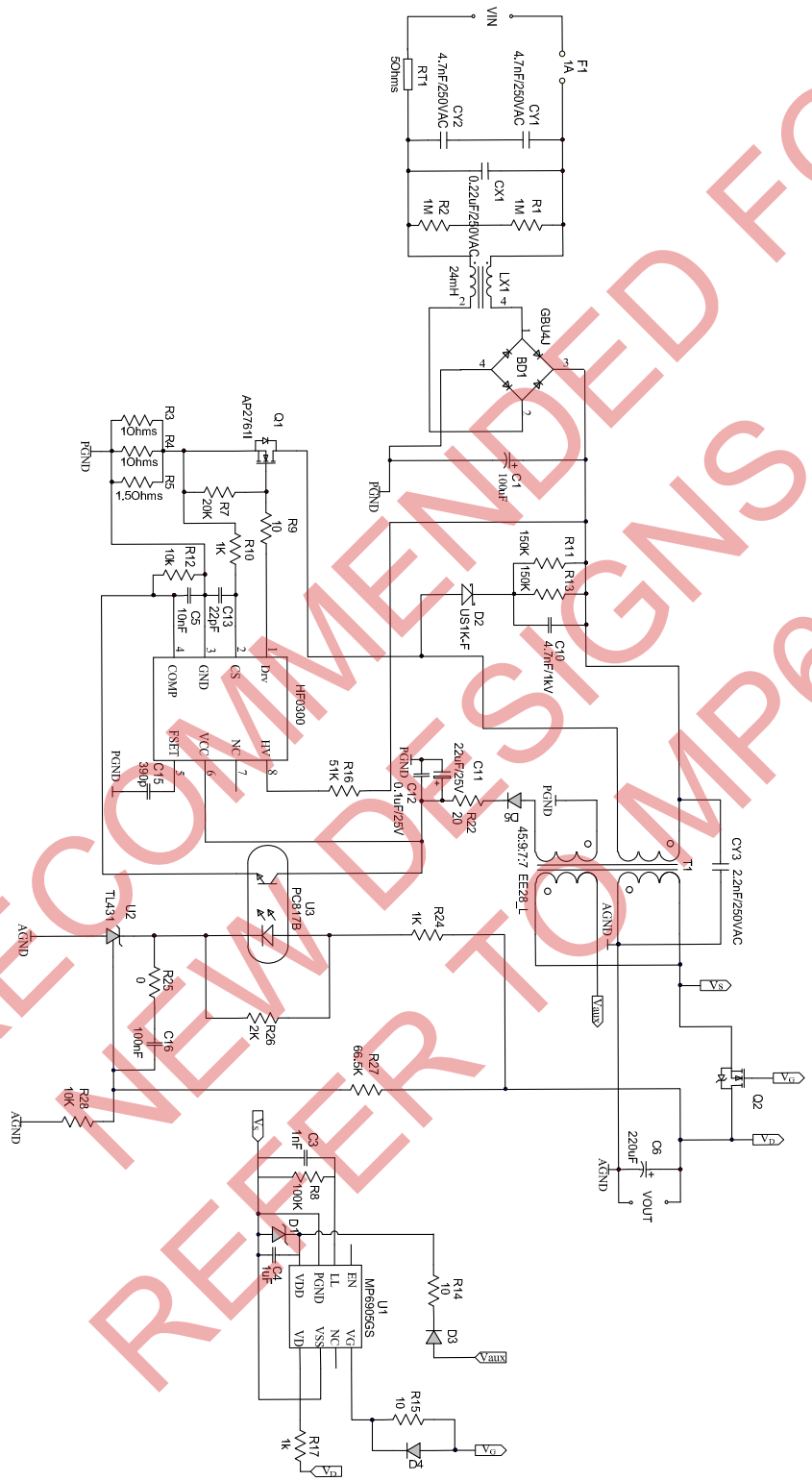
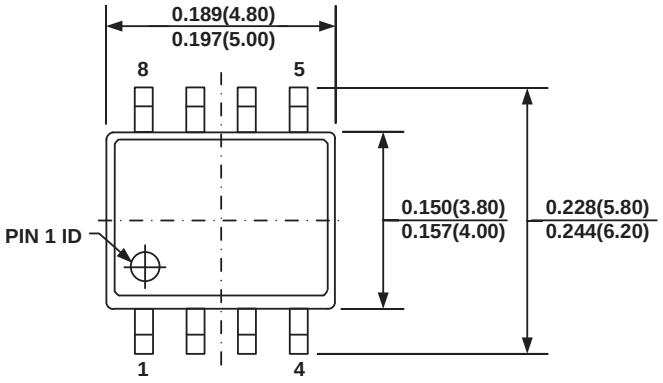


Figure 14:MP6905 for Secondary Synchronous Controller in 90W Flyback Application

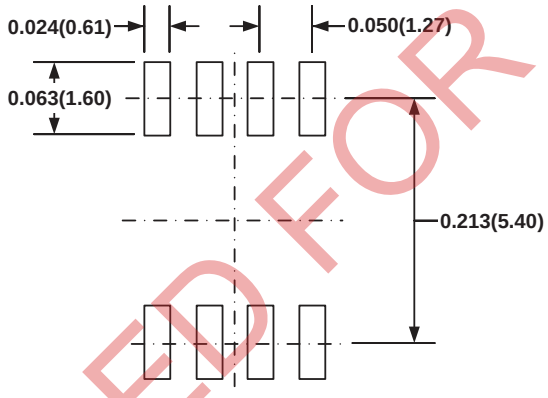
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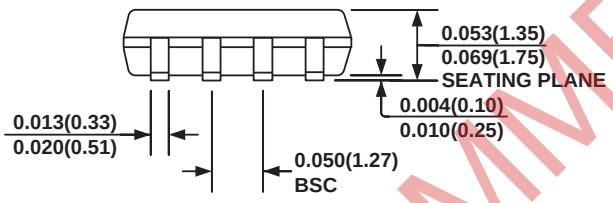
SOIC8



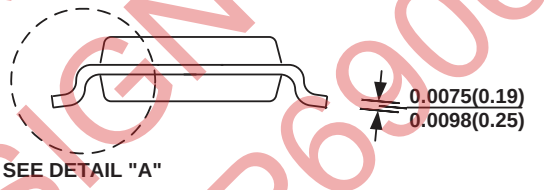
TOP VIEW



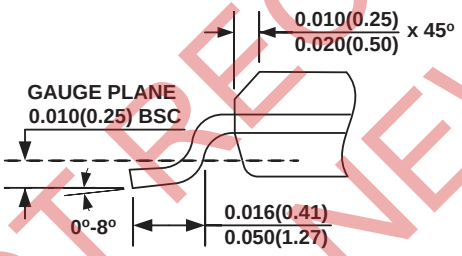
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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