MP6536

26V, 5.5A 3-Channel Half-Bridge Driver

The Future of Analog IC Technology

DESCRIPTION

The MP6536 is a 3-channel half-bridge driver IC intended to drive a 3-phase brushless DC motor.

The MP6536 features a low-current shutdown mode, standby mode, input under-voltage protection, current limit, thermal shutdown, and fault flag signal output. All channels of the drivers interface with standard logic signals.

The MP6536 is available in a 40 lead QFN 5mmx5mm package.

FEATURES

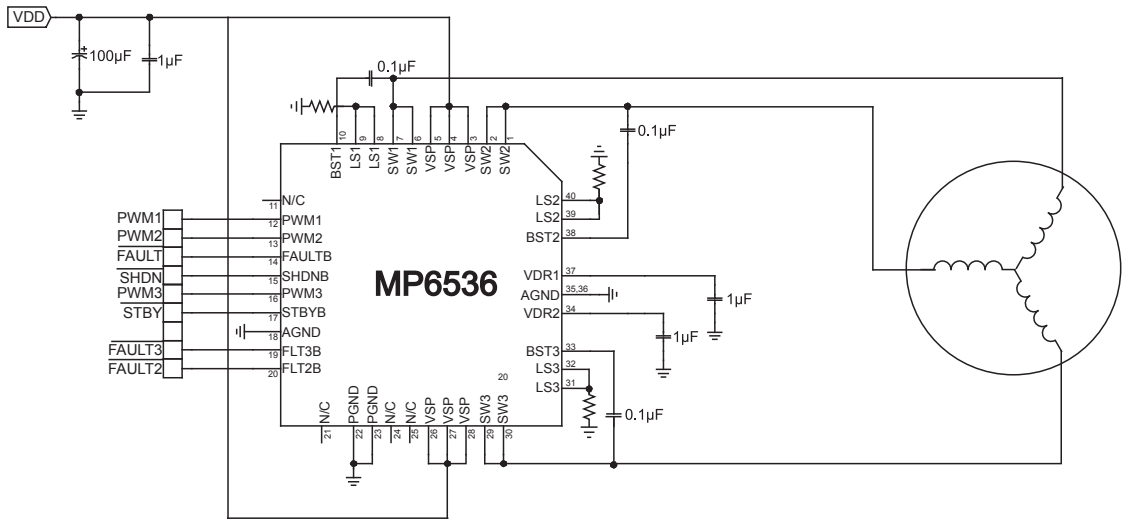
- 5V to 26V VDD
- ±5.5A Peak Current Output
- Up to 1MHz PWM Frequency
- Protected Integrated Power 0.14Ω Switches
- 10ns Switch Dead Time
- All Switches Current Limited
- Internal Under-Voltage Protection
- Internal Thermal Protection
- Short-Circuit Protection
- Fault Output Flag

APPLICATIONS

- 3-Phase BLDC Motor Drive

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6536DU	QFN-40 (5mmx5mm)	See Below

* For Tape & Reel, add suffix –Z (e.g. MP6536DU–Z);

For RoHS, compliant packaging, add suffix –LF (e.g. MP6536DU–LF–Z).

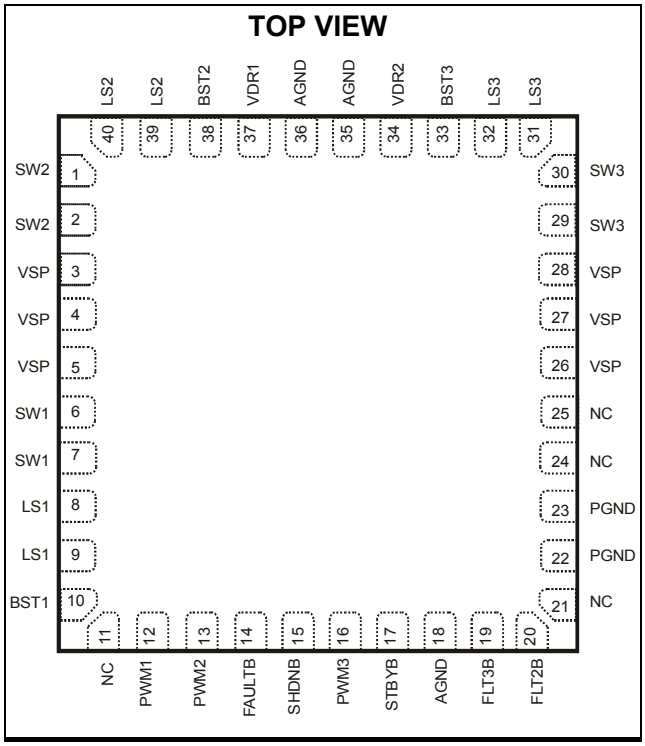
TOP MARKING

MPSYYWW
MP6536
LLLLLLL

MPS: MPS Prefix:
YY: Year Code;
WW: Week Code:
MP6536: Part Number;
LLLLLLL: Lot number;

PACKAGE REFERENCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (1)

VSP Supply Voltage 28V
SWx Voltage ..... -0.3V to V_{DD} + 0.3V
BSTx to SWx..... -0.3V to +6V
Voltage at All Other Pins..... -0.3V to +6V
Continuous Power Dissipation.. (T_A = +25°C) (2)
…… ...4.2W
Storage Temperature.....-55°C to +150°C
Junction Temperature..... 150°C
Lead Temperature ..... 260°C

Recommended Operating Conditions (3)

VSP Supply Voltage ..... 5V to 26V
Operating Junction Temp. (T_J) .-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-40 (5mmx5mm)	36	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{SP} = 12V, V_{SHDNB} = 5V, T_A = +25°C, unless otherwise specified.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VSP Operating Current		I_{LOAD} = 0A，PWMx=0		2.2	3.5	mA
VSP Shutdown Current		V_{SHDN} = 0V		24	30	μA
Operating VSP Threshold Low			3.7	4		V
Operating VSP Threshold High				4.4	4.8	V
STBYB Threshold Low			0.8	1.0		V
STBYB Threshold High				1.6	1.8	V
PWM Input Bias Current				0.1	1.0	μA
SHDNB Threshold Low			0.8	1.0		V
SHDNB Threshold High				1.6	1.8	V
PWMx Threshold Low			0.8	1		V
PWMx Threshold High				1.6	1.8	V
SWx On Resistance (5)		V_{SP} = 7V, High-Side and Low-Side		0.14		Ω
SWx Current Limit (5)		V_{PWM} = 0V, Sinking		5.5		A
		V_{PWM} = 5V, Sourcing		5.5		A
SWx Switching Frequency		V_{PWM} = 0 to 5V, 50% Duty Cycle			1	MHz
BST Voltage UVLO		Falling Value		2.2		V
BST Current		High-Side MOSFET On, V_{BST}-V_{SW}=5.5V		30		μA
SWx Rise/Fall Time (5)		V_{PWM} = 0V to 5V		5		ns
Minimum PWM Pulse Width		V_{PWM} = 0V to 5V, High or Low Pulse		30		ns
Dead Time (5)		I_{OUT}= ±100mA		10		ns
PWMx to SWx Delay Time Rising		V_{PWM} = 0V to 5V		30		ns
PWMx to SWx Delay Time Falling		V_{PWM} = 5V to 0V		30		ns
Thermal Shutdown Temperature (5)		T_J Rising		160		°C
Thermal Shutdown Hysteresis				35		°C

Notes:

5) Not production tested.

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PIN FUNCTIONS

Pin #	Name	Description
1,2	SW2	**Output 2**. SW2 is valid approximately 100μs after VSP goes high.
3,4,5	VSP	**Power Supply Input**. Connect VSP to the positive side of the input power supply. Bypass VSP to PGND as close to the IC as possible.
6,7	SW1	**Output 1**. SW1 is valid approximately 100μs after VSP goes high.
8,9	LS1	**Low-Side Source Connection of SW1.**
10	BST1	**Bootstrap Supply**. BST1 powers the high-side gate of the SW1 stage. Connect a capacitor (0.1μF or greater) between BST1 and SW1.
11	NC	**No Connection**. NC MUST be kept floating.
12	PWM1	**Driver Logic Input 1**. Drive PWM1 with the signal that controls SW1. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
13	PWM2	**Driver Logic Input 2**. Drive PWM2 with the signal that controls SW2. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
14	FAULTB	**Fault Output.** A low output at $\overline{\text{FAULT}}$ indicates that the MP6536 has detected an over-temperature, over-current, or under-voltage condition. FAULTB is an open-drain output.
15	SHDNB	**Shutdown Input**. When SHDNB is low, the IC shuts off.
16	PWM3	**Driver Logic Input 3.** Drive PWM3 with the signal that controls SW3. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
17	STBYB	**Standby Input.** Default low (internal pull-down). If driven high, the output of the driver is determined by PWM1/2/3. If driven low, all outputs are high impedance.
18	AGND	**Analog Ground.**
19	FLT3B	**Fault Monitor.** For details see the “Fault Output” section. FLT3B is an open-drain output.
20	FLT2B	**Fault Monitor.** For details see the “Fault Output” section. FLT2B is an open-drain output.
21	NC	**No Connection**. NC MUST be kept floating.
22, 23	PGND	**Power Ground**. Connect the exposed pad on the bottom side to ground plane.
24, 25	NC	**No Connection**. NC MUST be kept floating.
26,27, 28	VSP	**Power Supply Input**. Connect VSP to the positive side of the input power supply. Bypass VSP to PGND as close to the IC as possible.
29, 30	SW3	**Output 3.** SW3 is valid approximately 100μs after VSP goes high.

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PIN FUNCTIONS *(continued)*

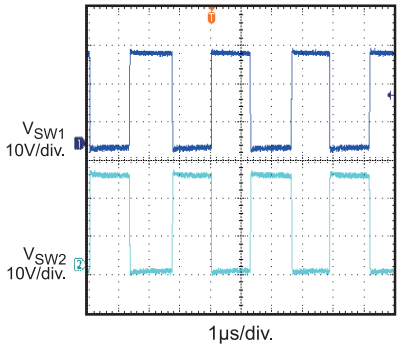
Pin #	Name	Description
31, 32	LS3	**Low-Side Source Connection of SW3.**
33	BST3	**Bootstrap Supply.** BST3 powers the high-side gate of the SW3 stage. Connect a capacitor (0.1μF or greater) between BST3 and SW3.
34	VDR2	**Gate Drive Supply Bypass.** The voltage at VDR2 is supplied from an internal regulator from VSP. VDR2 powers the internal circuitry and internal MOSFET gate drive for the SW3 output stage. Bypass VDR2 to PGND with a 0.1μF to 10μF capacitor.
35, 36	AGND	**Analog Ground.**
37	VDR1	**Gate Drive Supply Bypass.** The voltage at VDR1 is supplied from an internal regulator from VSP. VDR1 powers the internal circuitry and internal MOSFET gate drive for the SW1 and SW2 output stages. Bypass VDR1 to PGND with a 0.1μF to 10μF capacitor.
38	BST2	**Bootstrap Supply.** BST2 powers the high-side gate of the SW2 stage. Connect a capacitor (0.1μF or greater) between BST2 and SW2.
39,40	LS2	**Low-Side Source Connection of the SW2.**

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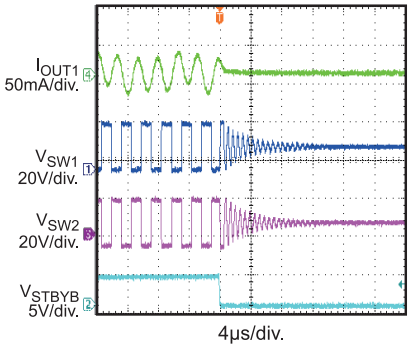
TYPICAL PERFORMANCE CHARACTERISTICS

V_{SP} = 24V, V_{SHDNB} = 5V, R_{LOAD} = 8Ω, T_A = +25ºC, unless otherwise noted.

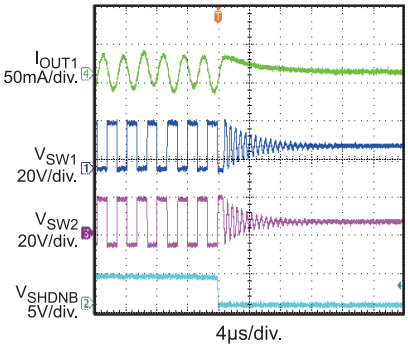
Normal Switch Waveform



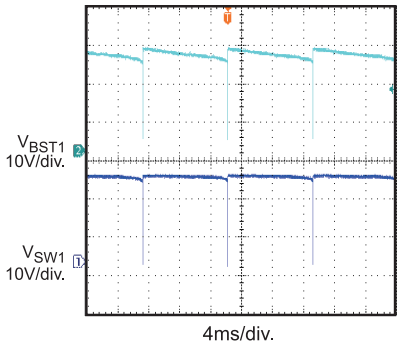
Standby



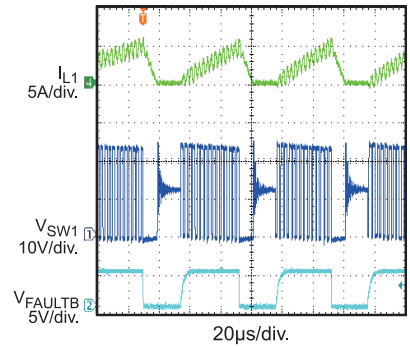
Shutdown



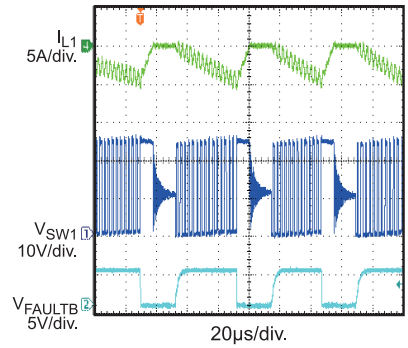
BS Re-Charge Cycling



Short-Circuit Positive Current



Short-Circuit Negative Current



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BLOCK DIAGRAM

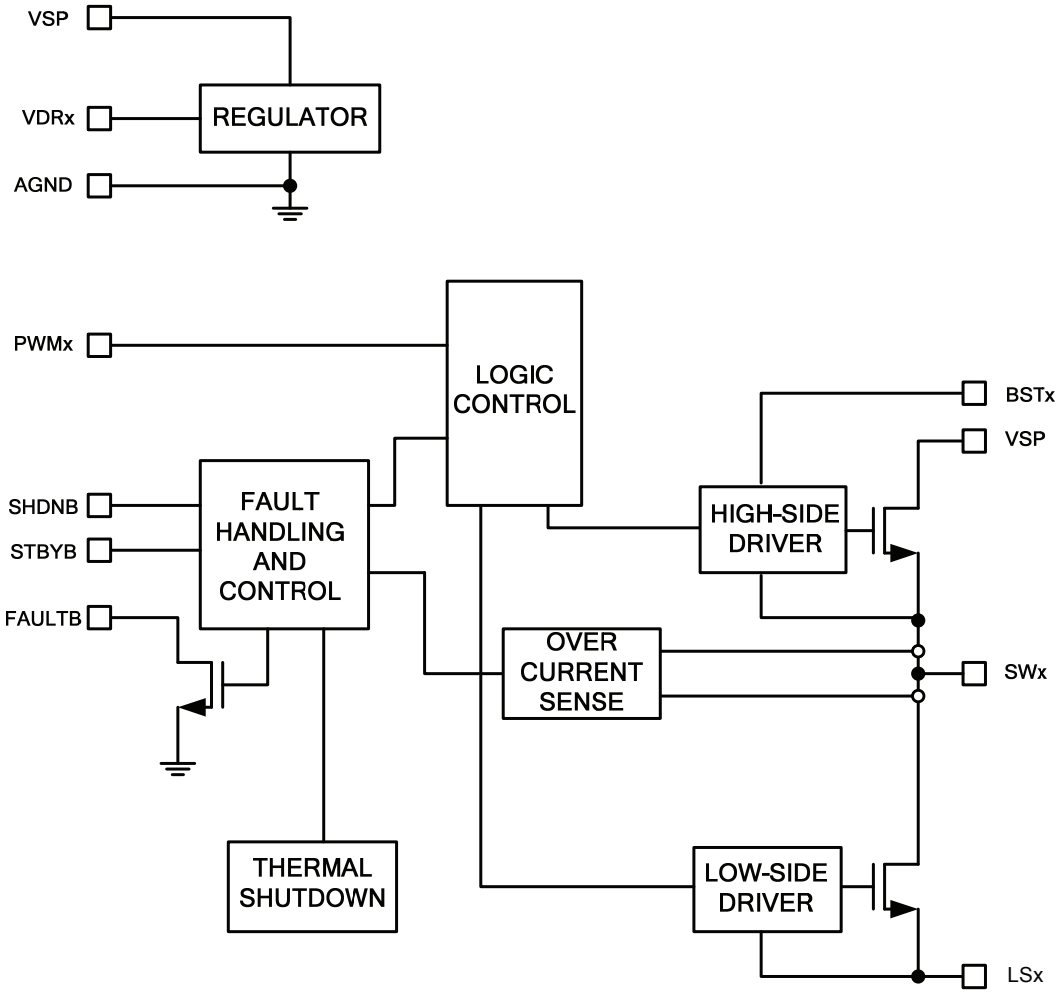


FIGURE 1. Function Block Diagram (1 Half-Bridge Channel Only)

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OPERATION

The MP6536 is a 3-channel half-bridge driver intended to drive a brushless DC motor. The output is in phase with the input, and the dead time is optimized for symmetrical performance, regardless of load conditions.

When SHDN is low, all channels are off. When STBYB is pulled low, it causes the outputs of all the channels to go into high impedance. However, when the voltage across BST1/2/3 and SW1/2/3 drops low significantly, the bottom MOSFET is turned on to refresh the external bootstrap capacitor. Connecting a capacitor (0.1μF or greater) between BST and SW (as the bootstrap capacitor) is recommended.

In order to prevent erratic operation, two under-voltage lockout (UVLO) circuits are used. One ensures that the supply for the bottom gate drive circuit is sufficiently high, and the other is for the top gate driver.

Fault Protection

To protect the power MOSFETs, an internal current limit of 5.5A is set for all MOSFETs. When this limit is reached, all MOSFETs of the over-current bridge channel will go into high impedance for a fixed duration (30μs approximately) before resuming normal operation.

Thermal monitoring is integrated into the MP6536. If the die temperature rises above 160ºC, all switches are turned off. The temperature must fall below 125ºC before normal operation resumes.

To enhance the robustness of the device under a short-circuit condition, a capacitor can be connected to FAULTB (see Fig. 2). The time constant of the RC must be greater than 50ms for the FAULTB node to reach 2V. Under a short-circuit condition, the FAULTB node re-sets to zero, and the part is placed in standby mode until the voltage at STBYB is above 2V.

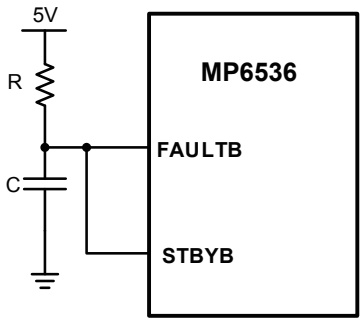


FIGURE 2. Fault Protection Enhancement Circuit

Fault Output

The MP6536 includes an open drain, active-low fault indicator output (FAULTB). A fault is indicated if one of the following conditions is detected:

1. The current limit is tripped.
2. Thermal shutdown is tripped.

A fault on any channel causes FAULTB to pull low. Once the fault is removed, the MP6536 resumes normal operation.

Do not apply more than 6V to FAULTB.

Error Reporting

The MP6536 has two fault monitor pins (FLT3B and FLT2B), which are active low open-drain outputs. They provide protection-mode signaling to a PWM controller or another system control device (see Table 1).

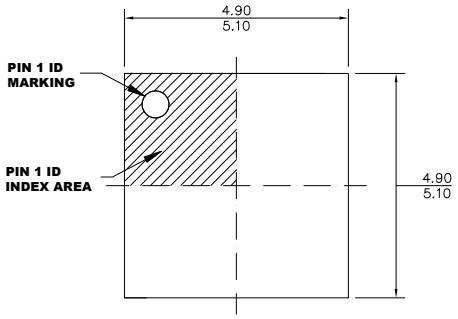
TABLE 1. Fault Output Logic

OCP	OTP	UVP	FLTB2	FLTB3
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
1	0	0	0	0

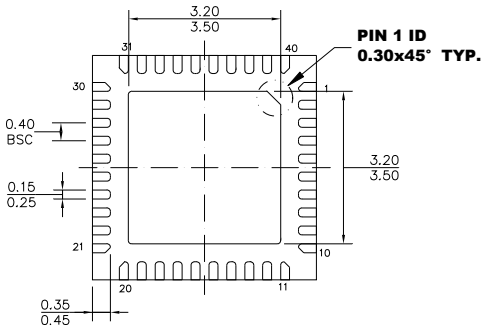
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PACKAGE INFORMATION

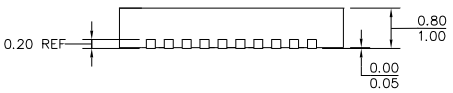
QFN-40 (5x5mm)



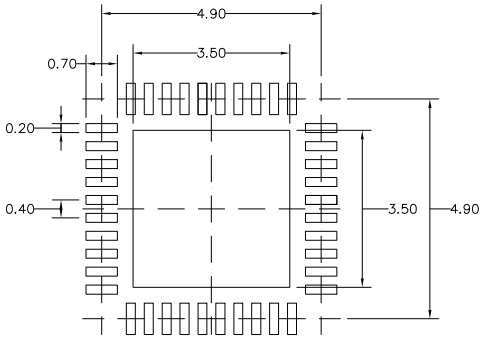
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHE-1
5) DRAWING IS NOT TO SCALE.

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