MP6520

8V to 32V, 1.5A, Stepper Motor Driver with Integrated MOSFETs

DESCRIPTION

The MP6520 is a stepper motor driver with a built-in microstepping translator. The MP6520 operates from a supply voltage of up to 32V and can deliver a motor current of up to 1.5A. The MP6520 can operate a bipolar stepper motor in full-, half-, quarter-, and eighth-step modes.

The MP6520 has a fixed 3.3V reference output, which allows it to operate without a separate logic power supply.

Full protection features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown.

The MP6520 is available in a QFN-28 (4mmx5mm) package with an exposed thermal pad.

FEATURES

- Wide 8V to 32V Input Voltage Range
- Two Internal Full-Bridge Drivers
- Low On Resistance (HS: 300mΩ; LS: 300mΩ)
- No Control Power Supply Required
- Simple Logic Interface
- Compatible with 3.3V and 5V Logic
- Full-, Half-, Quarter-, and Eighth-Step Functionality
- 1.5A Maximum Output Current
- Adjustable Mixed Decay Ratio
- Over-Current Protection (OCP)
- Input Over-Voltage Protection (OVP) Function
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in a QFN-28 (4mmx5mm) Package

APPLICATIONS

- Bipolar Stepper Motors
- Printers

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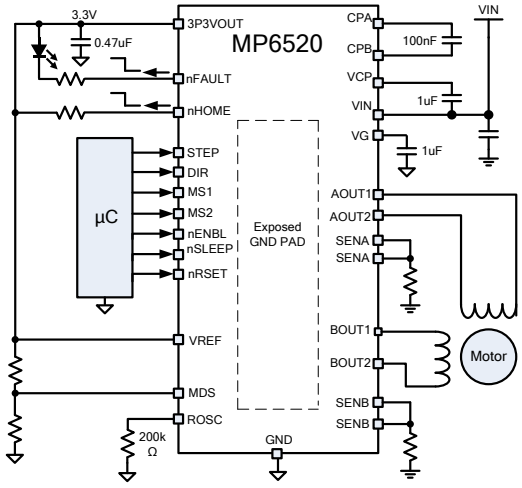
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6520GV	QFN-28 (4mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6520GV–Z)

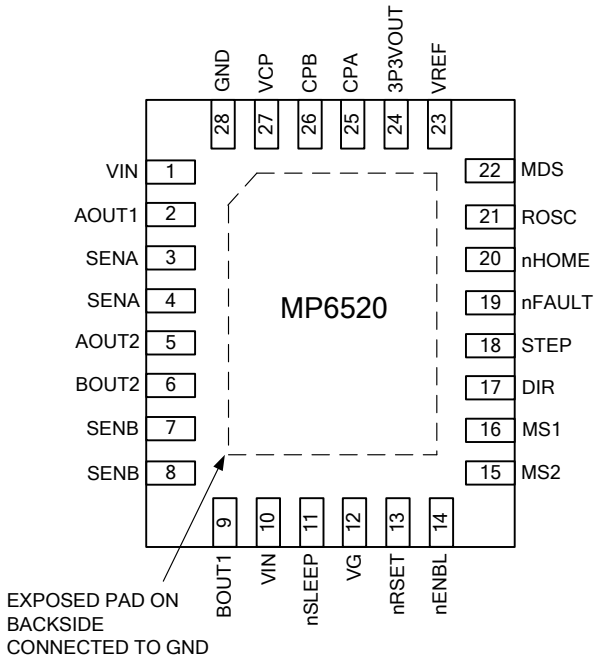
TOP MARKING

MPSYWW
MP6520
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6520: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-28 (4mmx5mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) ..... -0.3V to 40V
xOUTx voltage ($V_{A/BOUT1/2}$) ..... -0.7V to 40V
VCP, CPB ..... VIN to VIN + 6.5V
ESD rating (HBD) 2kV
SENA, SENB 700mV
All other pins to AGND (except for 3P3VOUT and VG) ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2) 3.1W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 8V to 32V
Output current ($I_{A,BOUT}$) ..... ±1.5A
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-28 (4mmx5mm)	40	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN = 24V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		8	24	32	V
Quiescent current	I_Q	VIN = 24V, nENBL = 0, nSLEEP = 1, with no load		7	10	mA
	I_{SLEEP}	VIN = 24V, nSLEEP = 0			5	µA
Voltage Regulator						
3P3VOUT reference output	V_{3P3}	I_{OUT} = 1mA	3.2	3.3	3.45	V
Internal MOSFETs						
Output on resistance	R_{HS}	VIN = 24V, I_{OUT} = 1A, T_J = 25°C		0.30	0.35	Ω
		VIN = 24V, I_{OUT} = 1A, T_J = 85°C		0.32		Ω
	R_{LS}	VIN = 24V, I_{OUT} = 1A, T_J = 25°C		0.30	0.35	Ω
		VIN = 24V, I_{OUT} = 1A, T_J = 85°C		0.32		Ω
Body diode forward voltage	V_F	I_{OUT} = 1.5A			1.3	V
Control Logic						
Input logic low threshold	V_{IL}	All logic pins			0.6	V
Input logic high threshold	V_{IH}	All logic pins	2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-25		25	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-8		8	µA
Internal pull-down resistance	R_{PD}	All logic pins		530		kΩ
Home, nFault Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_O = 5mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	µA
Protection Circuit						
UVLO rising threshold	V_{IN_RISE}		6.5	7	7.7	V
UVLO hysteresis (5)	V_{HYS}			970		mV
Input OVP threshold	V_{OVP}		36	37.9	40	V
Input OVP hysteresis	ΔV_{OVP}			600		mV
Over-current trip level	I_{OCP1}	Sinking	2.5	5.5		A
	I_{OCP2}	Sourcing	2.5	5.5		A
Over-current deglitch time (5)	t_{OCP}			1		µs
Thermal shutdown (5)	T_{TSD}			165		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			30		°C
Current Control						
Constant off time	t_{OFF}	R_t = 200kΩ	20	30	40	µs
Blanking time	t_{BLANK}			2		µs
Crossover dead time	t_{DT}	HS off to LS on, or LS off to HS on		400		ns
VREF input current	I_{REF}	V_{REF} = 3.3V			3.5	µA
SENx trip voltage	V_{TRIP}	V_{REF} = 3.3V, 100% (no switch in test mode)	600	645	700	mV
Current trip accuracy	ΔI_{TRIP}	V_{REF} = 3.3V, 70% - 100%	-5		5	%
		V_{REF} = 3.3V, 38% - 64%	-10		10	%
		V_{REF} = 3.3V, 19% - 30%	-15		15	%
		V_{REF} = 3.3V, <10%	-20		20	%
Charge pump frequency	f_{CP}			525		kHz

NOTE:

5) Not tested in production.

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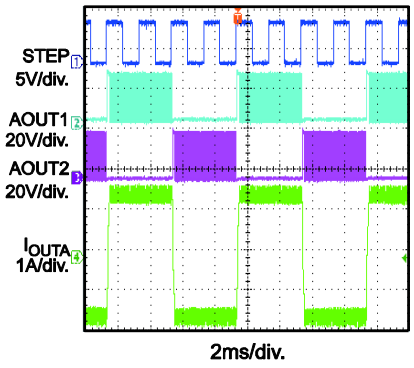
TYPICAL PERFORMANCE CHARACTERISTICS

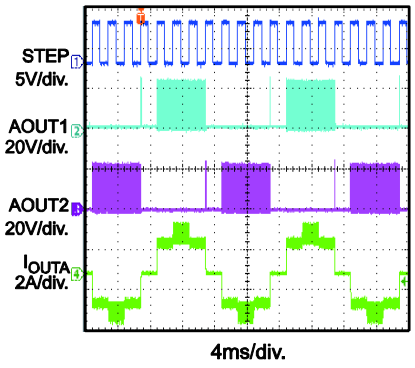
VIN = 24V, I_{OUT} = 1.5A, T_A = 25°C, F_{STEP} = 500Hz, resistor + inductor load: R = 3.3Ω, L = 1.5mH/channel, automatic decay, unless otherwise noted.

Steady State-Full Step

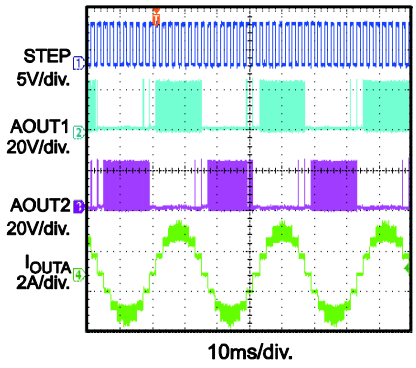
I_{OUT} = 1.8A



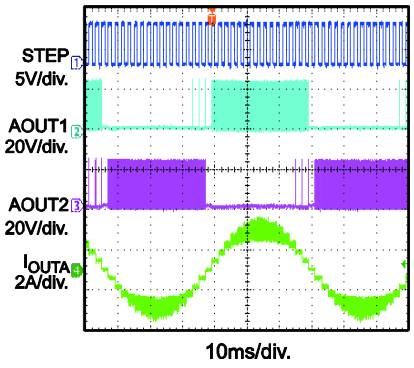
Steady State-Half Step



Steady State-Quarter Step

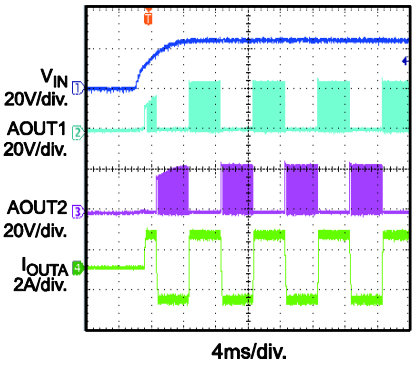


Steady State-Eighth Step

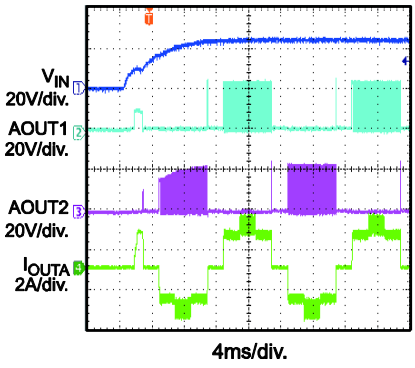


Power Ramp Up-Full Step

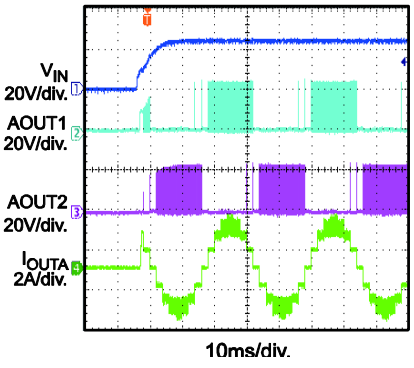
I_{OUT} = 1.8A



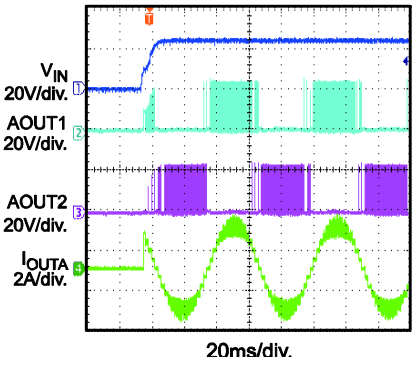
Power Ramp Up-Half Step



Power Ramp Up-Quarter Step

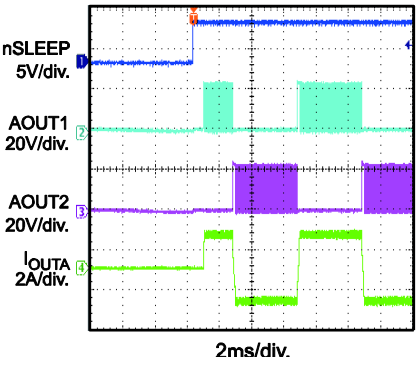


Power Ramp Up-Eighth Step



Sleep Recovery-Full Step

I_{OUT} = 1.8A



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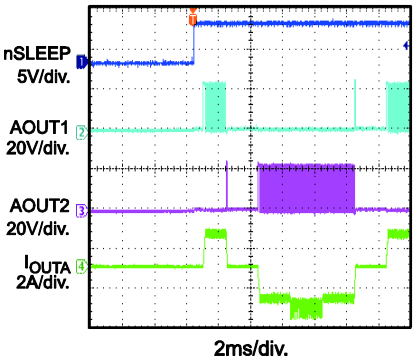
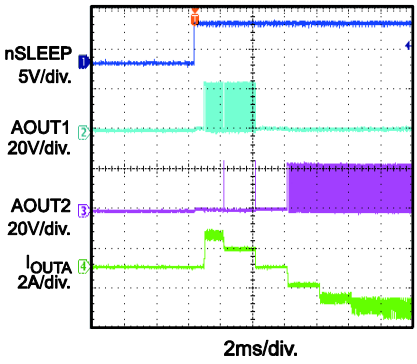
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 24V, I_{OUT} = 1.5A, T_A = 25°C, F_{STEP} = 500Hz, resistor + inductor load: R = 3.3Ω, L = 1.5mH/channel, automatic decay, unless otherwise noted.

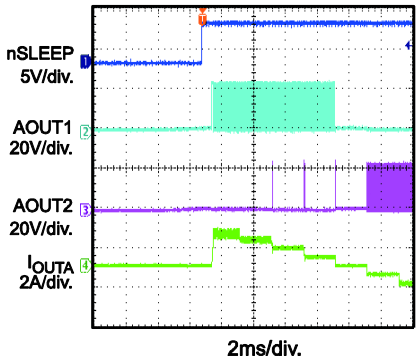
Sleep Recovery-Half Step



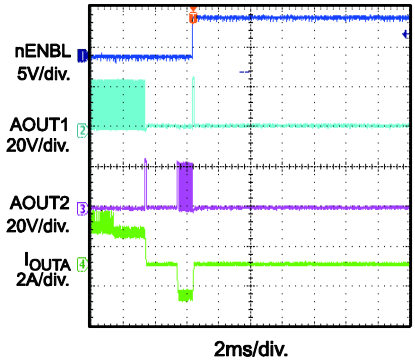
Sleep Recovery-Quarter Step



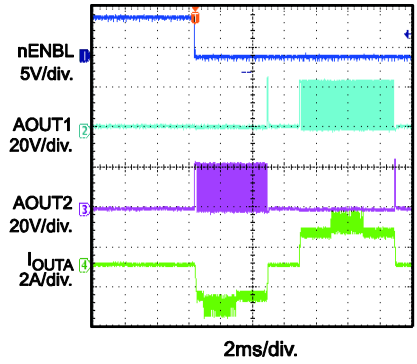
Sleep Recovery-Eighth Step



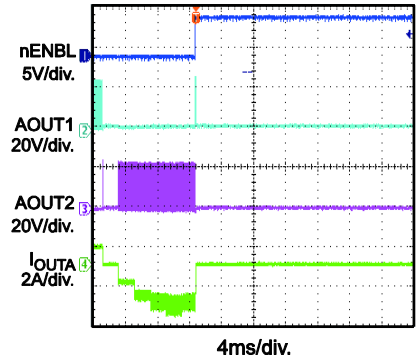
Disable-Half Step



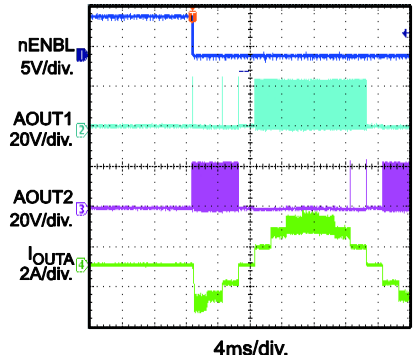
Enable-Half Step



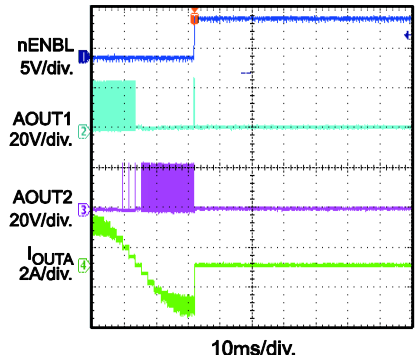
Disable-Quarter Step



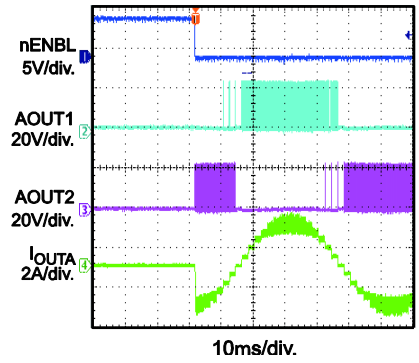
Enable-Quarter Step



Disable-Eighth Step



Enable-Eighth Step



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PIN FUNCTIONS

Pin #	Name	Description
1, 10	VIN	**Input supply voltage.** Both VIN pins must be connected to the same supply.
2	AOUT1	**Bridge A output terminal 1.**
3, 4	SENA	**Bridge A sense resistor connector.** Connect SENA to the current sensor resistor for bridge A.
5	AOUT2	**Bridge A output terminal 2.**
6	BOUT2	**Bridge B output terminal 2.**
7, 8	SENB	**Bridge B sense resistor connector.** Connect SENB to the current sensor resistor for bridge B.
9	BOUT1	**Bridge B output terminal 1.**
11	nSLEEP	**Sleep mode input.** Drive nSLEEP logic low to enter low-power sleep mode; drive nSLEEP logic high for normal operation. nSLEEP has an internal pull-down resistor.
12	VG	**Gate drive regulator output.** Bypass VG to GND with a 1µF, 16V ceramic capacitor.
13	nRSET	**Reset input.** Drive nRSET logic low to initialize the translator and reset internal logic; drive nRSET logic high for normal operation. nRSET has an internal pull-down resistor.
14	nENBL	**Enable input.** Drive nENBL logic high to disable the bridge outputs and translator operation; drive nENBL logic low to enable outputs and translator. nENBL has an internal pull-down resistor.
15	MS2	**Mode select.** MS1 and MS2 set the step mode to full-, half-, quarter-, or eighth-step. MS1 and MS2 have internal pull-down resistors. See the Microstep Selection section on page 10 for more details.
16	MS1	
17	DIR	**Direction input.** The logic level applied to DIR sets the direction of motor rotation. DIR has an internal pull-down resistor.
18	STEP	**Step input.** A rising edge on STEP sequences the translator and advances the motor by one increment. Internal pull-down resistor.
19	nFAULT	**Fault indication output.** nFAULT is driven low when a fault condition (OCP, OVP, OTS) occurs. nFAULT is an open-drain output. If used, it requires an external pullup resistor.
20	nHOME	**Home position output.** nHOME is driven low when the indexer is at the home position in the step table. nHOME is an open-drain output. If used, it requires an external pull-up resistor.
21	ROSC	**Constant off-time setting input.** A resistor from ROSC to GND sets the PWM off time.
22	MDS	**Mixed decay setting.** The voltage applied to the MDS input pin sets the PWM decay mode. See the Decay Modes section on page 10 for details.
23	VREF	**Reference voltage input.** The voltage applied to the VREF input in conjunction with the current sense resistance defines the current through the motor. VREF can be connected to 3P3VOUT.
24	3P3VOUT	**3.3V regulator output.** 3P3VOUT is a 3.3V regulator output. Decouple 3P3VOUT with a 0.47µF, 6.3V ceramic capacitor to GND.
25	CPA	**Charge pump capacitor.** Connect a 100nF ceramic capacitor between CPA and CPB. The capacitor must be rated for at least the voltage applied to VIN.
26	CPB	
27	VCP	**Charge pump output.** VCP requires a 1µF, 16V ceramic capacitor to VIN.
28, PAD	GND	**Ground.** Connect both GND and the exposed pad to ground directly.

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BLOCK DIAGRAM

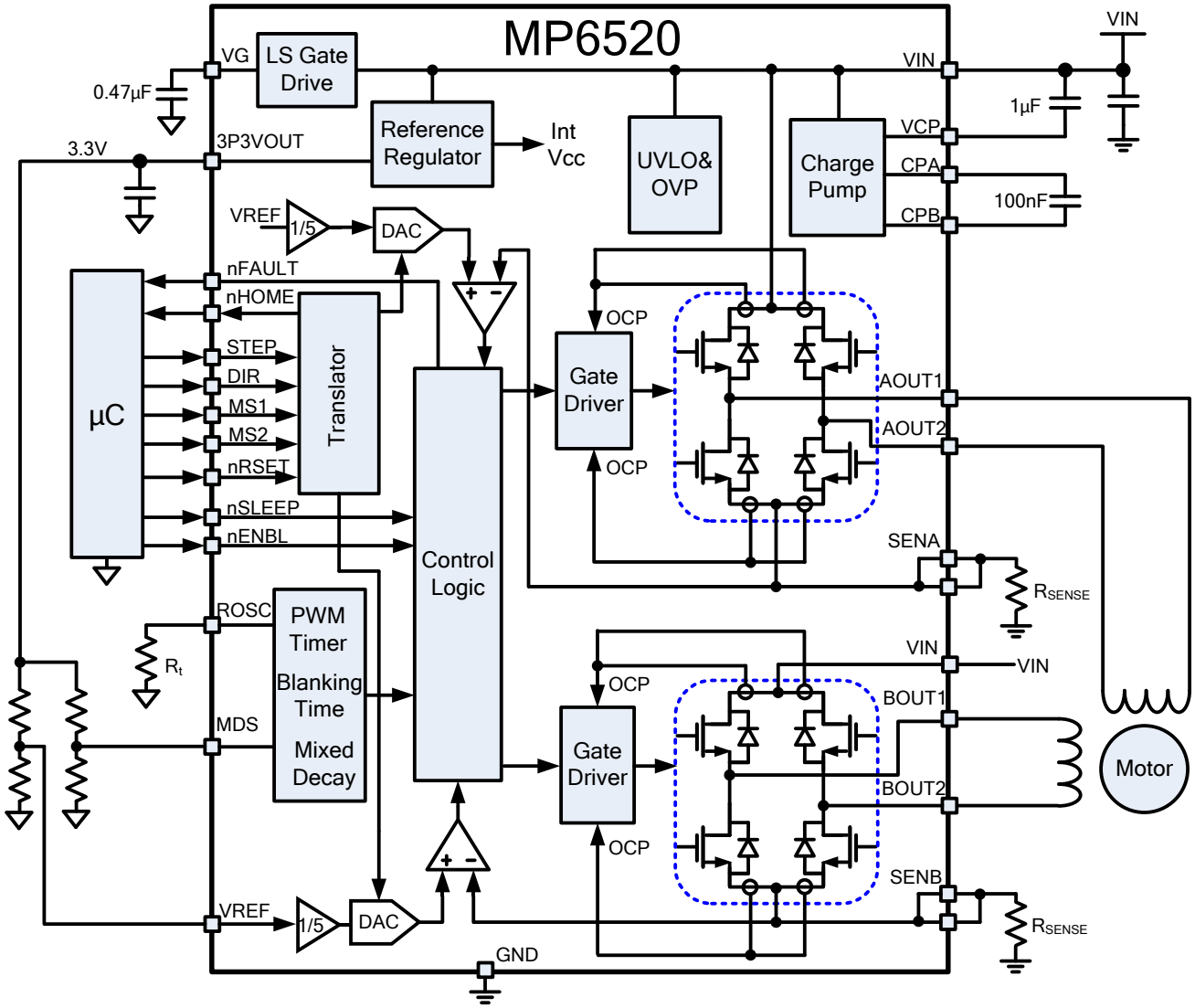

Figure 1: Functional Block Diagram

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OPERATION

The MP6520 is a bipolar stepper motor driver that integrates eight N-channel power MOSFETs arranged as two full bridges with translator logic to drive a bipolar stepper motor. It can supply up to 1.5A of current over a wide 8V to 32V input voltage range. The MP6520 is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. The current in each of the two output bridges is regulated with programmable, constant off-time pulse-width modulation (PWM) control circuitry. At each step, the current for each full bridge is set by the value of its external current sense resistor, a reference voltage (V_{REF}), and the output voltage of its DAC, which is controlled by the output of the translator.

Stepping

The motor moves step-by-step by applying a series of pulses to STEP. A rising edge on the STEP input sequences the translator one increment in the direction set by the level of the DIR input. The translator controls the input to the DACs and the direction of current flow in each winding. The amplitude of the increment is determined by the state of the inputs MS1 and MS2 (see Table 2).

Figure 2 and Table 1 show the timing requirements of the STEP, DIR, MS1, and MS2 inputs.

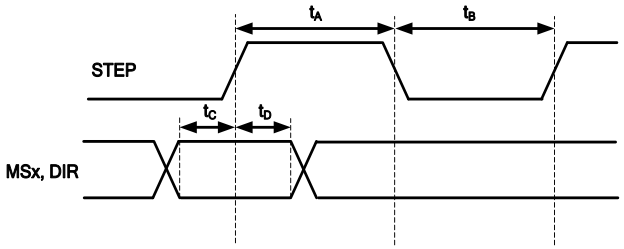

Figure 2: Input Logic Timing

Table 1: Input Logic Timing

Time Duration	Symbol	Typ.	Unit
Step minimum high pulse width	t_A	1	µs
Step minimum low pulse width	t_B	1	µs
Set-up time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

The motor winding currents are regulated by a programmable, constant-off-time, PWM, current control circuit, which operates as follows:

1. Initially, a diagonal pair of MOSFETs turns on so current can flow through the motor winding.
2. The current increases in the motor winding, which is sensed by an external sense resistor (R_{SENSE}). During the initial blanking time (t_{BLANK}), the high-side MOSFET always turns on regardless of current limit detection.
3. When the voltage across R_{SENSE} reaches the current regulation threshold, the internal current comparator either shuts off the high-side MOSFET so the winding inductance current freewheels through the two low-side MOSFETs (slow decay), or turns on the opposite diagonal pair of MOSFETs so the current flows back to the input (fast decay).
4. The current continues decreasing for the constant off-time.
5. The cycle repeats.

The constant off-time (t_{off}) is determined by the selection of an external resistor (R_t) which can be approximated with Equation (1):

$$t_{OFF}(ns) = 190 \times R_t(k\Omega) \quad (1)$$

The full-scale (100%) current limit threshold can be calculated with Equation (2):

$$I_{Max-LIMIT} = \frac{V_{REF}}{5 \times R_{SENSE}} \quad (2)$$

The DAC output reduces the V_{REF} output to the current sense comparator in precise steps. The current at any given step ($I_{Trip-LIMIT}$) can be calculated with Equation (3):

$$I_{Trip-LIMIT} = \%I_{Trip-LIMIT} I_{Max-LIMIT} \quad (3)$$

See Table 3 for $\%I_{Trip-LIMIT}$ at each step.

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Microstep Selection (MS1, MS2)

The step mode is selected by applying logic-high and -low voltages to the MS1 and MS2 input pins. The MP6520 supports full-, half-, quarter-, and eighth-step modes.

Full-step has four states with each motor winding driven with either 70.7% maximum positive current or 70.7% maximum negative current. This provides four steps per electrical rotation. Half-step provides eight steps per electrical rotation; quarter-step provides 16 steps per electrical rotation; eighth-step provides 32 steps per electrical rotation. Refer to Table 3 and Figure 3 for details.

Table 2 shows step modes selected for different settings of the MS1 and MS2 input pins.

Table 2: Stepping Format

MS2	MS1	Step Mode
L	L	Full-step
L	H	Half-step
H	L	Quarter-step
H	H	Eighth-step

Decay Modes

During PWM off-time, the output current decay can operate in slow, fast, or mixed decay depending on the voltage level at the MDS input and any current change commanded by a STEP transition.

If the voltage on the MDS input pin is less than 2.5V, then mixed decay mode with an adjustable fast decay ratio is selected. The time that the device operates in fast decay can be approximated with Equation (4):

$$t_{FD} = V_{mds}(V) \times 0.4 \times t_{OFF} \quad (4)$$

After this fast decay portion (t_{FD}), the MP6520 switches to slow decay mode for the remainder of the constant-off-time period. Note that if MDS is set to 0V (connected to ground), slow decay is used for the entire off time.

If the voltage at the MDS input is greater than 2.8V, then automatic decay mode is selected. In automatic decay mode, if the commanded current level is equal to or higher than the level at the previous step, then slow decay is selected. If the current level is lower than previous level, then mixed decay with a fixed 30% fast decay ratio is selected.

nRSET, nSLEEP, and nENBL Operation

When nRSET is driven logic low, the step table is reset to the home position (see Table 3). The STEP input signal is ignored while nRSET is low.

Driving nSLEEP low puts the device into a low power sleep state. In this state, all internal circuits including the gate drive charge pump and the 3P3VOUT regulator are disabled. The H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, approximately 1ms of time must pass before issuing a STEP command to allow the internal circuitry to stabilize.

nENBL is used to control the output drivers. When nENBL is low, the output H-bridge outputs are enabled, and rising edges on STEP are recognized. When nENBL is high, the H-bridge outputs are disabled, and the STEP input is ignored.

Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from shutting down the high-side MOSFET erroneously. An internal fixed blanking time (t_{BLANK}) blanks the output of the current sense comparator when the outputs are switched, which is also the minimum on time for high-side MOSFET.

In automatic decay mode, if the current limit is reached within the blanking time, the mixed decay with 30% fast decay ratio is performed after the blanking time.

Charge Pump

The MP6520 integrates an internal charge pump to generate gate drive voltage for the high-side MOSFETs. The charge pump requires a 100nF ceramic capacitor rated for at least the voltage applied to VIN to be connected between the CPA and CPB, and a 1µF, 16V ceramic capacitor connected between VCP and VIN.

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Fault

The MP6520 provides an nFAULT pin, which is driven low when a fault condition such as OCP, OTP, or OVP occurs. nFAULT is an open-drain output, so if it is used, an external pull-up resistor is required. When the fault condition is released, nFAULT is pulled to a high level by the external pull-up resistor.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through any MOSFET. If the over-current limit threshold is reached and lasts longer than the over-current deglitch time, all MOSFETs in the H-bridge are disabled, and nFAULT is driven low. The driver remains disabled for approximately 5ms, then is re-enabled automatically. If this cycle repeats five times, the MP6520 shuts down.

Over-current conditions on both the high- and low-side devices (i.e.: a short to ground, supply, or across the motor winding) result in an over-current shutdown. Note that OCP does not use the current sense circuitry used for PWM current control and is independent of the sense resistor value or VREF voltage.

Over-Voltage Protection (OVP)

If the input voltage on VIN is higher than the OVP threshold, the H-bridge output is disabled, and nFAULT is driven low. This protection is released when VIN drops to a safe level.

Input UVLO Protection

If the voltage on VIN falls below the under-voltage lockout (UVLO) threshold voltage at any time, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when VIN rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, all MOSFETs in the H-bridge are disabled, and nFAULT is driven low. Once the die temperature has fallen to a safe level, operation resumes automatically.

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Table 3: Step Table (Relative Current Level Sequence)

Eighth-Step #	Quarter-Step #	Half-Step #	Full-Step #	Phase A Current $\%I_{Trip-LIMIT}$ (%)	Phase B Current $\%I_{Trip-LIMIT}$ (%)	Step Angle (°C)
1	1	1		100.00	0.00	0.0
2				98.08	19.51	11.3
3	2			92.39	38.27	22.5
4				83.15	55.56	33.8
***5**	**3**	**2**	**1**	**70.71**	**70.71**	**45.0**
6				55.56	83.15	56.3
7	4			38.27	92.39	67.5
8				19.51	98.08	78.8
9	5	3		0.00	100.00	90.0
10				-19.51	98.08	101.3
11	6			-38.27	92.39	112.5
12				-55.56	83.15	123.8
13	7	4	2	-70.71	70.71	135.0
14				-83.15	55.56	146.3
15	8			-92.39	38.27	157.5
16				-98.08	19.51	168.8
17	9	5		-100.00	0.00	180.0
18				-98.08	-19.51	191.3
19	10			-92.39	-38.27	202.5
20				-83.15	-55.56	213.8
21	11	6	3	-70.71	-70.71	225.0
22				-55.56	-83.15	236.3
23	12			-38.27	-92.39	247.5
24				-19.51	-98.08	258.8
25	13	7		0.00	-100.00	270.0
26				19.51	-98.08	281.3
27	14			38.27	-92.39	292.5
28				55.56	-83.15	303.8
29	15	8	4	70.71	-70.71	315.0
30				83.15	-55.56	326.3
31	16			92.39	-38.27	337.5
32				98.08	-19.51	348.8

* The home position is at step angle 45°.

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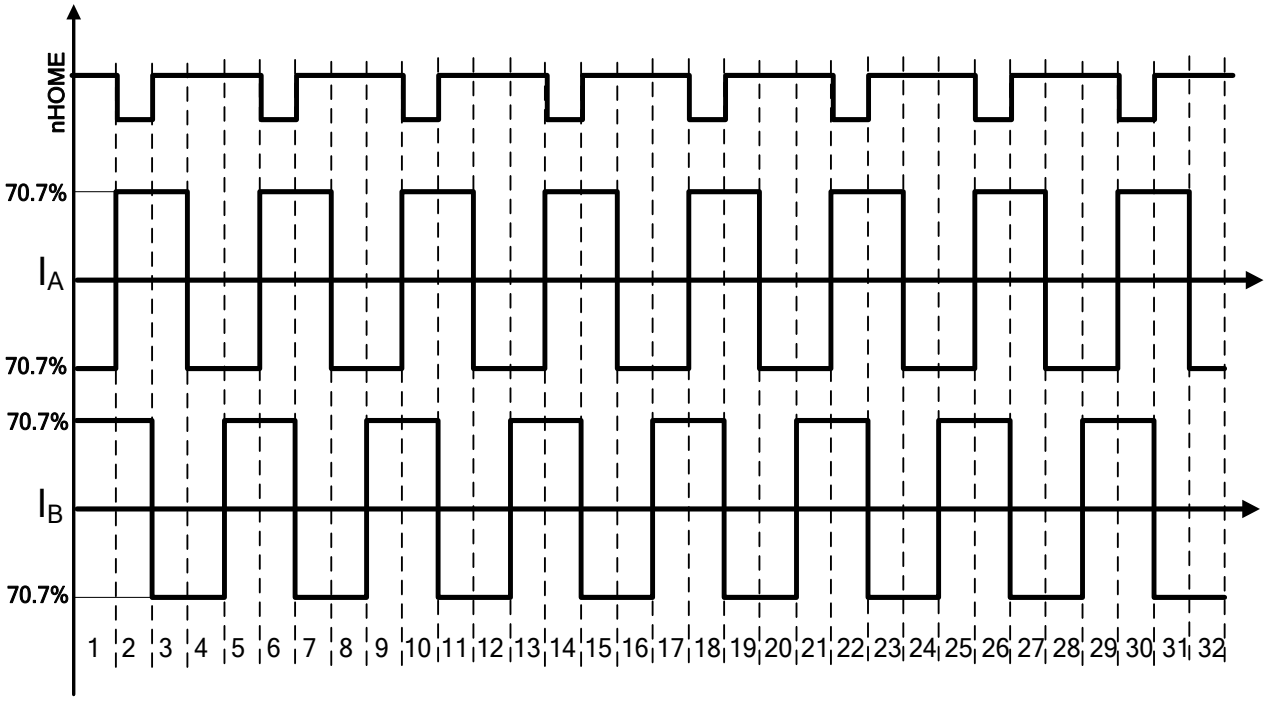

Figure 3a: Full-Step Winding Current

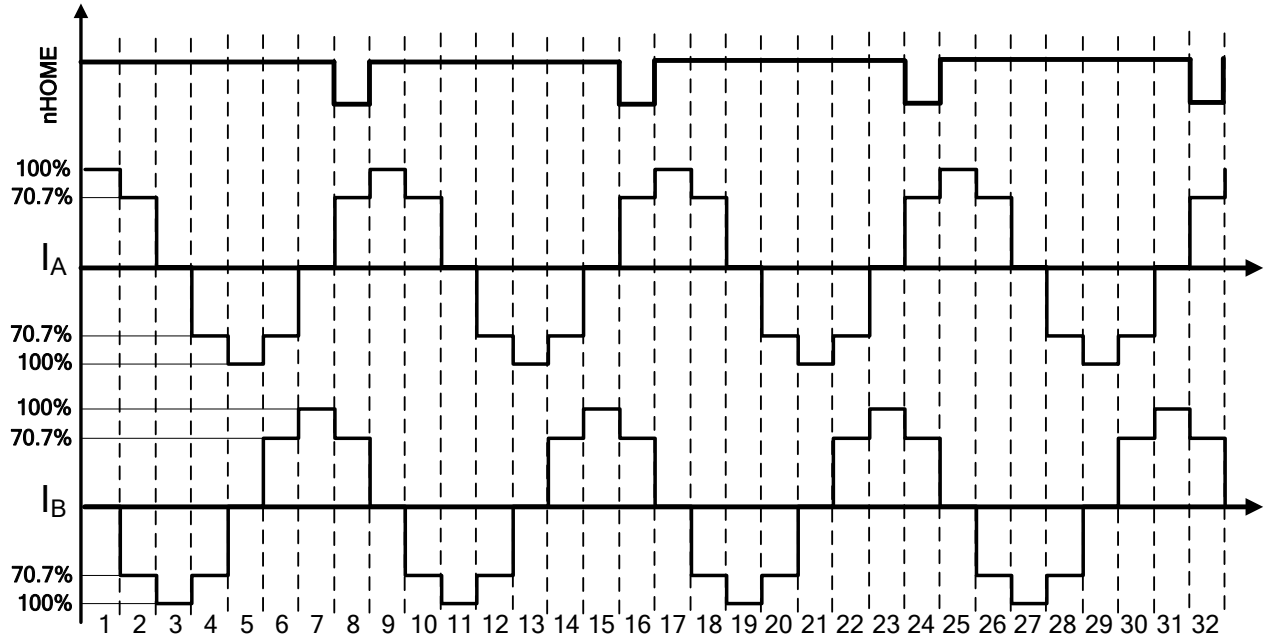

Figure 3b: Half-Step Winding Current

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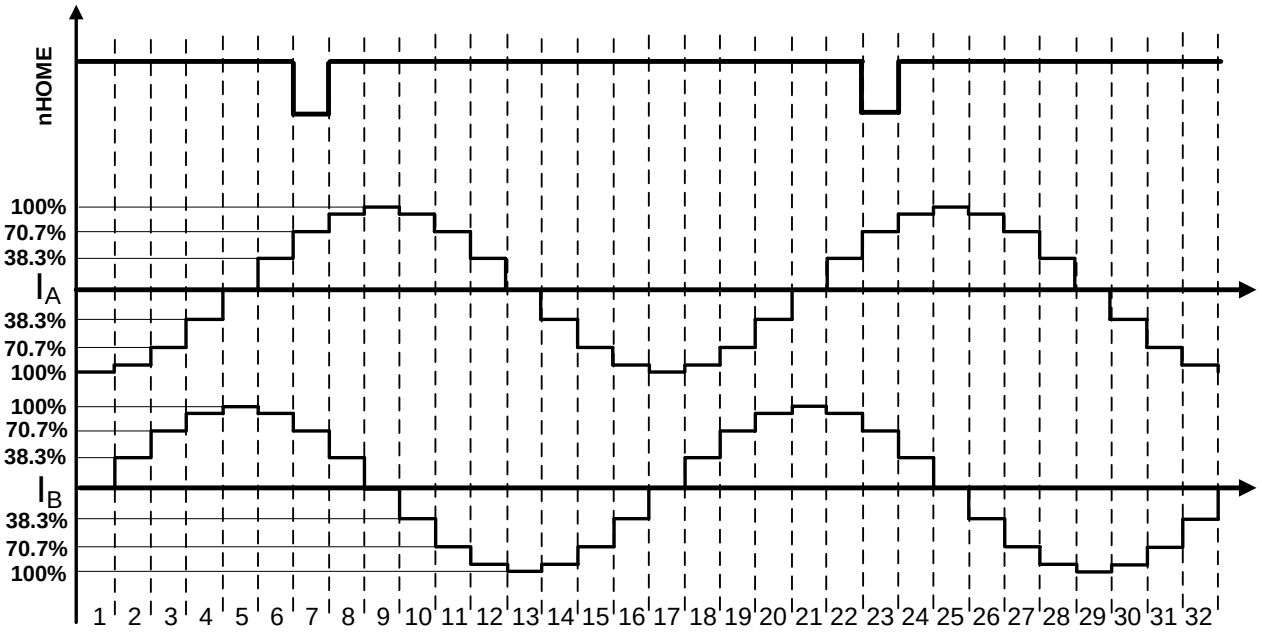

Figure 3c: Quarter-Step Winding Current

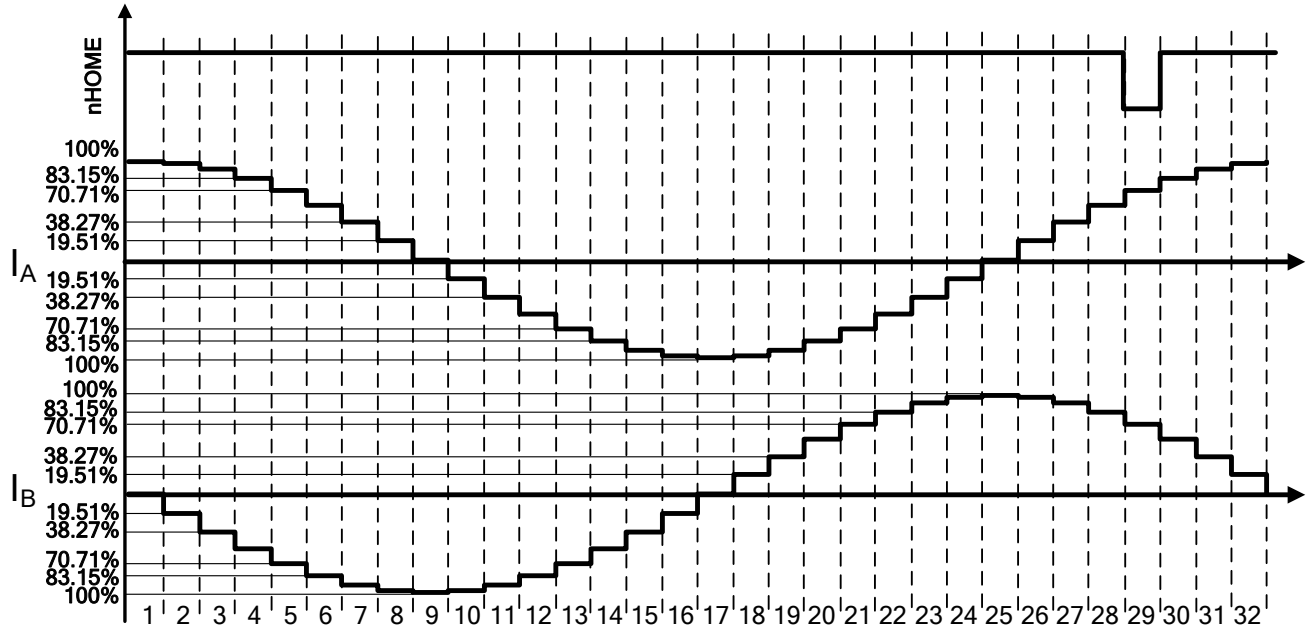

Figure 3d: Eighth-Step Winding Current

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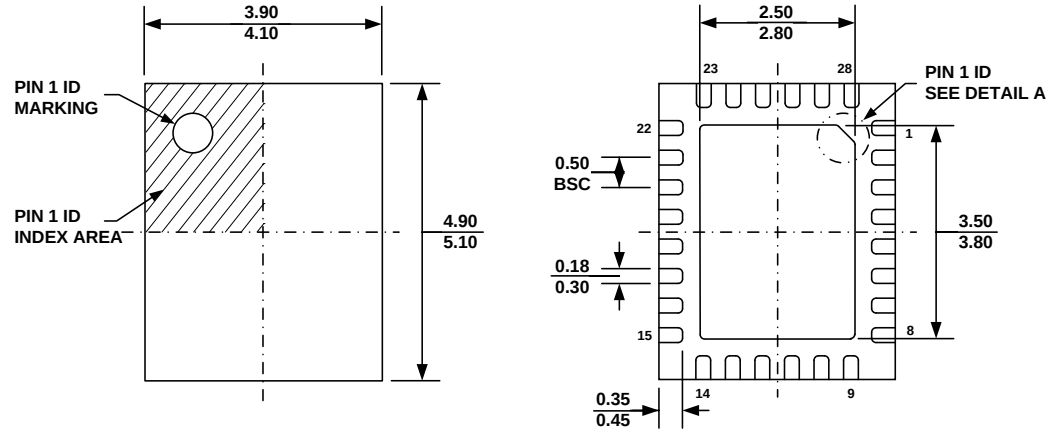
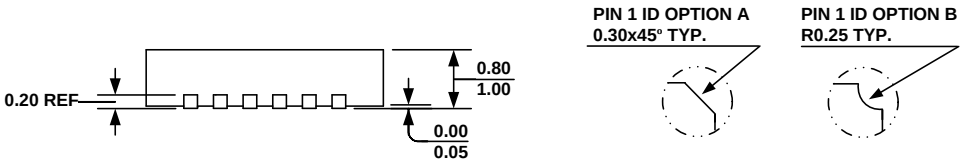
PACKAGE INFORMATION

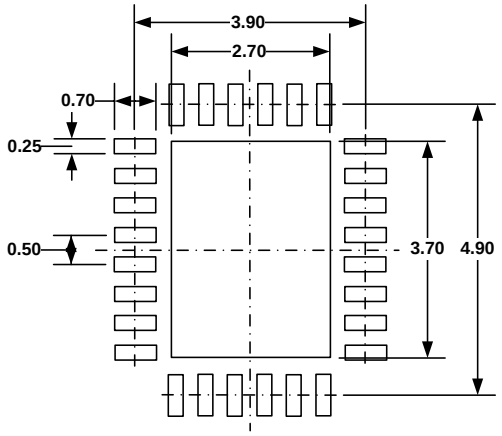
QFN-28 (4mmx5mm)



TOP VIEW **BOTTOM VIEW**



SIDE VIEW **DETAIL A**



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

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