MP6412

Ultra-Low I_Q Load-Switch Controller with RESET Timer

DESCRIPTION

The MP6412 is a load-switch controller used to turn the main-power P-channel MOSFET on and off. The MP6412 has a 2.2V to 12V operating input voltage range. The MP6412 is a space-saving solution for smartphones, tablets, and other portable device applications.

The MP6412 is equipped with reset and power sequence functions with a factory-programmable delay timer. The reset and power sequence are controlled by the RST0/RST1 and OFF signals. The MP6412 also has a system discharge path, shipping mode and charger insert detection feature.

The MP6412 is available in a UTQFN-10 (1.4mmx1.8mm) package.

FEATURES

- V_{IN} Range from 2.2V to 12V
- P-MOSFET Gate Driver
- Auto 150Ω Output Discharge
- <2μA Quiescent Current
- <1μA Shipping Mode Current
- Factory-Fixed Reset Delay
- ESD HBM 2kV
- Available in a Space-Saving UTQFN-10 (1.4mmx1.8mm) Package

APPLICATIONS

- Mobile Phones
- Portable/Handheld Devices
- Wearable Devices

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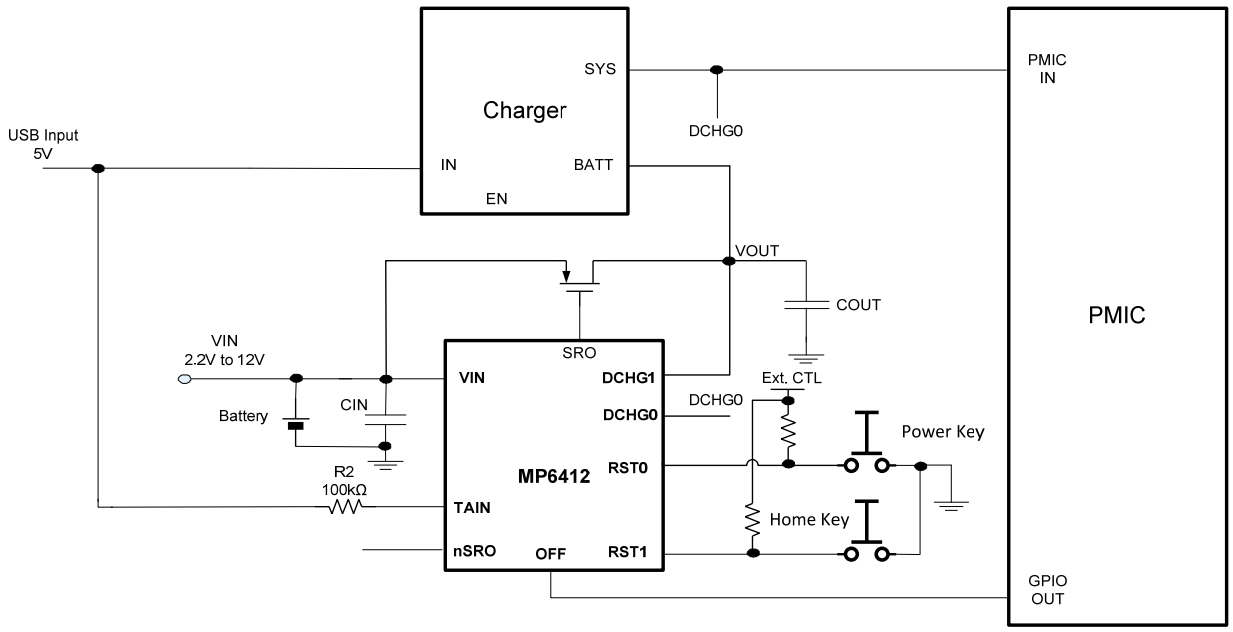
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6412GQGU	UTQFN-10 (1.4mmx1.8mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6412GQGU–Z).

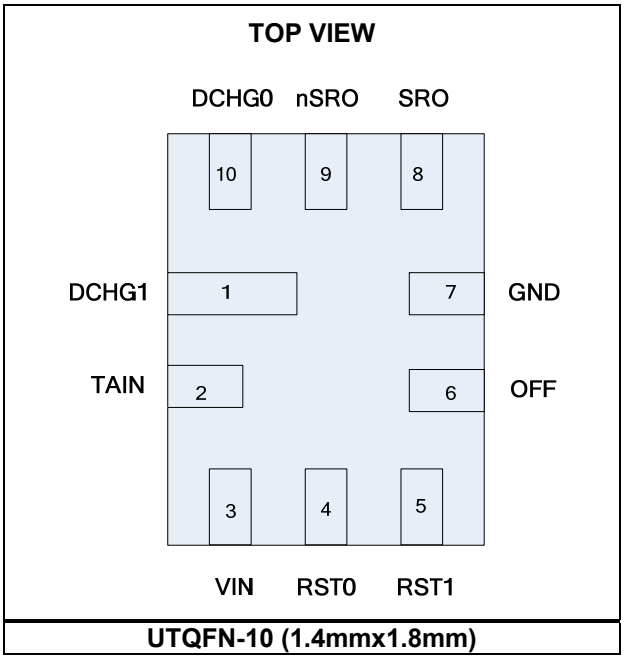
TOP MARKING

$\overline{\text{FV}}$

LL

FV: Product code of MP6412GQGU
LL: Lot number

PACKAGE REFERENCE



UTQFN-10 (1.4mmx1.8mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	DCHG1	**Path 1 discharge pin.** DCHG1 begins to discharge when the MP6412 enters RESET mode and TAIN is low.
2	TAIN	**Charger insert detection pin.** TAIN pulls down to GND internally through a resistor. When a charger is inserted, TAIN is pulled high by an external charger.
3	VIN	**Input power supply.**
4	RST0	**Reset input 0.** RST0 is active low. Do not float RST0.
5	RST1	**Reset input 1**. RST1 is active low. Do not float RST1.
6	OFF	**Function to turn off external P-FET to enter shipping mode.** OFF pulls down to GND internally through a resistor.
7	GND	**Ground.**
8	SRO	**System reset output signal.** SRO is the push-pull output. SRO has an external P-FET gate driver.
9	nSRO	**System reset output negative signal.** nSRO is an open-drain output. When SRO is low, the open-drain MOSFET is off. When SRO is high, the open-drain MOSFET is on. nSRO is floated in shipping mode.
10	DCHG0	**Path 0 discharge pin.** DCHG0 begins to discharge when the MP6412 enters RESET mode and TAIN is low.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to 14V
$V_{RST0/RST1}$ ..... -0.3V to 6V
V_{OFF} ..... -0.3V to 6V
V_{TAIN}, $V_{DCHG0/1}$, V_{SRO}, V_{nSRO}..... -0.3V to 14V
Junction temperature ..... 150°C
Lead temperature..... 260°C
Continuous power dissipation (T_A = +25°C) (2)
..... 0.9W
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.2V to 12V
$V_{RST0/RST1}$ ..... 0V to 5.5V
V_{OFF} ..... 0V to 5.5V
V_{TAIN}, V_{DCHG0}, V_{DCHG1} ..... 0V to 12V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

UTQFN-10 (1.4mmx1.8mm).... 140 .. 30 ...°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input and Supply Voltage Range						
Input voltage	V_{IN}		2.2		12	V
Supply Current						
Shipping mode current	I_{OFF}	V_{IN} = 3.6V, load switch off, shipping mode		0.75	1.5	μA
On state current	I_{ON1}	V_{IN} = 3.6V, load switch on, no load, no action assert			2	μA
	I_{ON2}	V_{IN} = 3.6V, load switch on, no load, action assert to turn OSC on			10	μA
Gate Driver						
SRO rising time	T_{Rise}	V_{IN} = 4V, Qg = 20nC	1	2	3	ms
SRO falling time	T_{Fall}	V_{IN} = 4V, Qg = 20nC	1	2	3	ms
SRO rising delay (5)	T_{SRO}	Between V_{IN} good and SRO starting to fall	1	2	3	ms
SRO logic high level			V_{IN}-0.3			V
SRO logic low level					0.3	V
$V_{DCHG0/1}$ discharge resistance		Force 1mA current		70	120	Ω
		$V_{DCH0/1}$ = 4V		150		Ω
Discharge delay (5)	T_{DD}		4	5	6	ms
Under-Voltage Protection (UVP)						
VIN under-voltage lockout threshold	V_{IN_UVLO}			1.43		V
UVLO hysteresis (6)	$V_{UVLOHYS}$			500		mV
RST0/RST1/OFF Logic (Input)						
RST0/1 high level	V_H		1			V
RST0/1 low level	V_L				0.4	V
OFF high level	V_{HOFF}		1			V
OFF low level	V_{LOFF}				0.4	V
OFF pull-down resistor				1		MΩ
RST0/RST1 leakage current		V_{IN} = V_{RST0} = V_{RST1} = 3.6V			150	nA
Debounce time (5)	T_{DG1}	RST0, RST1, TAIN		10		ms
	T_{DG2}	OFF		250		μs
nSRO Logic (Open-Drain Output)						
High level		V_{IN} = 3.3V, pull up V_{IN} through external 100kΩ	V_{IN}*0.8	V_{IN}		V
Low level		Sink 1mA			0.4	V
nSRO leakage current/logic high		V_{IN} = 3.3V, pull up V_{IN} through external 100kΩ		50		nA
TAIN Logic (Input)						
TAIN rising			2.8	3.15	3.5	V
TAIN hysteresis				100		mV
TAIN confirm delay (5)	T_7		40	50	60	ms
TAIN internal pull-down resistor				2		MΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
RESET Time (5)						
Power RESET entry time (5)	T_1		8	10	12	s
Power RESET off time (5)	T_2		0.32	0.4	0.48	s
Turn-off response time (5)	T_3		1	1.5	2	ms
Turn-off confirm cycle (6)				5		
Turn-off confirm time (5)	T_4		80	100	120	ms
Turn-off delay time (5)	T_5		12	15	18	s
Turn-on response time (5)	T_6		1.6	2	2.4	s
SRO pull-up current		V_{IN} = 4V		1.3		µA

NOTES:

5) Guaranteed by correlation.

6) Guaranteed by engineering sample test, not tested in production.

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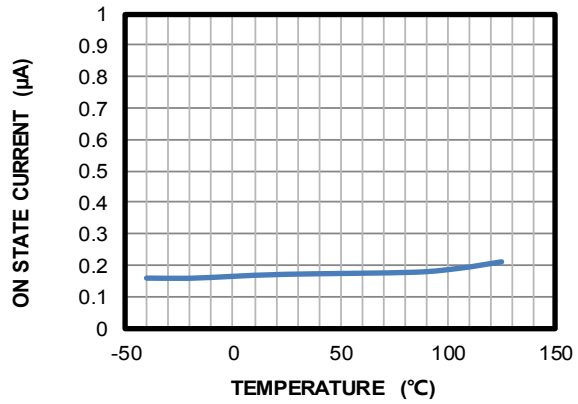
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, T_A = 25°C, unless otherwise noted.

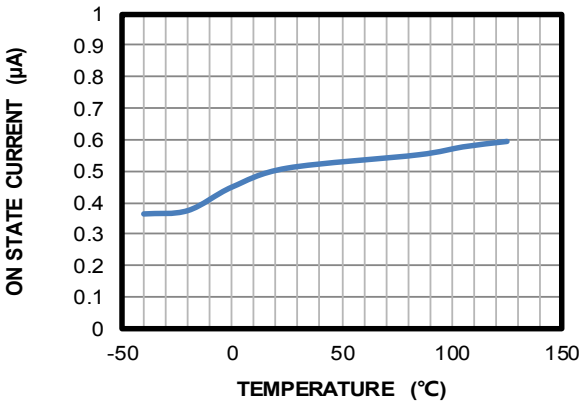
On-State Current vs. Temperature

V_{IN} = 2.2V



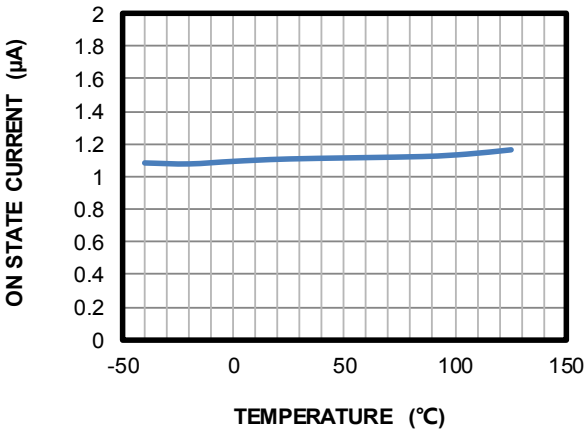
On-State Current vs. Temperature

V_{IN} = 3.6V

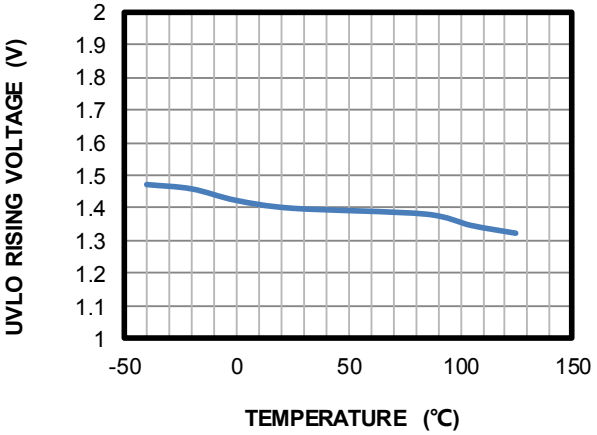


On-State Current vs. Temperature

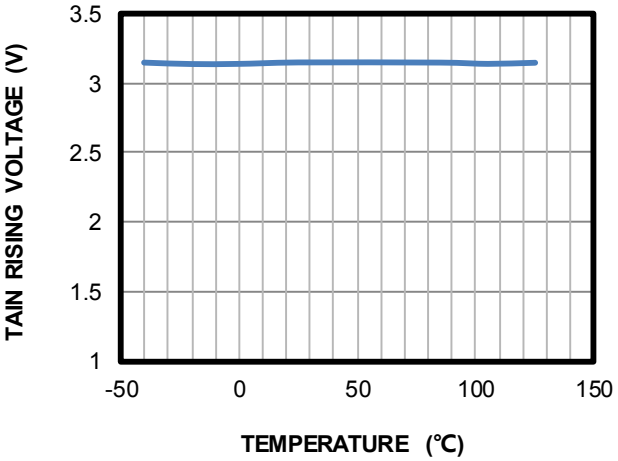
V_{IN} = 12V



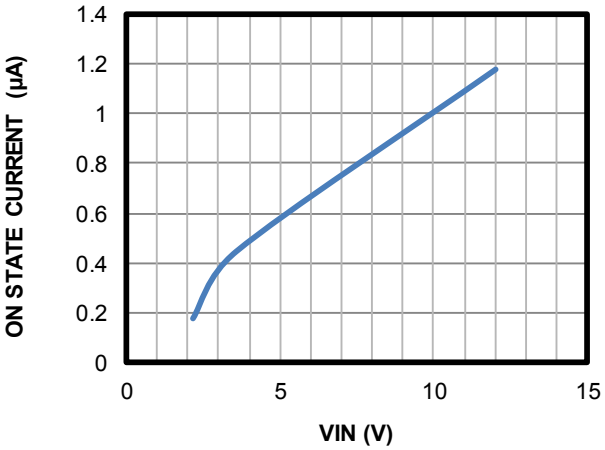
UVLO Rising Voltage vs. Temperature



TAIN Rising Voltage vs. Temperature



On-State Current vs. V_{IN}



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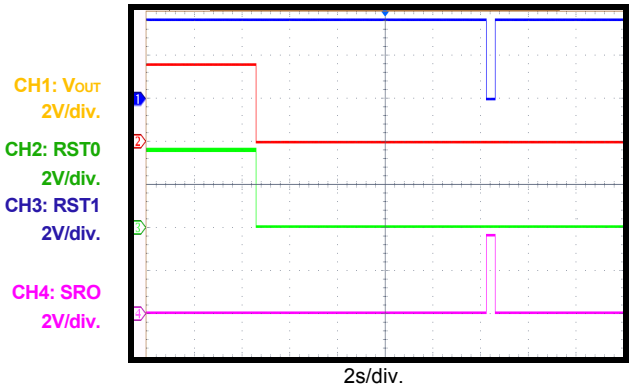
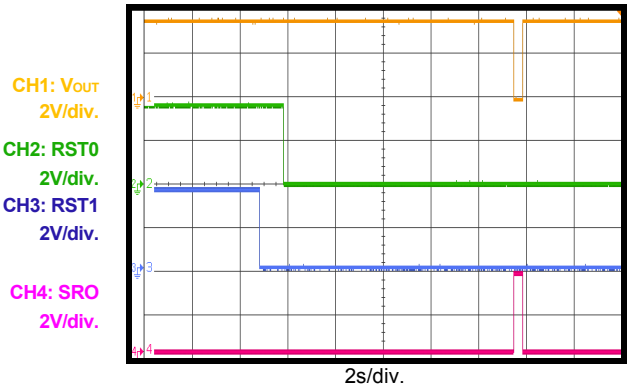
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_A = 25°C, unless otherwise noted.

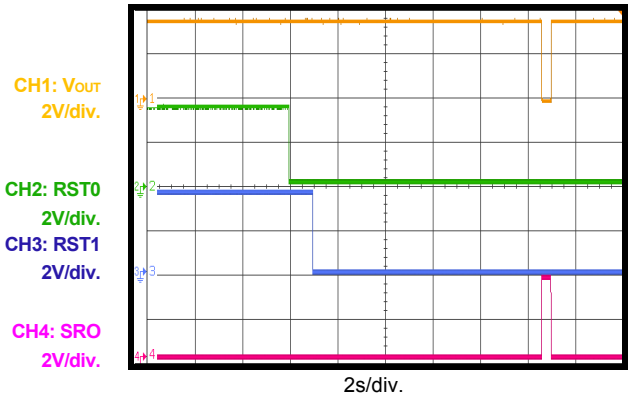
Reset Function



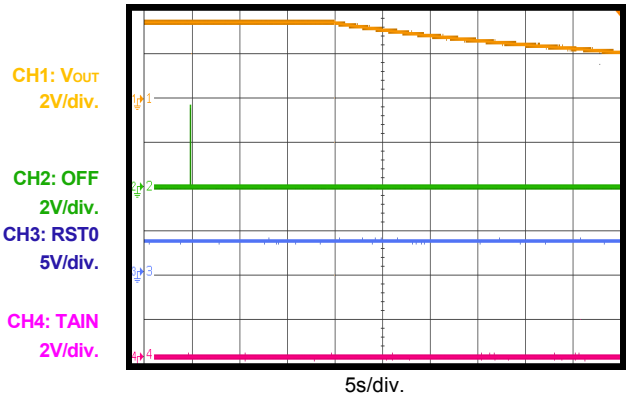
Reset Function (RST1 First)



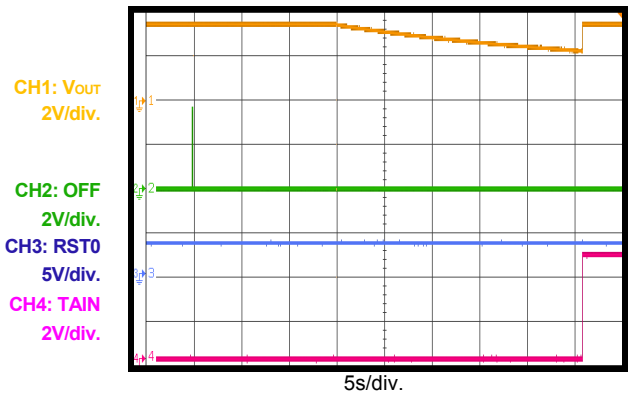
Reset Function (RST0 First)



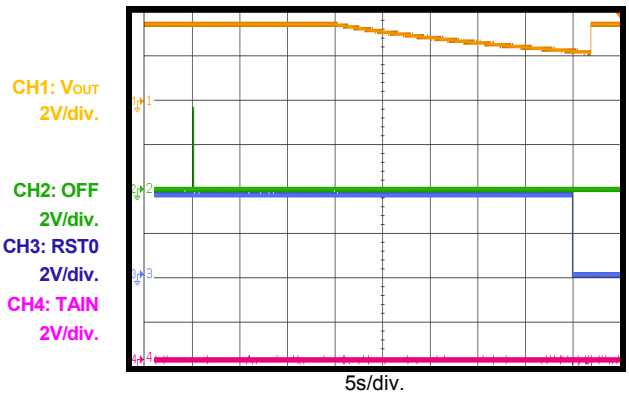
Shipping Mode Enter



Shipping Mode Exit with TAIN



Shipping Mode Exit with RST0



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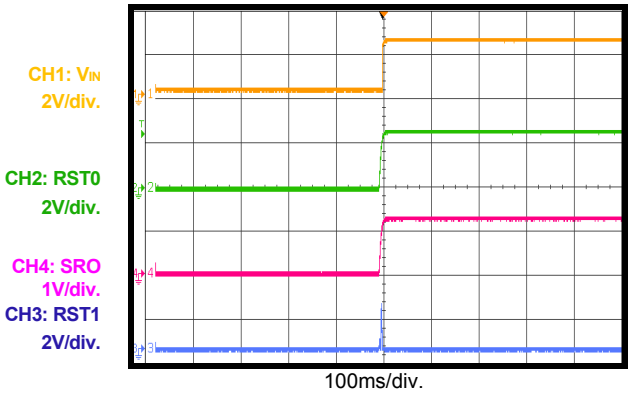
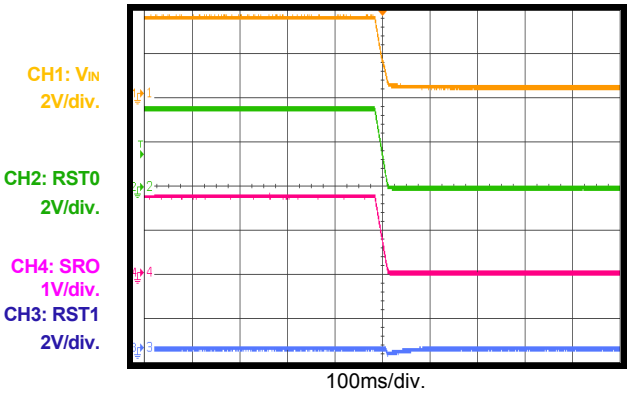
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_A = 25°C, unless otherwise noted.

Start-Up



Shutdown



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BLOCK DIAGRAM

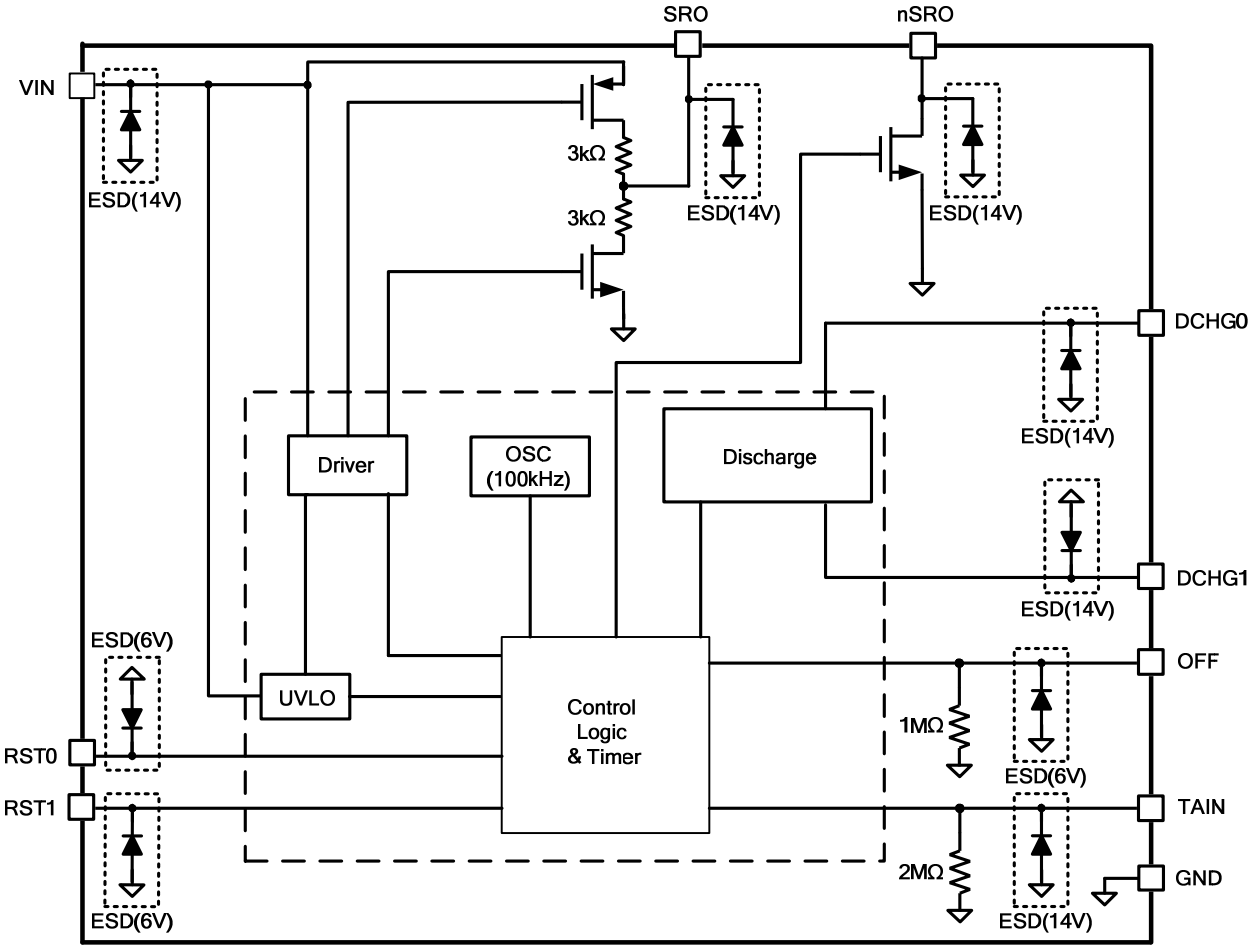

Figure 1: Functional Block Diagram

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OPERATION

The MP6412 is a load-switch controller to turn the main power P-channel MOSFET on and off. The MP6412 has a 2.2V to 12V operating input voltage range. The MP6412 provides a space-saving solution for smartphones, tablets, and other portable device applications.

The MP6412 is equipped with reset and power sequence functions with a factory-programmable delay timer. The reset and power sequence are controlled by the RST0/RST1 and OFF signals. For mobile applications, the MP6412 has two discharge paths and a charger insert detection feature.

Reset Function (RESET)

The MP6412 can reset the system by turning off the external power MOSFET (load switch) if needed. This action clears the current status and restarts to the initial status by cutting off the power supply of the down-stream system. Enter the RESET function by pulling both RST0 and RST1 down to logic low for 10s (Note that T_2' = T_2 + T_{DD} x 2).

Figure 2 and Figure 3 show the waveforms during a T_2' RESET action.

To avoid an erroneous RST0/1 trigger, a debounce time (TDG1) can be implemented. If the logic glitch duration is less than TDG1, the logic glitch is ignored (see Figure 4).

In normal operation, if the MP6412 detects that both RST0 and RST1 are low for 10s, the MP6412 turns off the load switch for T_2' (400 + 10ms) and restarts it. During the 400ms off time, DCHG0 and DCHG1 turn on their respective discharge path to pull down the V_{OUT} and system voltage to clear out the current status. The RESET function can be activated once RST0 and RST1 are both active. The next RESET function is active after the RST0 or RST1 logic changes again (See Figure 5 and Figure 6).

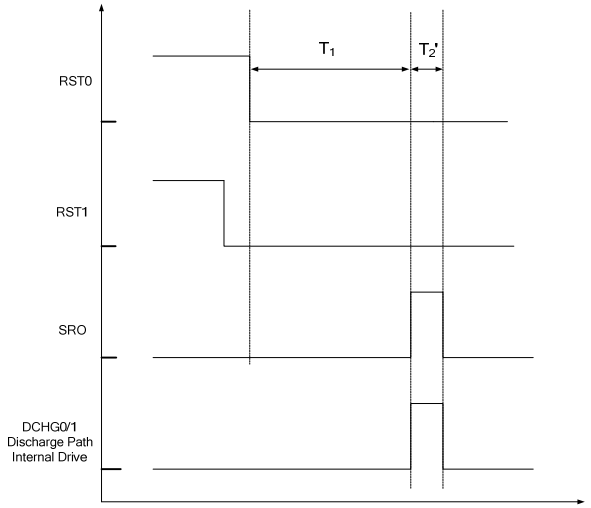

Figure 2: RESET Procedure

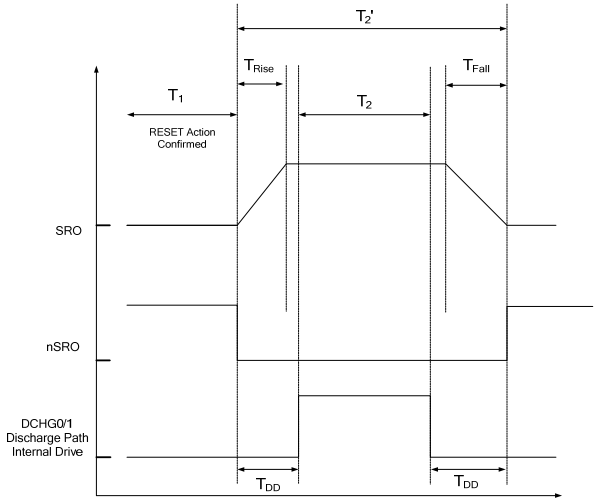

Figure 3: SRO and Discharge Procedure

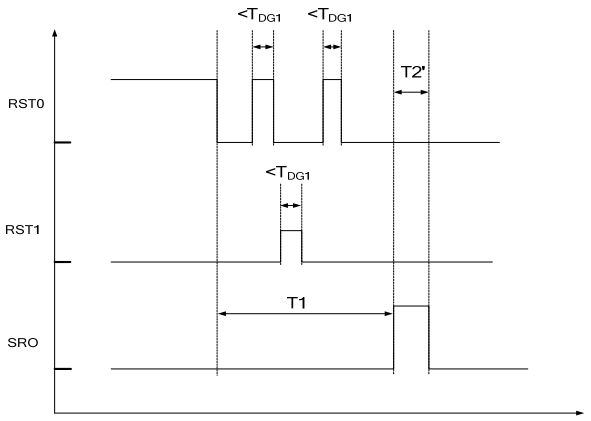

Figure 4: Debounce Procedure

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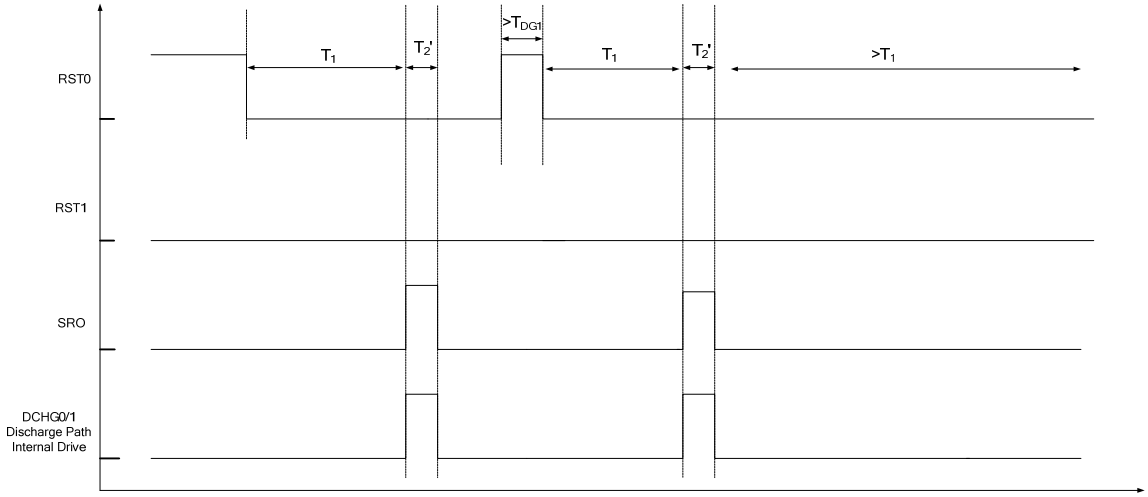

Figure 5: Multiple RST0 Reset

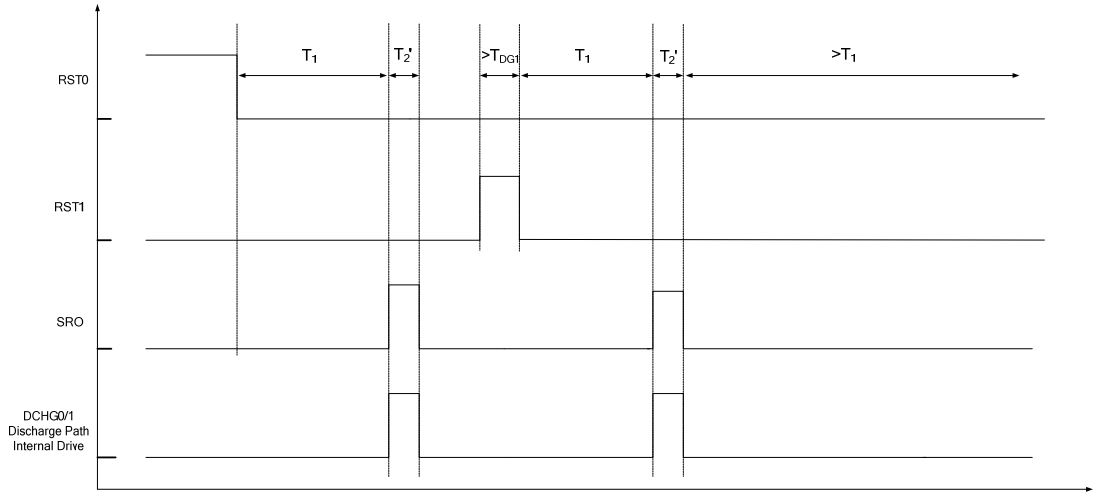

Figure 6: Multiple RST1 Reset

During T_1 (after RST0/1 both drop low) and T_2' (if a RESET action occurs), the RESET action has the highest priority. This action masks the high TAIN logic or shipping mode trigger signal. During T_1 and its follow RESET period, all signals are ignored. Refer to the Enter/Exit Shipping Mode sections on page 11 and page 13.

Enter Shipping Mode

The MP6412 can fully turn off the load switch to achieve a very small shutdown current. In this mode, the MP6412 cuts off the battery from the system. Therefore, the battery energy can be stored for a long time due to the low consumption current of the MP6412 in shipping mode.

In normal status, a specific OFF pin signal (on time more than T_3, off time more than T_3, repeat five cycles in 100ms) makes the MP6412 turn off the load switch and enter shipping mode. Afterward, nSRO is floated (see Figure 7). The discharge function is not active in this mode.

If the enter shipping mode signal is confirmed, all signals are ignored during T_5.

To avoid an erroneous OFF trigger, a debounce time (TDG2) can be implemented. If the logic glitch duration is less than TDG2, the logic glitch will be ignored (see Figure 8).

The OFF signal has lower priority than RST0/1 signal. OFF is terminated if RST0/1 low occurs (see Figure 9).

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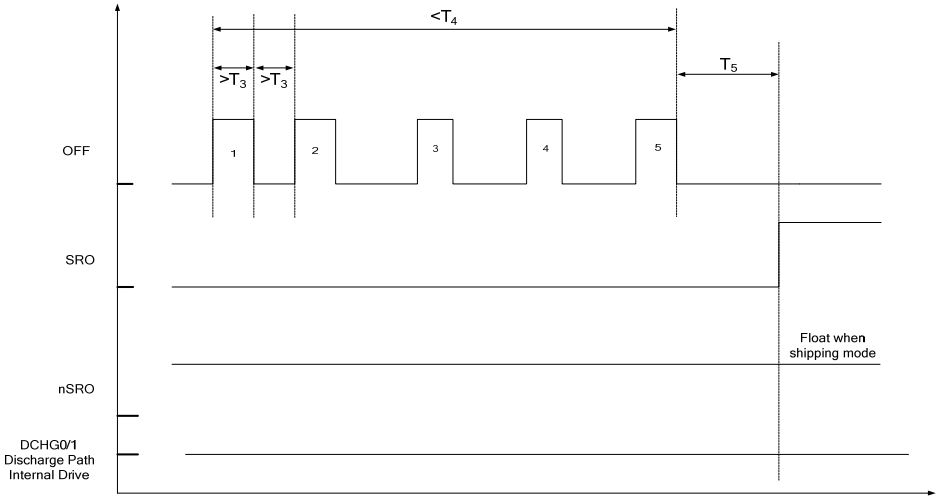

Figure 7: Entering Shipping Mode

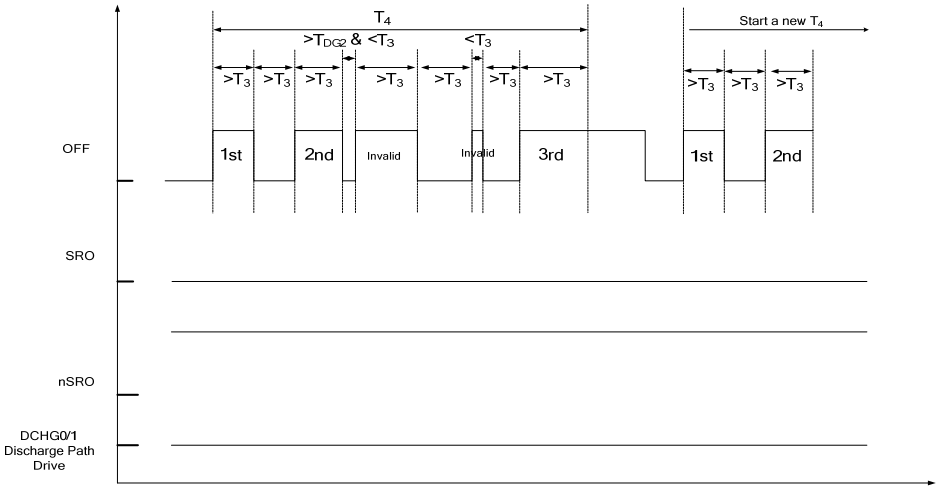

Figure 8: Cannot Enter Shipping Mode

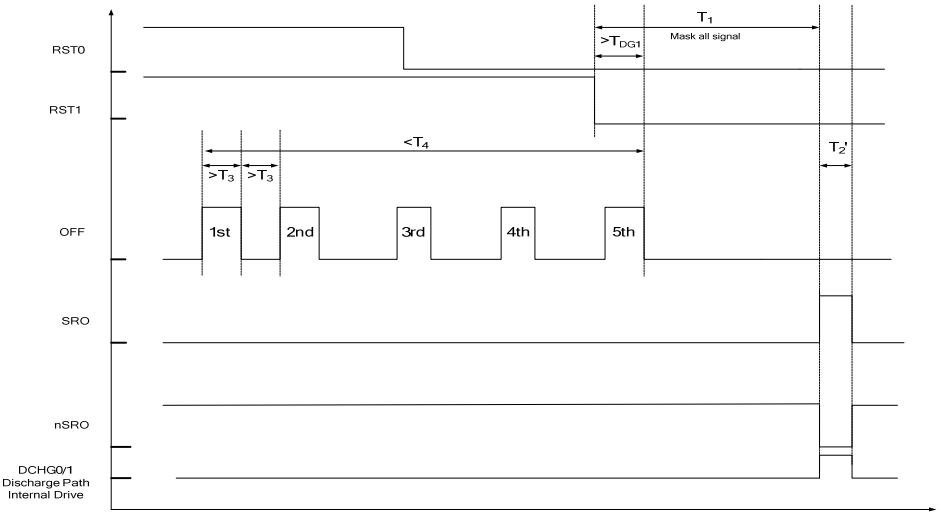

Figure 9: OFF Priority Procedure

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The OFF signal has higher priority than the TAIN signal. After the OFF signal is confirmed, the high TAIN signal can exit the MP6412 from shipping mode (see Figure 10).

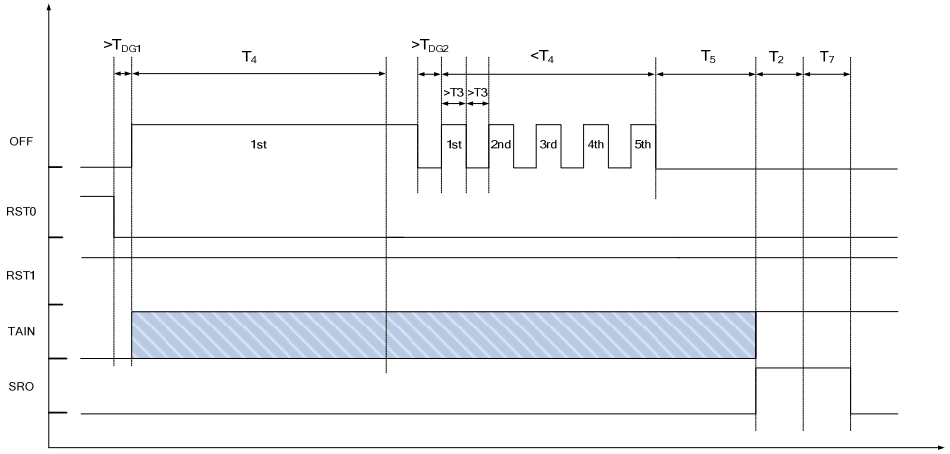

Figure 10: OFF Priority Procedure

Exiting Shipping Mode

The MP6412 turns on the load switch when exiting shipping mode.

In shipping mode, when the RST0 signal is pulled down for 2s and V_{IN} is higher than its under-voltage lockout (UVLO) threshold, the MP6412 exits shipping mode and turns on the load switch.

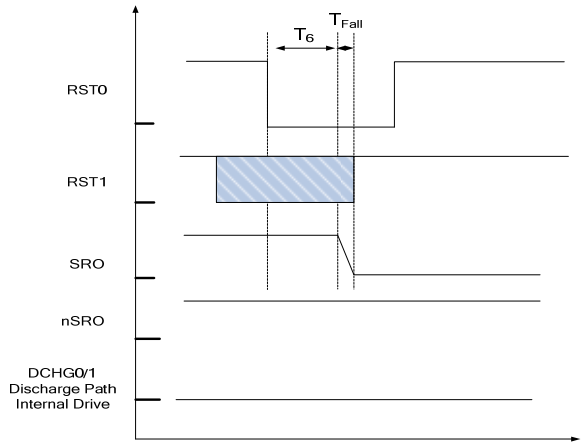

Figure 11: Shipping Mode Exit Procedure

In addition to RST0, a high TAIN signal can also make the MP6412 exit shipping mode. TAIN is connected to the power jack through a 100kΩ resistor, typically. When a charger is inserted, TAIN monitors a high logic, which can also make the MP6412 exit shipping mode.

Figure 12 shows the MP6412 in shipping mode initially. TAIN and RST0 can both be used to make the MP6412 exit shipping mode, but the MP6412 must confirm the action of TAIN first.

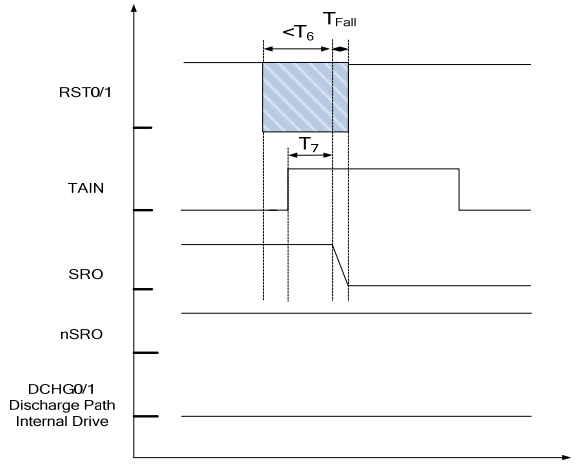

Figure 12: TAIN Procedure

When the MP6412 is in shipping mode, a RST0 or TAIN input is required to exit shipping mode. The RST0 input requires a logic change to enable the confirmation sequence. If RST0 is dead low when the OFF confirm time is triggered, the MP6412 does not exit shipping mode (see Figure 13). If TAIN is dead high when the OFF confirm time is triggered, the shipping mode logic cannot be masked (see Figure 14).

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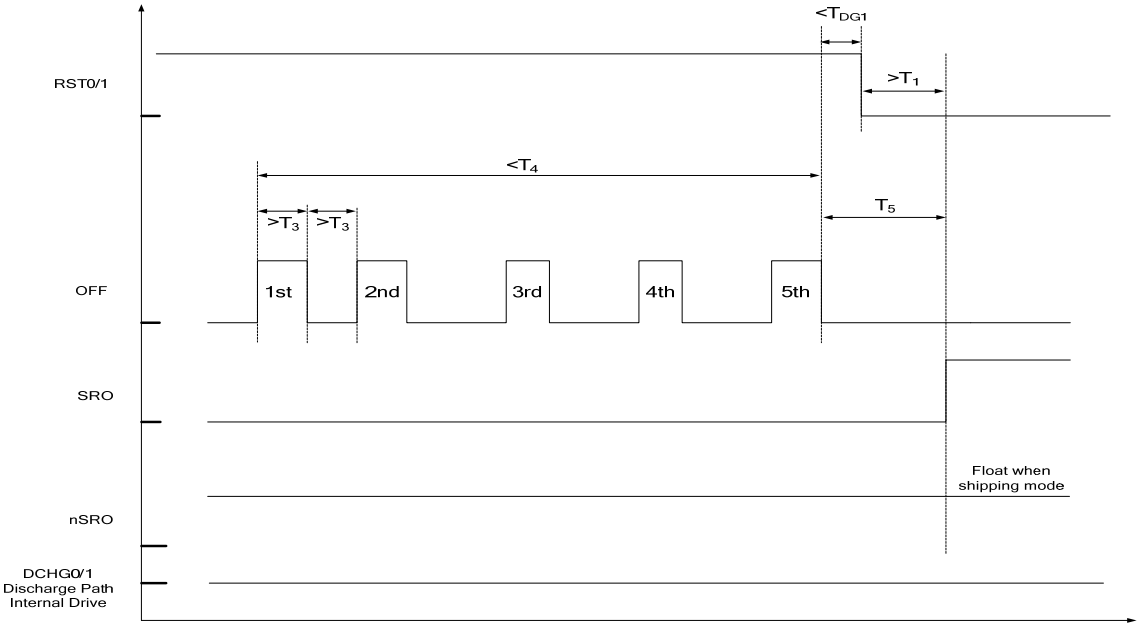

Figure 13: RST0/1 Not Exiting Shipping

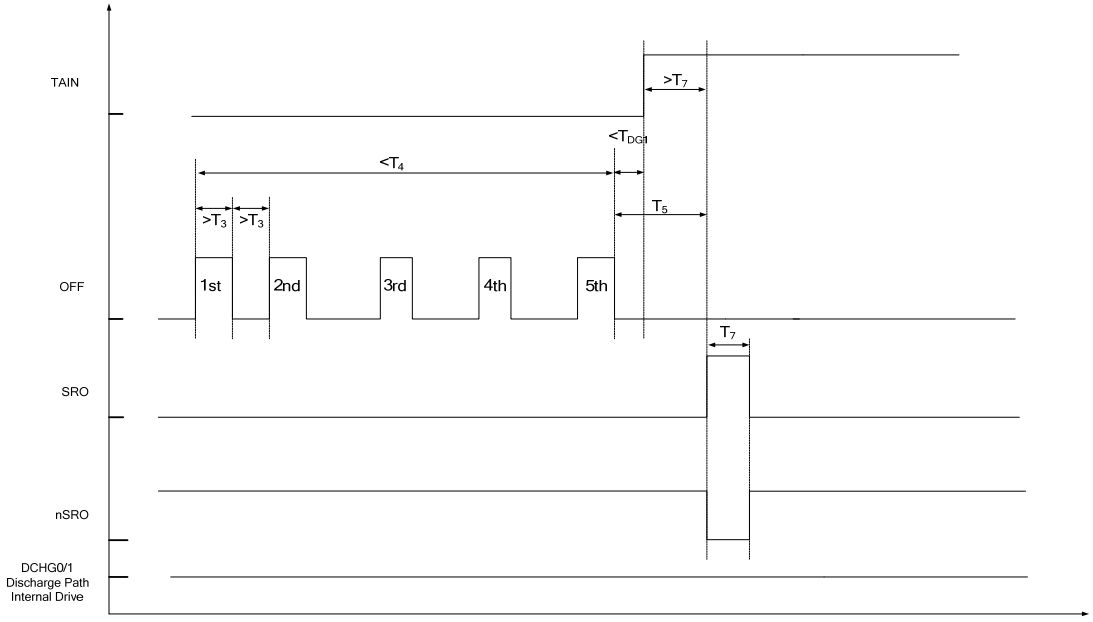

Figure 14: TAIN Cycle Exiting Shipping

TAIN Feature

TAIN is connected to an external charger through a 100kΩ resistor. TAIN has an internal 2MΩ pull-down resistor to ground. The external and internal resistors form a resistor-divider circuit. The TAIN voltage can be calculated with Equation (1):

$$V(TAIN) = \frac{R_{Int}}{R_{Int}+R_{Ext}} \times V(Charger) \quad (1)$$

Where V(TAIN) is the TAIN voltage, V(Charger) is the external charger voltage, R_{Ext} is the external resistor, and R_{Int} is the internal 2MΩ resistor.

When the TAIN voltage is higher than 3.3V, it is treated as an active high logic. If the MP6412 is in shipping mode, this high logic makes the MP6412 exit it.

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Figure 15 shows the TAIN internal ESD structure, which is equal to a Zener diode. When VCHG is high (maximum 30V), the ESD breaks down and clamps the TAIN voltage to 14V. The internal ESD safe current is 1mA to prevent damage to the ESD Zener diode. For example, when VCHG is 30V, there is a 16V voltage between VCHG and TAIN pin, and the current through the resistor and ESD diode is 160μA.

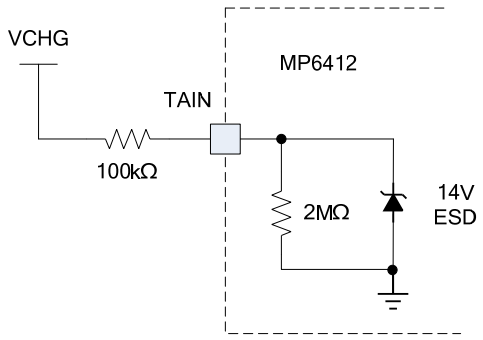

Figure 15: TAIN ESD Structure

Power-On

When VIN rises from a very low value to the MP6412 UVLO, a power-on procedure begins. The MP6412 turns on the external P-channel MOSFET (P-FET) softly to prevent inrush current. The power-on procedure is shown in Figure 16.

The power-on procedure is a RESET procedure and ignores the RST0 and RST1 RESET signals. To enable a RESET function, the RST0 logic must be changed.

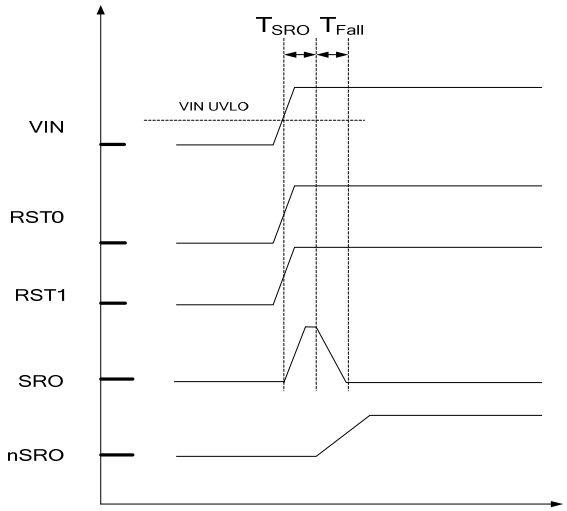

Figure 16: Power-On Priority

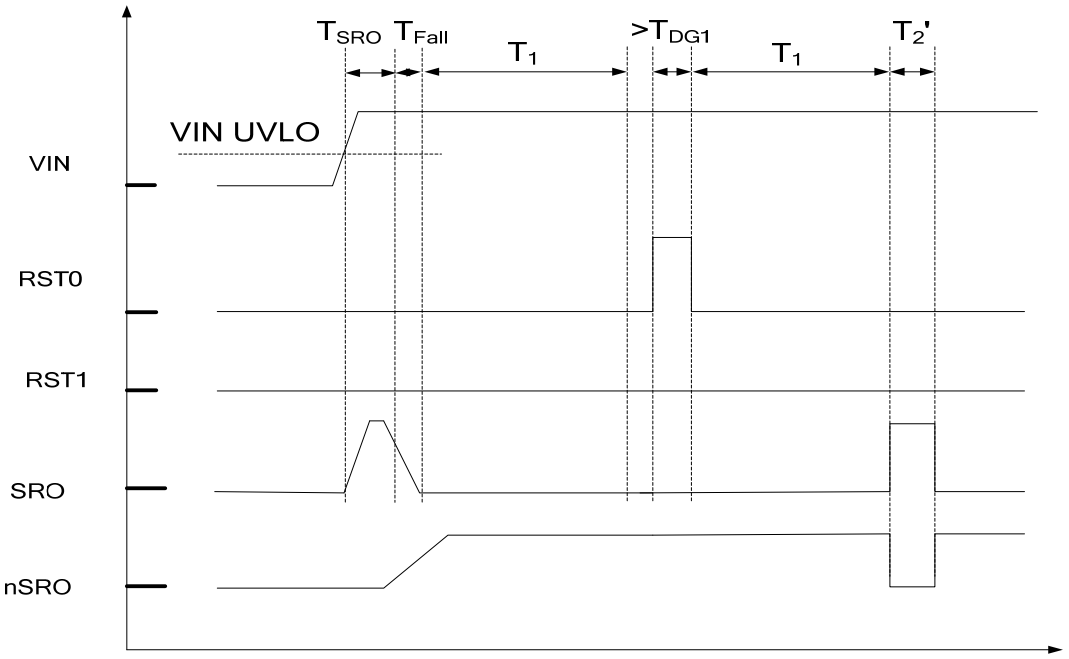

Figure 17: RESET after Power-On

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Discharge

The MP6412 has two discharge paths (DCHG0/1) to release system energy during a RESET action. The DCHG0/1 path is enabled during T_2. These discharge paths are through a passive resistor. If an external charger is plugged in, the passive resistor is too large to pull DCH0/1 low, and the discharge current generates a high temperature on the IC. A TAIN high logic disables DCH0/1 immediately under this situation (see Figure 18 and Table 2).

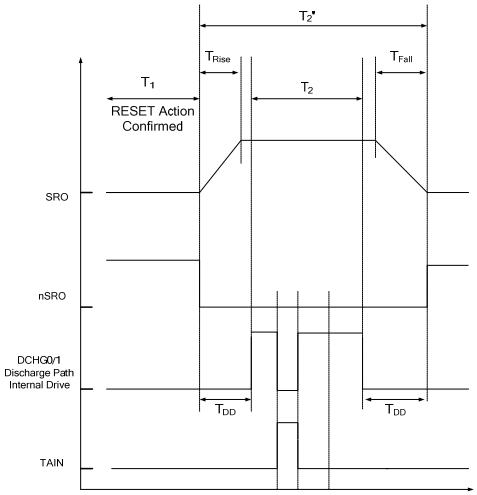

Figure 18: TAIN Disable Discharge

Conflicts Strategy

The MP6412 has different response actions when RST0/RST1/OFF/TAIN has input voltage. To prevent input conflicts, refer to Table 1.

Table 1: Signal Priority

Priority	Action
1	RESET
2	OFF
3	TAIN

RESET has the highest priority. The MP6412 only answers the highest priority requirement if several actions occur at the same time.

If some actions are active at the same time and one of these actions is confirmed first, the other actions will be ignored. For example, if the OFF action is confirmed first, the MP6412 enters shipping mode after 15s. In this period, RST0/RST1/TAIN cannot terminate it.

nSRO Function

The nSRO output is an open-drain output. Its output indicates the main power MOSFET status. When the main power MOSFET is on, it output a high logic. Otherwise, it outputs a low logic. nSRO does not have a soft on/off effect like SRO. The nSRO signal floats if the MP6412 enters shipping mode.

Table 2: State Change Table

	Event 0					STATE0			Event0 For (in seconds)	STATE1			Duration between state1 and 2	STATE2		
	VIN	RST0	RST1	TAIN	OFF	SRO	nSRO	DCHGx		SRO	nSRO	DCHGx		SRO	nSRO	DCHGx
POR	↑	X	X	X	X	0	Open	Open	T_{SRO}	H	X	X	T_{Fall}	L	Open	Open
RESET	VIN	L	H	X	X	L	Open	Open		L	Open	Open		L	Open	Open
	VIN	L	L	H	X	L	Open	Open	T1	↑	↓	Open	T2'	↓	↑	Open
	VIN	L	L	L	X	L	Open	Open	T1	↑	↓	↓	T2'	↓	↑	↑
	VIN	H	L	X	X	L	Open	Open		L	Open	Open		L	Open	Open
Enter Sleep	VIN	H	X	X	5 pulse	L	Open	Open	T5	↑	Open	Open	0	H	Open	Open
	VIN	X	H	X	5 pulse	L	Open	Open	T5	↑	Open	Open	0	H	Open	Open
	VIN	X	X	X	H	L	Open	Open		L	Open	Open		L	Open	Open
	VIN	X	X	X	L	L	Open	Open		L	Open	Open		L	Open	Open
	VIN	X	X	X	<5 pulse	L	Open	Open		L	Open	Open		L	Open	Open
Exit Sleep	VIN	H	X	L	X	H	Open	Open		H	Open	Open		H	Open	Open
	VIN	X	X	H	X	H	Open	Open	T7=50m	H	Open	Open	T_{FALL}	L	Open	Open
	VIN	L	X	X	X	H	Open	Open	T6=2	H	Open	Open		L	Open	Open

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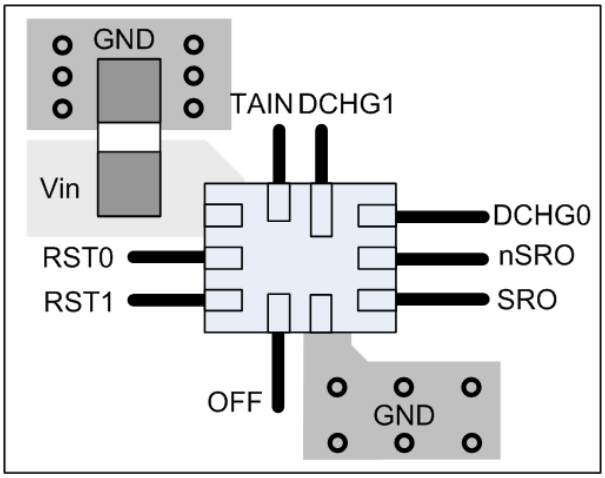
APPLICATION INFORMATION

Selecting the Input Capacitor

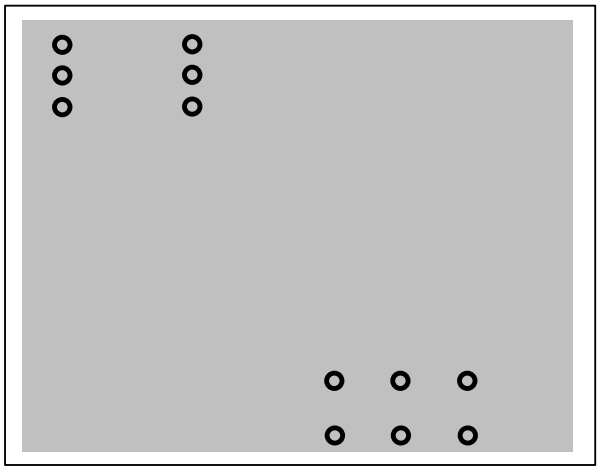
Input capacitors are important for protecting the MP6412 from input voltage spikes when a V_{IN} hot-plug occurs. 0603 ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 1µF 0603 input capacitor is sufficient.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 19.



Top Layer



Bottom Layer

Figure 19: Recommended Layout

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TYPICAL APPLICATION CIRCUIT

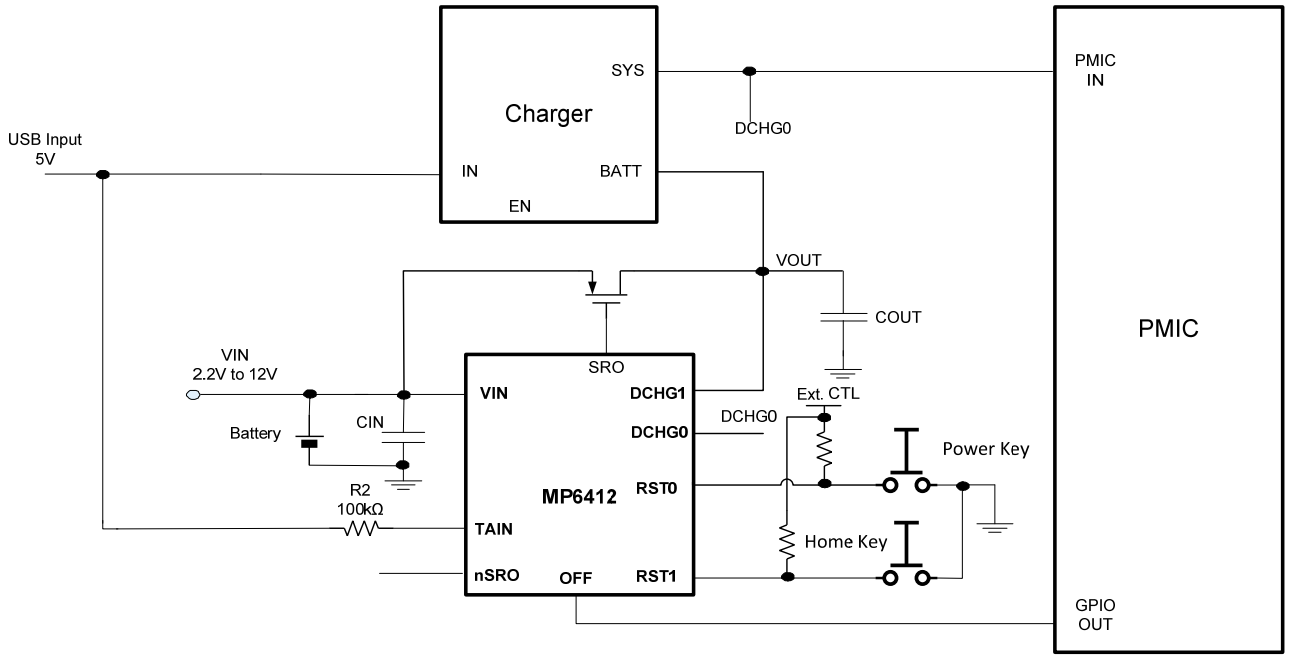

Figure 20: Typical Application Circuit

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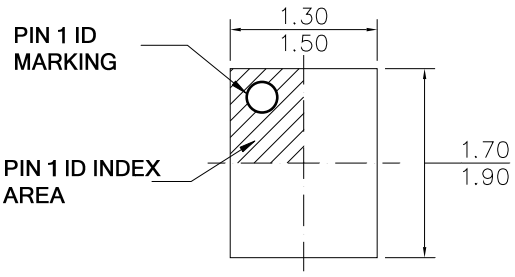
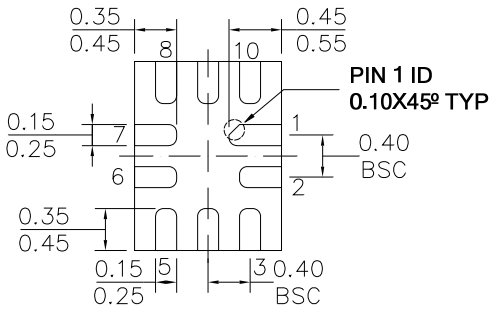
PACKAGE INFORMATION

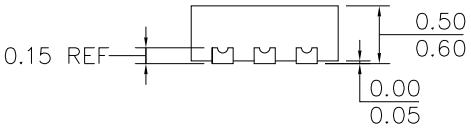
UTQFN-10 (1.4mmx1.8mm)



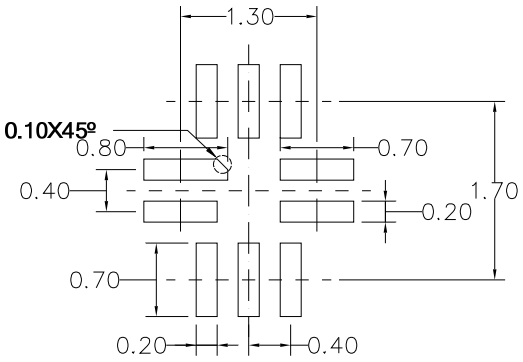
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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