MP6233

3.3V/5V, Dual-Channel 1.5A Current-Limited Power Distribution Switch

The Future of Analog IC Technology

DESCRIPTION

The MP6233 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP6233 analog switch includes an 85mΩ power MOSFET switch. It is available with guaranteed current limits, making it ideal for load switching applications. The MP6233 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP6233 is available in MSOP8E package.

FEATURES

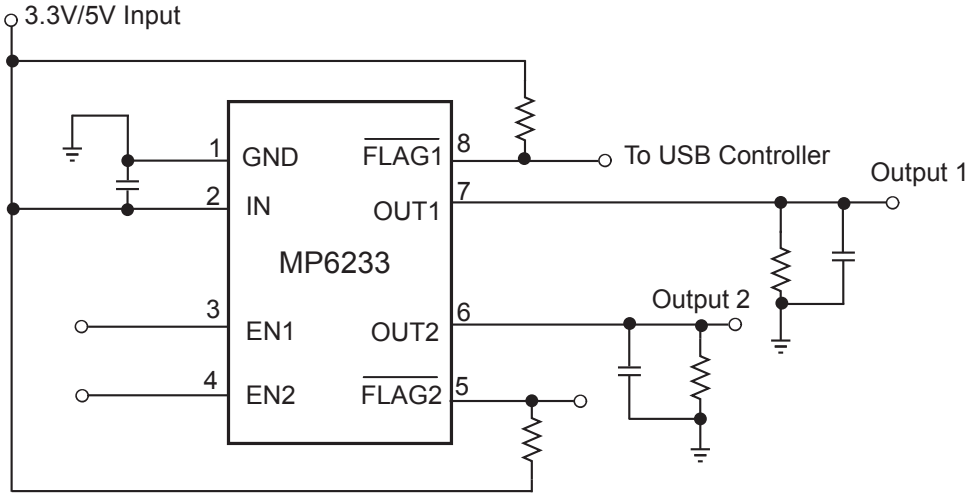
- 1.5A Continuous Current
- 2.7V to 5.5V Supply Range
- 140uA Quiescent Current
- 85mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- UL Recognized: E322138

APPLICATIONS

- Portable GPS Device
- Notebook PC
- LCD TV
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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TYPICAL APPLICATION



DUAL-CHANNEL

UL Recognized Component

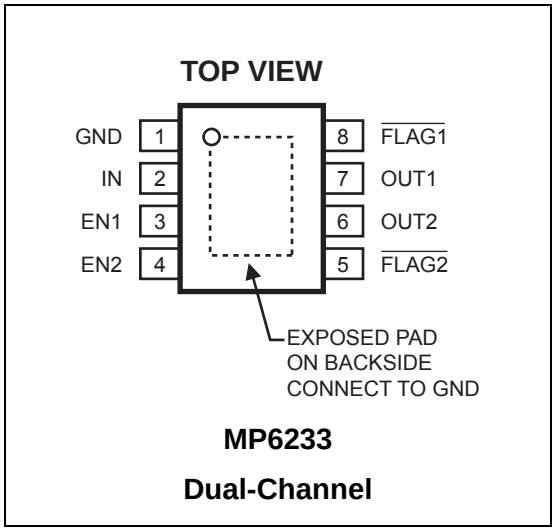
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ORDERING INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T_A=25C	Package	Top Marking	Temperature
MP6233DH	Active High	Dual	1.5A	2.3A	MSOP8E	6233D	–40°C to +85°C

For Tape & Reel, add suffix –Z (eg. MP6233DH–Z); For RoHS Compliant Packaging, add suffix –LF; (eg. MP6233DH–LF)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.3V to +6.0V
EN, FLAG, OUT to GND .....-0.3V to +6.0V
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C
Operating Temperature..... –40°C to +85°C

Thermal Resistance (2)	θ_{JA}	θ_{JC}
MSOP8E	55	12... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (3)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	One Channel Enabled, I_{OUT}=0, One Switch ON		90	120	μA
Supply Current	Both Channels Enabled, I_{OUT}=0, Both Switch ON		140	160	μA
Shutdown Current	Device Disable, V_{OUT}=float, V_{IN}=5.5V		1		μA
Off Switch Leakage	Device Disable, V_{IN}=5.5V		1		μA
Current Limit		1.6	2.3	3	A
Trip Current	Current Ramp (slew rate≤100A/s) on Output		2.7	3.5	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	I_{OUT}=100mA and-40°C<T_A< 85°C		85	130	mΩ
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.4	V
FLAG Output Logic Low Voltage	I_{SINK}=5mA			0.4	V
FLAG Output High Leakage Current	V_{IN}=V_{FLAG}=5.5V			1	μA
Thermal Shutdown			140		°C
Thermal Shutdown Hysteresis			20		°C
V_{OUT} Rising Time, Tr	V_{IN}=5.5V, CL=1uF, RL=5Ω		0.9		ms
	V_{IN}=2.7V, CL=1uF, RL=5Ω		1.7		ms
V_{OUT} Falling Time, Tf	V_{IN}=5.5V, CL=1uF, RL=5Ω			0.5	ms
	V_{IN}=2.7V, CL=1uF, RL=5Ω			0.5	ms
Turn On Time, Ton	C_L=100μF, RL=5Ω			3	ms
Turn Off Time, Toff	C_L=100μF, RL=5Ω			10	ms
FLAG Deglitch Time		4	8	15	ms
ENx Input Leakage		-1			μA
Reverse Leakage Current	OUTX=5.5V, IN=GND		0.2		μA

NOTE:

3) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

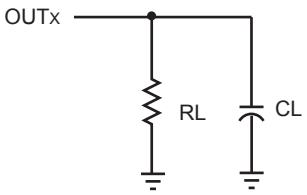
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PIN FUNCTIONS

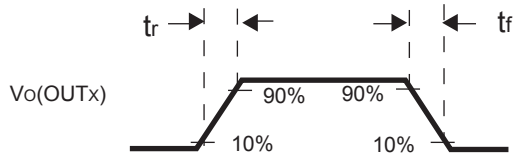
MSOP8E	Name	Description
1	GND, Exposed Pad	Ground. Connect exposed pad to GND plane for optimal thermal performance.
2	IN	Input Voltage. Accepts 2.7V to 5.5V input.
3	EN1	Active High
4	EN2	Active High
5	$\overline{\text{FLAG2}}$	IN-to-OUT2 Over-current, active-low output flag. Open-Drain.
6	OUT2	IN-to-OUT2 Power-Distribution Switch Output.
7	OUT1	IN-to-OUT1 Power-Distribution Switch Output
8	$\overline{\text{FLAG1}}$	IN-to-OUT1 Over-current, active-low output flag. Open-Drain.

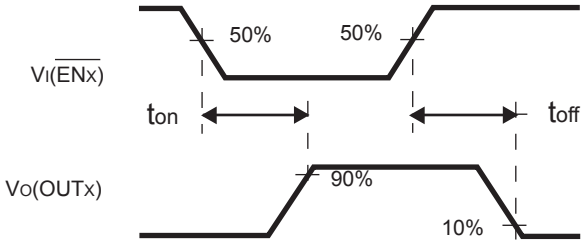
TYPICAL PERFORMANCE CHARACTERISTICS

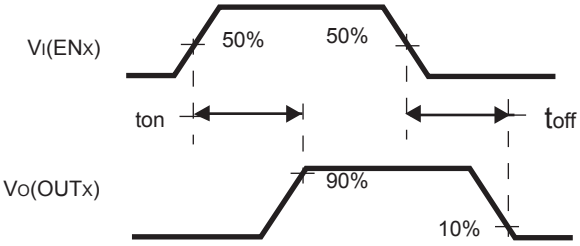
T_A = +25ºC, unless otherwise noted.



TEST CIRCUIT







VOLTAGE WAVEFORMS

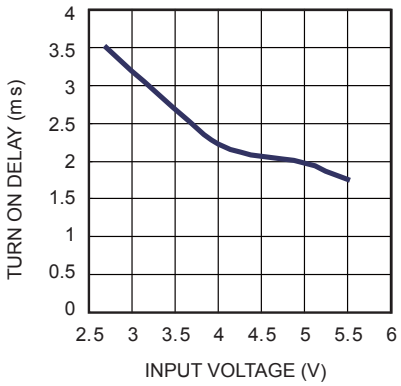
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TYPICAL PERFORMANCE CHARACTERISTICS

C_L = 2.2µF, V_{IN} = 5.5V, T_A = +25ºC, unless otherwise noted.

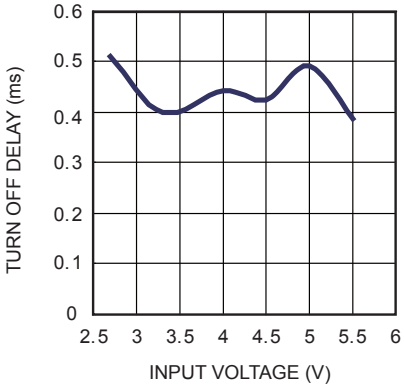
Turn on Delay vs. Input Votage

V_{EN}=5V, R_L=3.3Ω



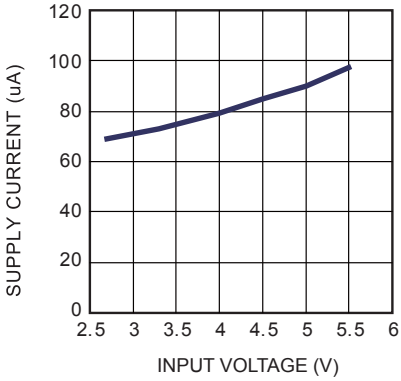
Turn off Delay vs. Input Votage

V_{EN}=5V, R_L=3.3Ω



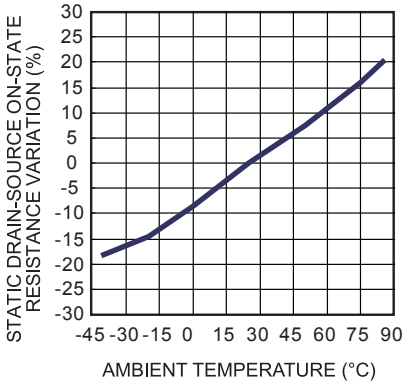
Supply Current, Output Enabled vs. Input Voltage

V_{EN}=5V



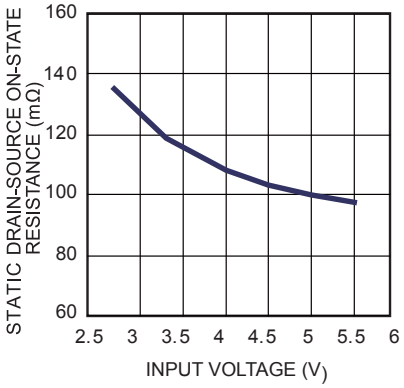
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

V_{IN}=5V, I_O=0.1A



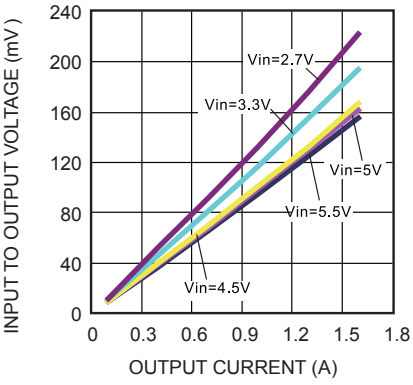
Static Drain-Source On-State Resistance vs. Input Voltage

V_{EN}=5V, ,I_{OUT}=1.5A



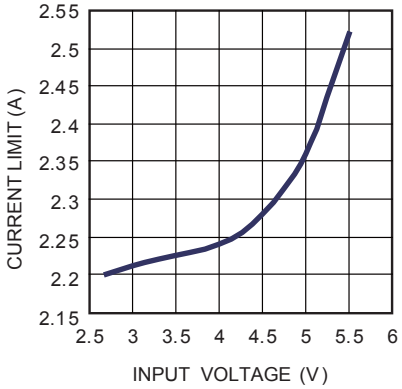
Input to Output Voltage vs. Load Current

V_{EN}=5V



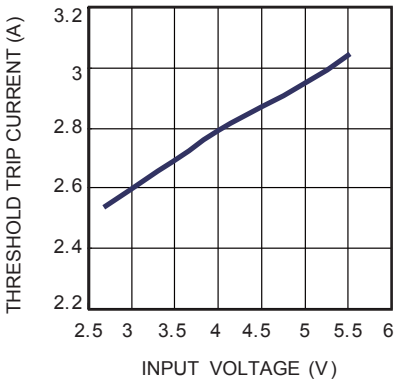
Current Limit vs. Input Voltage

V_{EN}=5V



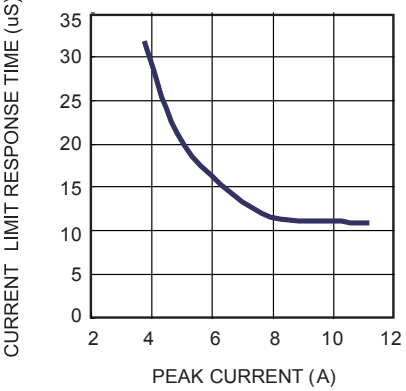
Threshold Trip Current vs. Input Voltage

V_{EN}=5V



Current Limit Response vs. Peak Current

V_{EN}=5V



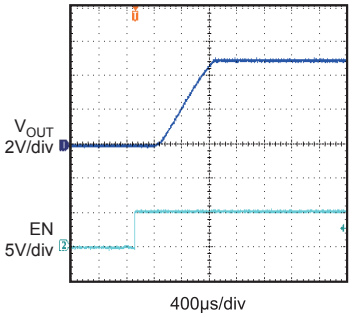
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.5V , T_A = +25ºC, unless otherwise noted. *(continued)*

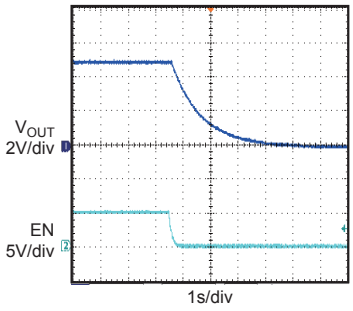
Turn On Delay and Rise Time with 0.1uF Load

V_{EN}=5V,C_L=0.1uF



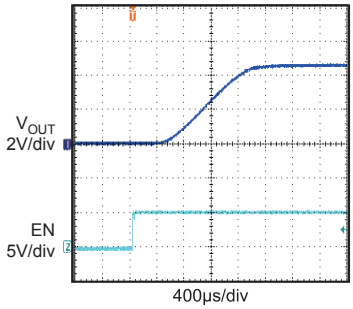
Turn Off Delay and Fall Time with 0.1uF Load

V_{EN}=5V,C_L=0.1uF



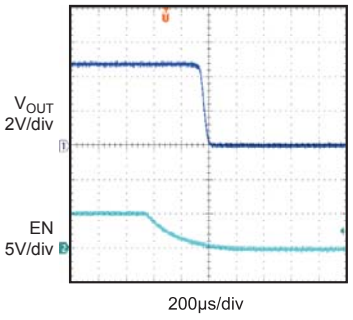
Turn On Delay and Rise Time

V_{EN}=5V,R_L=3.3Ω,C_L=2.2uF



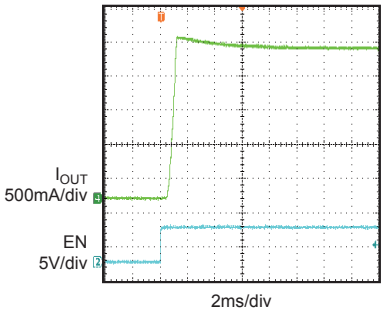
Turn Off Delay and Fall Time

V_{EN}=5V,R_L=3.3Ω,C_L=2.2uF



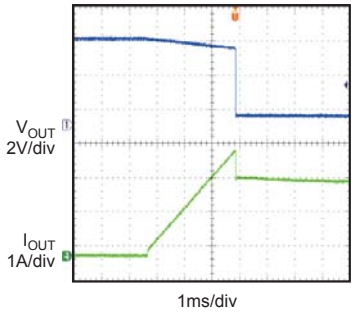
Short Circuit Current, Device Enabled into Short

V_{EN}=5V,C_L=2.2uF



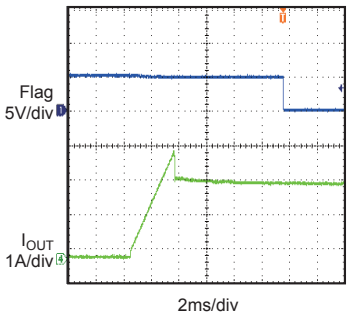
Threshold Trip Current with Ramped Load on Enabled Device

V_{EN}=5V,C_L=2.2uF



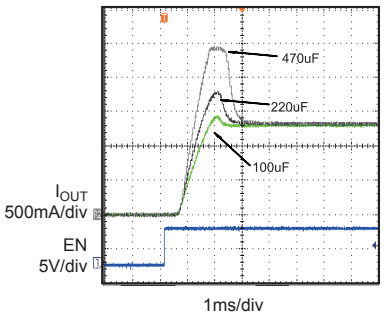
Ramped Load on Enabled Device

V_{EN}=5V,CL=2.2uF



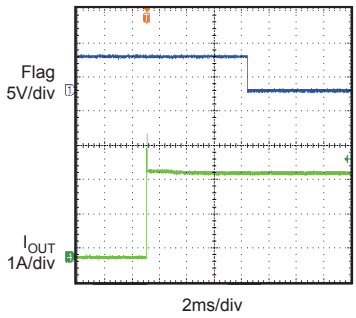
Inrush Current with Different Load Capacitance

R_L=3.3Ω,V_{EN}=5V,
Start up by EN



1Ω Load Connected to Enabled Device

V_{EN}=5V,C_L=2.2uF



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FUNCTION BLOCK DIAGRAM

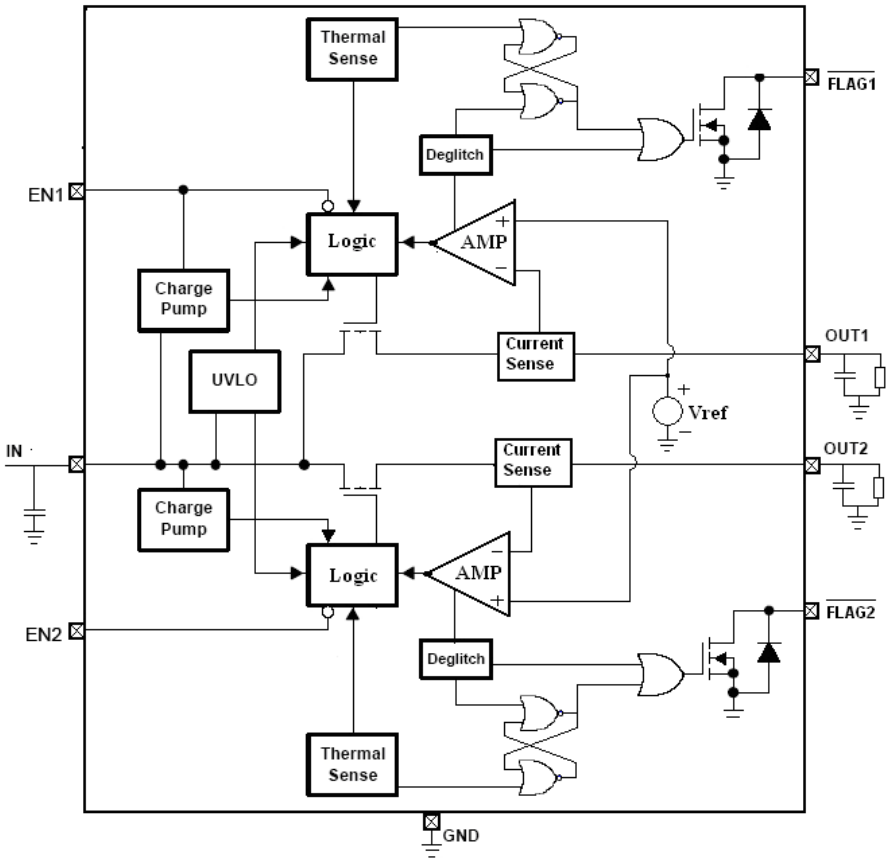


Figure1—Functional Block Diagram

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP6233 switches into to a constant-current mode (current limit value). MP6233 will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the device is enabled or input applied. MP6233 detects the short or overload and immediately switches into a constant-current mode.
2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP6233 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or a voltage lockout.

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Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temp. is internally monitored until the thermal limit is reached. Once this temp. is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP6233 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

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APPLICATION INFORMATION

Power-Supply Considerations

Over 10μF capacitor between IN and GND is recommended.

This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

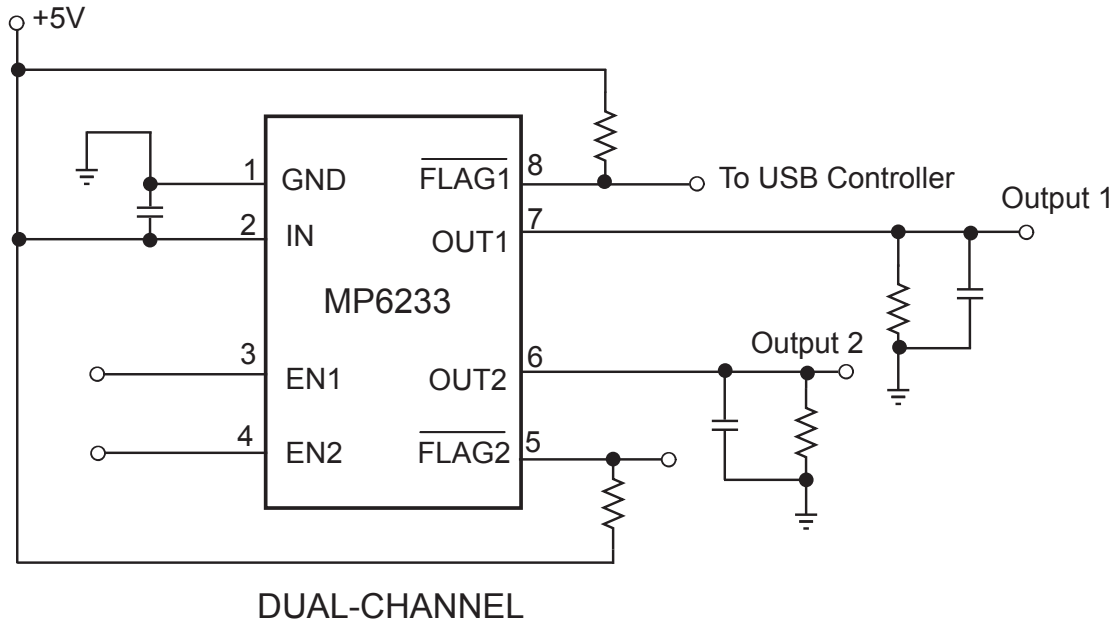
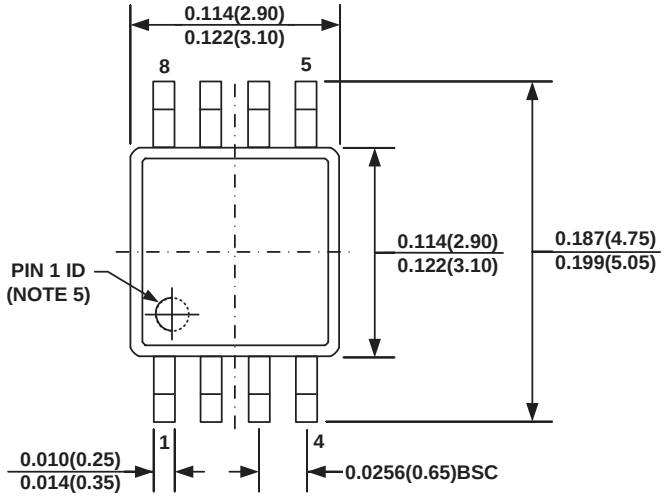


Figure2—Application Circuit

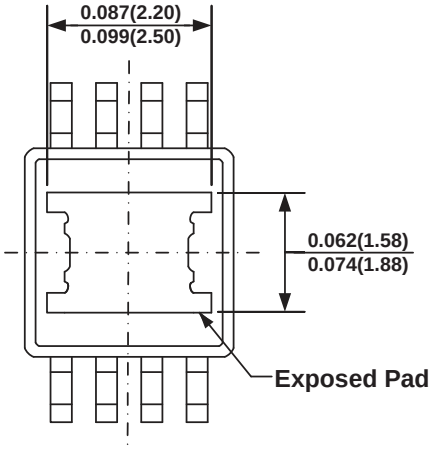
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PACKAGE INFORMATION

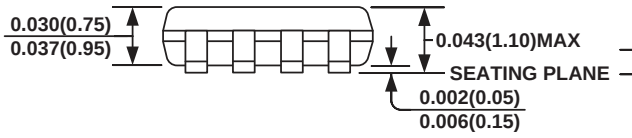
MSOP8E (EXPOSED PAD)



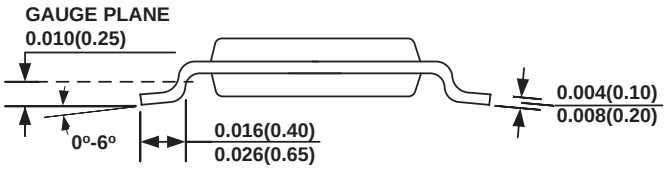
TOP VIEW



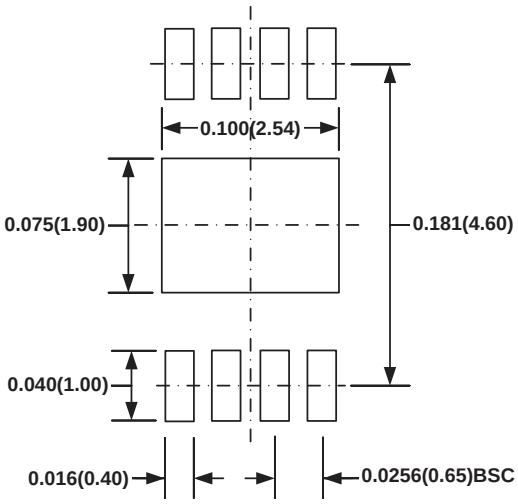
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
7) DRAWING IS NOT TO SCALE.

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