MP5032

QC 3.0 Controller with Integrated Current-Limit Switch

DESCRIPTION

The MP5032 integrates a USB current-limit switch and charging port identification circuit. The MP5032 achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limit programmable. The MP5032 supports DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and quick charge specification (QC 3.0) without the need for external user interaction.

The MP5032 provides linear line drop compensation.

Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

The MP5032 requires a minimal number of readily available, standard, external components to complete the USB switch and charging mode auto-detection solution. The MP5032 is available in an 8-pin TSOT23 package.

FEATURES

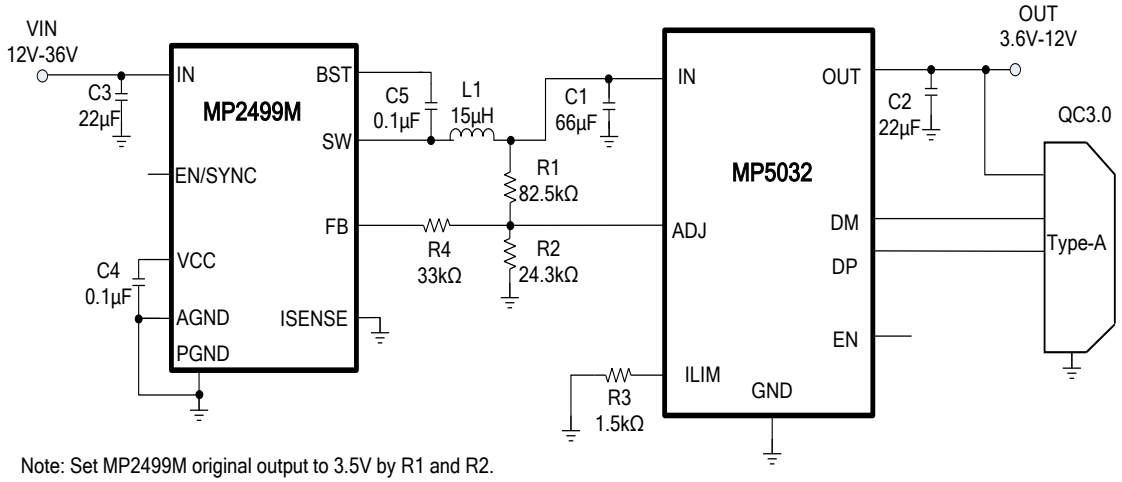
- Wide 3.6V to 14V Operating Input Voltage Range
- Supports QC 3.0 (3.6V - 12V_{OUT}) and DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- Line Drop Compensation for 5V Output
- Fairly Constant Power Limit
- 32mΩ Low $R_{DS(ON)}$ Power MOSFET
- Input Discharge during High Voltage to Low Voltage Change
- Intelligent Input Over-Voltage Shutdown Protection
- Compatible with Buck and Boost Converters
- Available in a TSOT23-8 Package

APPLICATIONS

- USB Power Supplies
- Automotive Cigarette Lighter Adapters
- Power Banks

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TYPICAL APPLICATION



Note: Set MP2499M original output to 3.5V by R1 and R2.

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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5032GJ	TSOT23-8	*See Below*

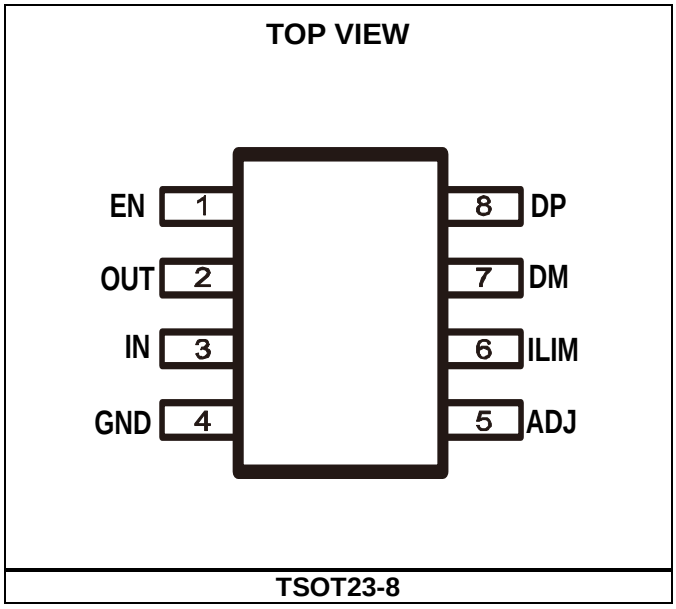
* For Tape & Reel, add suffix –Z (e.g.MP5032GJ-Z)

TOP MARKING

|AYBY

AYB: Product code of MP5032GJ
Y: Year code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +16V
Output voltage (V_{OUT}) ..... -0.3V to +16V
All other pins ..... -0.3V to +6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2) (5)
..... 1.89W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.6V to 14V (4)
Output voltage (V_{OUT}) ..... Follow with V_{IN}
Output current (I_{OUT}) ..... Up to 3A
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
TSOT23-8			
EV5032-J-00A (5)	66	23	°C/W
JESD51-7 (6)	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, refer to the Operation section on page 12.
5) Measured on EV5032-J-00A, 2-layer PCB, 58mmx32mm, 2oz copper
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, R_{ILIM} = 1.5kΩ, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO1}	ADJ starts to work	2.7	3.0	3.3	V
UVLO hysteresis	$V_{UVLOHYS1}$			880		mV
Second V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO2}	Power MOSFET turn-on	3.7	3.9	4.1	V
Second UVLO hysteresis	$V_{UVLOHYS2}$			500		mV
EN rising threshold	V_{EN_R}		1.17	1.21	1.25	V
EN hysteresis	V_{EN_HYS}			200		mV
EN auto pull-up current	I_{EN_UP}		7	11.5	16	μA
Shutdown current	I_{Q_STD}	EN = 0, V_{IN} = 5V		280		μA
Supply current	I_Q	V_{IN} = 5V, no load		250	320	μA
USB Power MOSFET						
On resistance	R_{DSON}	V_{IN} = 5V, I_{OUT} = 0.5A, T_J = 25°C		32	40	mΩ
		V_{IN} = 5V, I_{OUT} = 0.5A, T_J = -40°C to 125°C		32	55	
Input discharge resistance	R_{DIS}	V_{IN_OVP} = 6V		72	105	Ω
Soft-start time	T_{SS}	V_{IN} = 5V, no load, V_{OUT} from 10% to 90%		330		μs
Current Limit Set						
USB current limit	I_{LIMIT}	V_{IN} = 5V, V_{OUT} starts to drop	3.05	3.2	3.4	A
		V_{IN} = 9V (QC 2.0, 9V mode or QC 3.0, 3.6V ≤ V_{OUT} < 6.6V), V_{OUT} starts to drop	2.51	2.70	2.89	
		V_{IN} = 12V (QC 2.0, 12V mode or QC 3.0, 6.6V ≤ V_{OUT} < 9.8V), V_{OUT} starts to drop	1.87	2.08	2.29	
Output Voltage Control						
Default V_{IN}	V_{IN_Def1}	I_{OUT} = 0A, T_J = 25°C	5.05	5.10	5.15	V
	V_{IN_Def2}	I_{OUT} = 0A, T_J = -40°C to 125°C	5	5.10	5.2	V
9V_{IN} voltage	V_{IN_9}		8.82	9	9.18	V
12V_{IN} voltage	V_{IN_12}		11.76	12	12.24	V
V_{ADJ} sink current capability		V_{ADJ} = 0.8V	500			μA
Line drop compensation	$V_{IN_5_C}$	I_{OUT} = 2.4A, only 5V_{IN} active		330	440	mV
Protection						
V_{IN} OVP threshold	V_{OV_TH}	V_{IN} rising edge, V_{IN} = 5V	110	115	120	%
		V_{IN} rising edge, V_{IN} = 9V	110	115	120	
		V_{IN} rising edge, V_{IN} = 12V	110	115	120	
V_{IN} OVP Recovery Threshold	$V_{OV_Recovery}$	Reset mode to 5V default	5.35	5.5	5.65	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, R_{ILIM} = 1.5kΩ, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OCP on time of hiccup	T_{HIC_ON}	V_{OUT}<3.5V		2		ms
OCP off time of hiccup	T_{HIC_OFF}			2		s
Shutdown Temperature[8]	T_{STD}			160		°C
Hysteresis[8]	T_{HYS}			35		°C
BC1.2 DCP Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA			50	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM_1.2V}$		200	300	400	kΩ
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = V_{OUT} = 5V	2.5	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM}$		18	22	28	kΩ
Quick Charge 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.25	0.3	0.4	V
DP/DM high voltage	V_{QC_High}		1.8	2	2.2	V
DP output impedance	R_{DP_QC}		250	350	450	kΩ
DM output impedance	R_{DM_QC}		15	20	25	kΩ
DM low glitch time [8]	T_{Glitch_DM}			10		ms
DP high glitch time	T_{Glitch_DP}		1000		1500	ms
Output voltage change glitch time	$T_{Glitch_V_Change}$		20	40	60	ms
Bus voltage step	$V_{BUS_CONT_STEP}$		150	200	250	mV
Time for V_{BUS} to discharge to 5V when DP < 0.6V [8]	T_{V_UNPLUG}				500	ms

NOTES:

7) Guaranteed by over-temperature correlation, not tested in production.

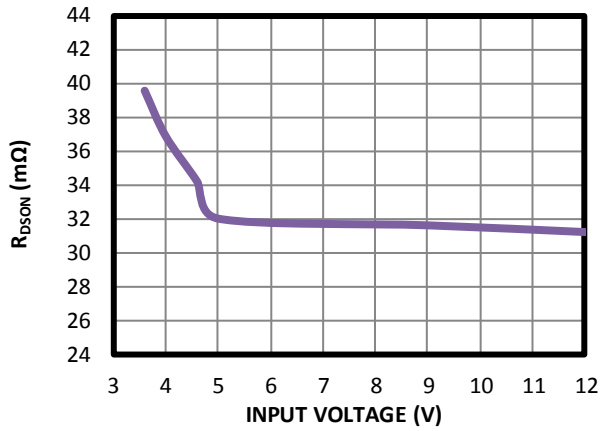
8) Guaranteed by engineering sample characterization.

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TYPICAL CHARACTERISTICS

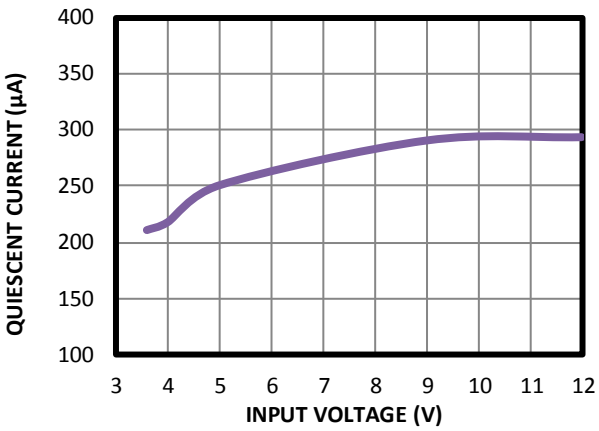
V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted.

$R_{DS(ON)}$ vs. Input Voltage



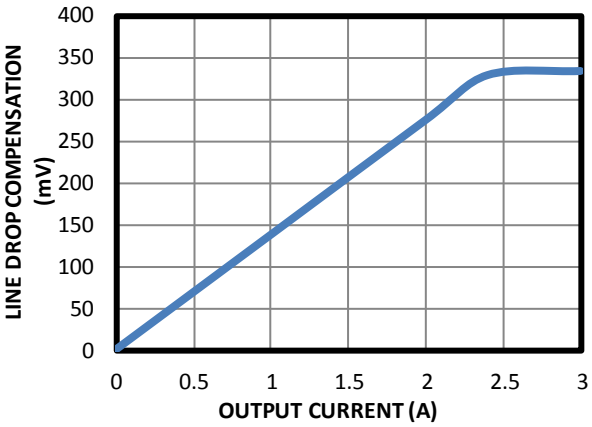
Quiescent Current vs. Input Voltage

EN Float



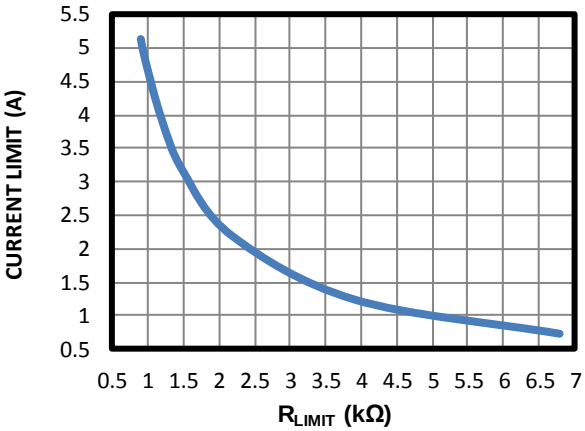
Line Drop Compensation

V_{IN} = 5V Only



Current Limit vs. R_{LIMIT}

V_{IN} = 5V Only



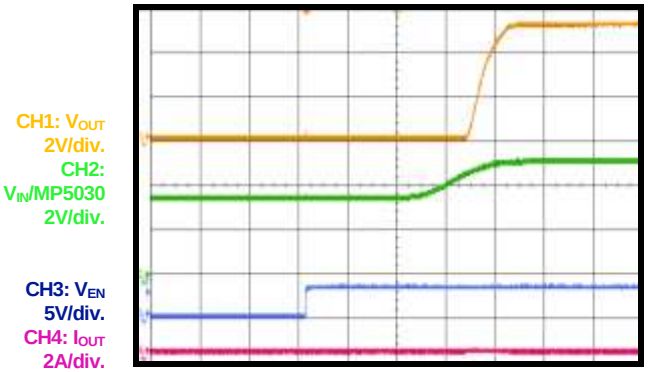
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted.

Start-Up through Enable

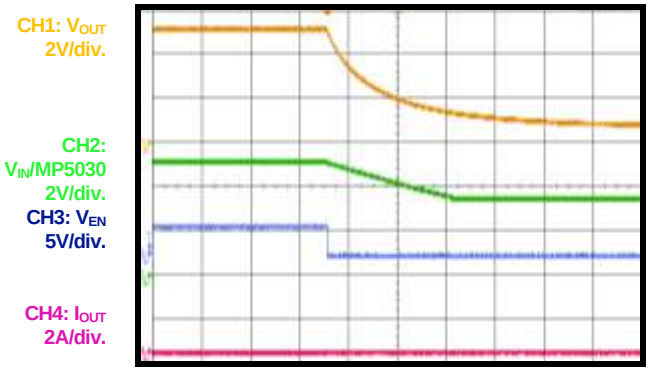
I_{OUT} = 0A



500µs/div.

Shutdown through Enable

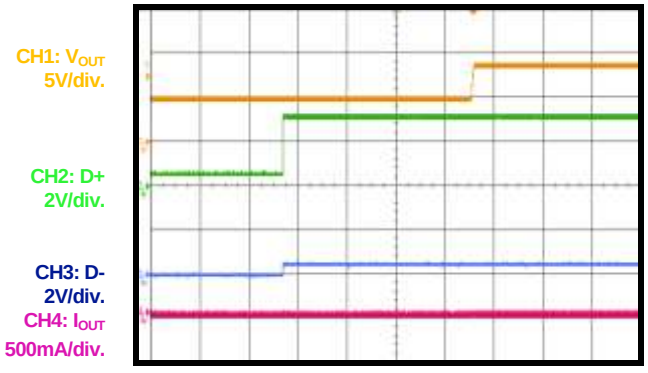
I_{OUT} = 0A



20ms/div.

Mode Transition from 5V to 9V

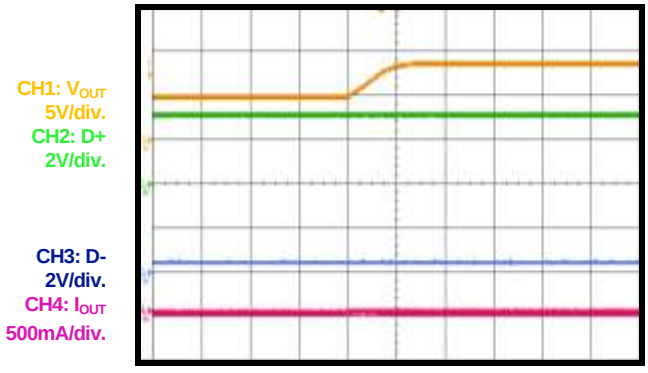
I_{OUT} = 0A, from QC 2.0_5V to 9V



10ms/div.

Mode Transition from 5V to 9V

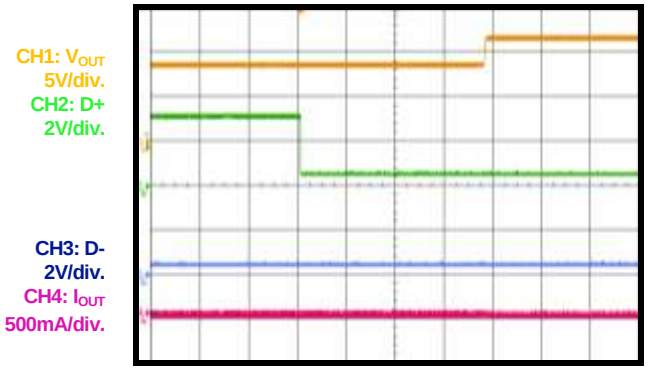
Zoom in 5V to 9V Slew Rate



500µs/div.

Mode Transition from 9V to 12V

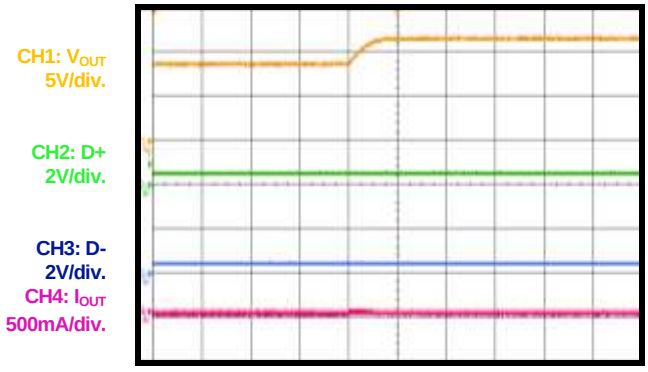
I_{OUT} = 0A, from QC 2.0_9V to 12V



10ms/div.

Mode Transition from 9V to 12V

Zoom in 9V to 12V Slew Rate



500µs/div.

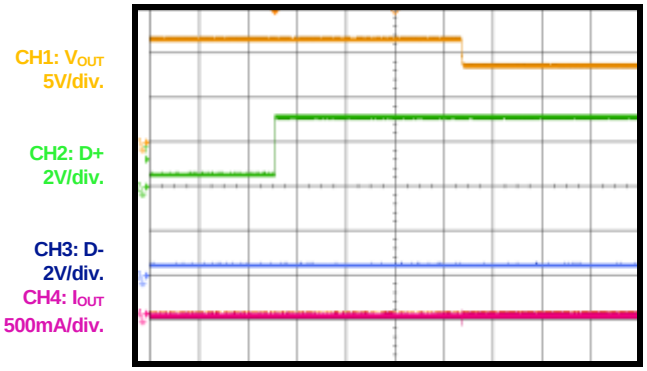
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted.

Mode Transition from 12V to 9V

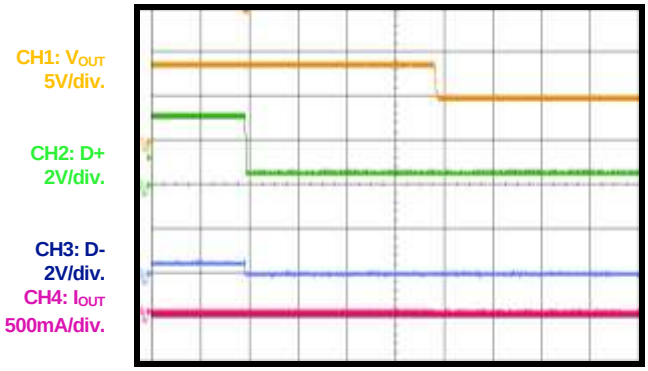
I_{OUT} = 0A, from QC 2.0_12V to 9V



10ms/div.

Mode Transition from 9V to 5V

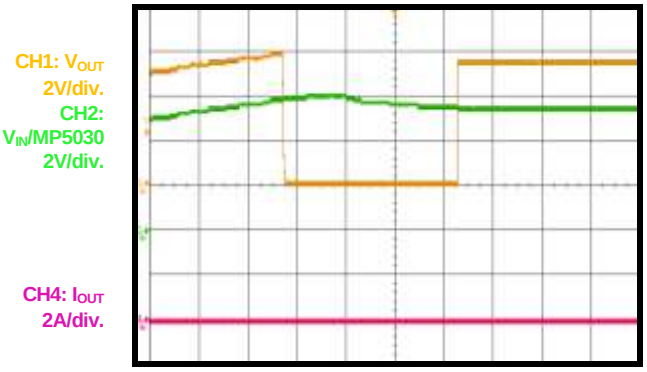
I_{OUT} = 0A, from QC 2.0_9V to 5V



10ms/div.

Input Over-Voltage Protection

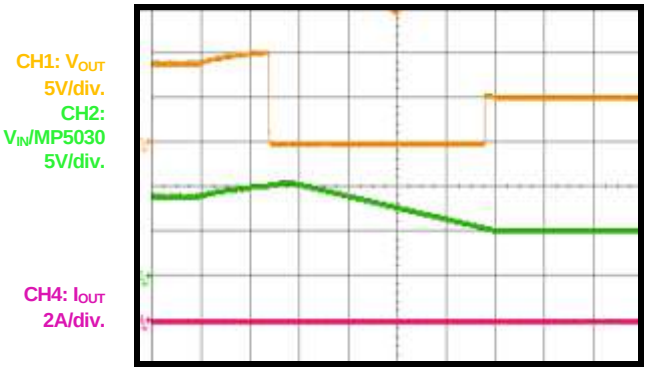
QC 5V Mode, I_{OUT} = 0A



1s/div.

Input Over-Voltage Protection

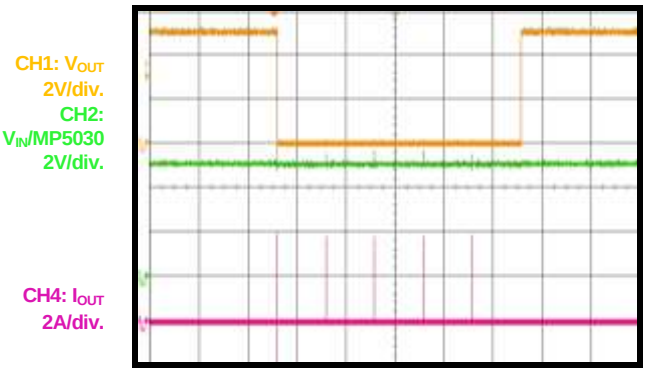
QC 9V Mode, I_{OUT} = 0A



2s/div.

Short-Circuit Protection Entry and Recovery

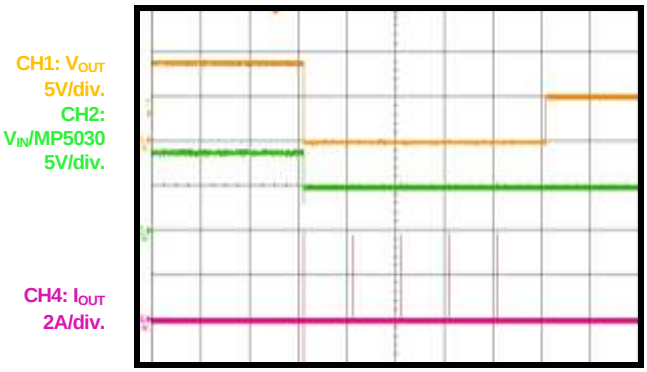
V_{IN} = 5V, I_{OUT} = 0A



2s/div.

Short-Circuit Protection Entry and Recovery

V_{IN} = 9V, I_{OUT} = 0A



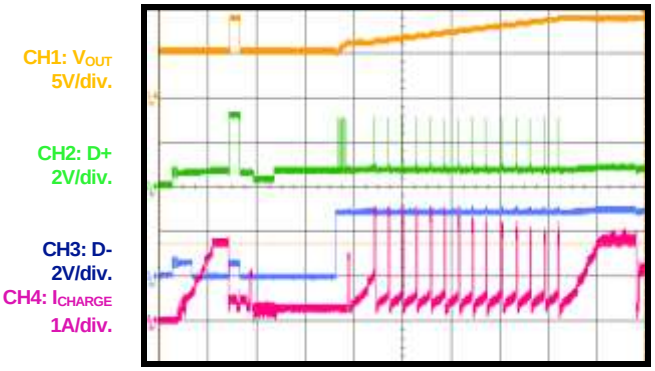
2s/div.

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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted.

QC 3.0 Device Charging Test



2s/div.

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PIN FUNCTIONS

Package Pin #	Name	Description
1	EN	**Enable control.** EN has an internal auto pull-up current to 5V. Float EN or apply a logic high voltage to enable the IC. Pull EN to logic low to disable the IC.
2	OUT	**Output of USB current limit switch.**
3	IN	**Supply voltage.**
4	GND	**Ground.**
5	ADJ	**Output voltage adjustment.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage. ADJ also supports line drop compensation.
6	ILIM	**Set the current limit level.** Place a resistor between ILIM and GND to achieve a high-accuracy current limit. The current limit threshold varies versus the output voltage to maintain a fairly constant output power limit.
7	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
8	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices.

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BLOCK DIAGRAM

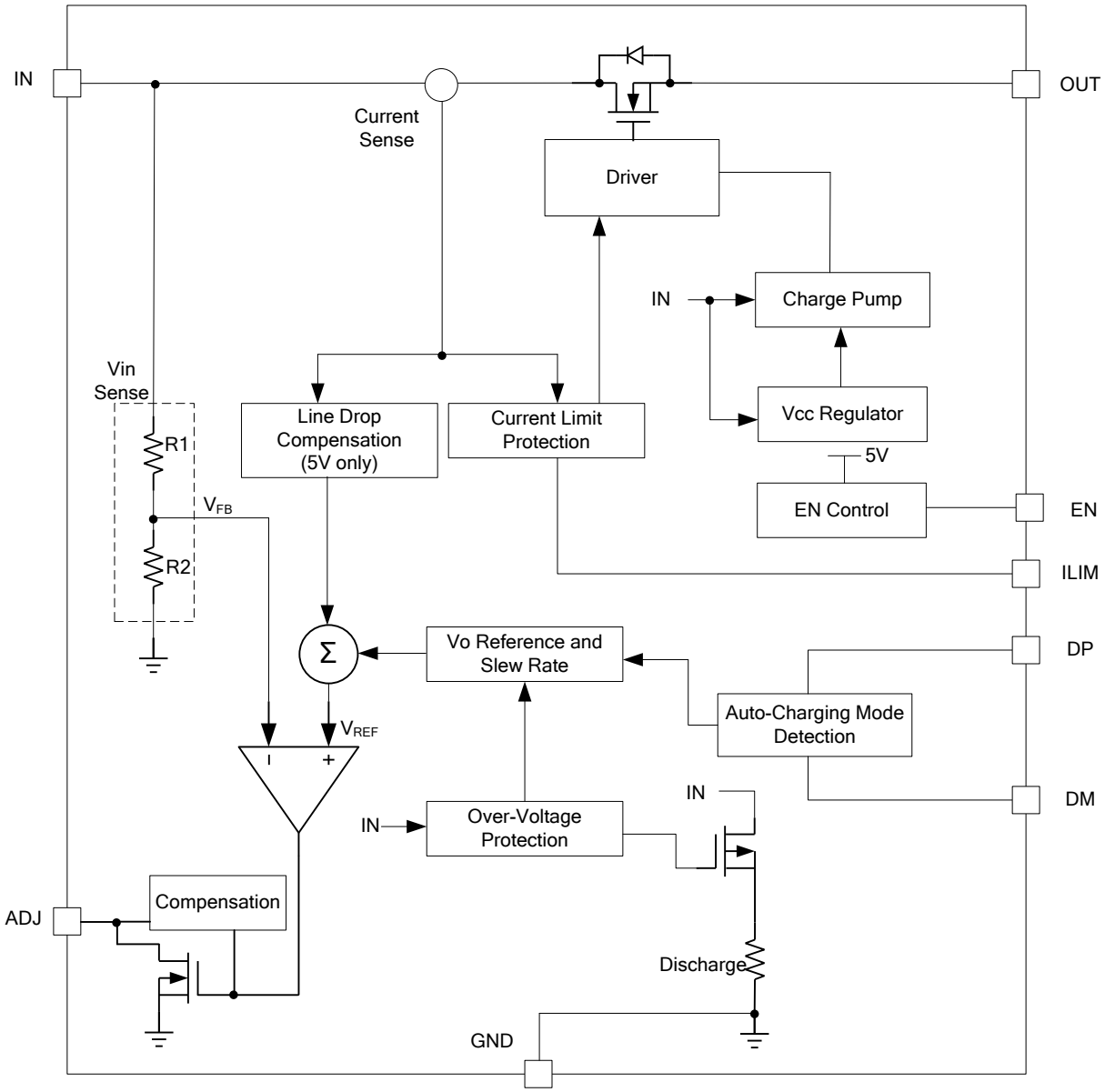


Figure 1: Functional Block Diagram

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OPERATION

The MP5032 integrates a USB current-limit switch and charging port identification circuit. The MP5032 achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limited with an adjustable current-limit threshold. The MP5032 supports the latest quick-charge specification (QC 3.0) and is backwards-compatible with QC 2.0. The MP5032 also supports DCP schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MP5032 provides line drop compensation for a 5V output. Fault condition protection includes hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

Operation Supply Voltage

The MP5032 has a two-stage input voltage threshold. The first threshold is around 3V, and the second threshold is the under-voltage lockout (UVLO) of the power MOSFET. When V_{IN} is higher than the first threshold, the MP5032's ADJ block starts working and sinks a current to adjust the upstream regulator's output to an accurate 5.1V. Afterward, the MP5032 can enable the power MOSFET to fully enter the working state.

Under-Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The MP5032's second UVLO comparator monitors the input voltage. Once the input voltage is higher than 3.9V, the power MOSFET starts to turn on with a controlled slew rate.

Internal Soft Start (SS)

An internal soft start prevents the output voltage from inrush current and overshooting during start-up.

QC Mode Voltage Transition - Class A

If the downstream device of the MP5032 supports the QC specification, the MP5032 can require a output voltage higher than 5V by DM and DP communication. If a higher USB bus voltage is required, ADJ must be used. ADJ is usually connected to the feedback pin of the upstream voltage converter. After the handshake, the MP5032 sinks a controlled current by ADJ gradually to adjust the V_{OUT} to 9V/12V or another voltage 200mV step-by-step. Because of smart controller mode, only one ADJ pin can be set to a different high voltage that meets QC specification. The output voltage transition is smooth and has no undershoot or overshoot (see Figure 2 and Table 1).

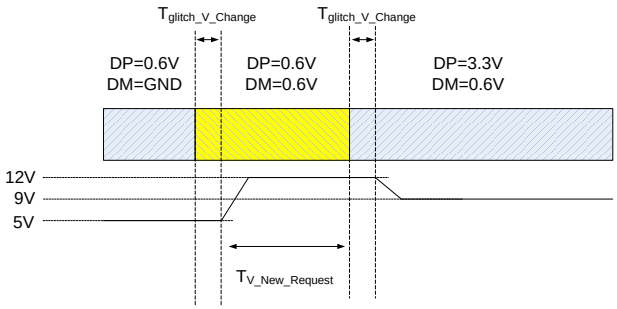


Figure 2: QC Mode Transition

Table 1: QC Mode Definition

Portable Device		USB Bus Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6V - 12V/200mV step according to QC 3.0
3.3V	3.3V	No action
0.6V	GND	5V

When the downstream device is removed, the output voltage returns to the default 5V automatically. The input-to-ground discharge resistor helps expedite this procedure.

Line Drop Compensation

The MP5032 is capable of compensating for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant 5V load-side voltage. The line drop compensation is only active at 5V V_{IN} while it is disabled under QC 3.0 mode. Line drop compensation is achieved through ADJ. The MP5032 increases the input voltage by 330mV at a 2.4A output current. Refer to the Line Drop Compensation graph in the Typical Performance Characteristics section on page 6.

The ADJ voltage (V_{ADJ}) slowly sinks a controlled current. The line drop compensation amplitude increases linearly as the load current increases.

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In no-load condition, if the input voltage is lower than the typical 5.1V, ADJ sinks a current to regulate the upstream regulator's output voltage to 5.1V. If the input voltage is higher than 5.1V, the MP5032 no longer regulates the input voltage.

Figure 3 shows the typical ADJ usage. The ADJ sink current capability is 500μA. The feedback current through R1 must be less than 500μA. Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{V_{OUT}(V) - V_{FB}(V)}{0.5} \quad (1)$$

Where V_{OUT} is the maximum output voltage to be adjusted to.

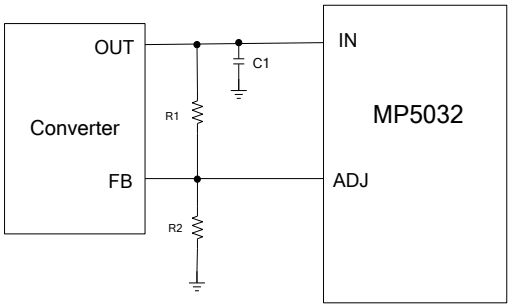


Figure 3: ADJ Configuration

Input Over-Voltage and Discharge

To protect the downstream device from an over-voltage condition, the MP5032 provides an input over-voltage protection (OVP) shutdown function. Since the MP5032 supports QC 3.0 protocol, it has a dynamic OVP threshold.

An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the gate of the internal MOSFET is pulled low quickly, and the power MOSFET is shut down. At the same time, the input-to-ground discharge path is active. When input voltage falls below the typical 5.5V, the MP5032 exits OVP mode.

The OVP shutdown function is blanked during the high-to-low voltage mode change period.

The input-to-ground discharge resistance is always active during the high-to-low voltage mode change period. The discharge path is turned off when FB is lower than 108% * V_{REF} with 20ms of additional delay (see Figure 4).

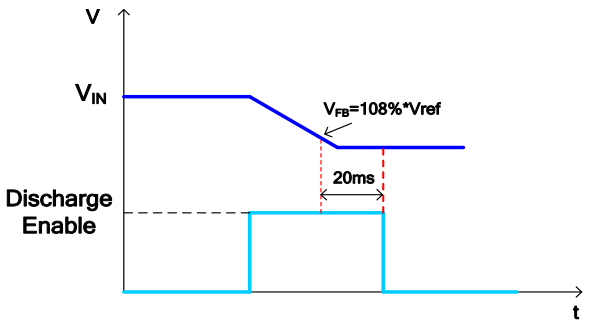


Figure 4: Input Discharge during High Voltage to Low Voltage Transition

QC mode is reset during the OVP rising edge.

Over-Current Protection (OCP)

The MP5032 provides a constant current limit. The current-limit threshold is adjustable by an external resistor.

Once the device reaches its current-limit threshold, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant.

The MP5032 supports different voltage modes. Table 2 shows the over-current threshold for each case. Figure 5 shows an example of the current limit versus the bus voltage curve.

Table 2: OCP Threshold vs. Bus Voltage

USB Bus Voltage	Mode	Over-Current Threshold (V_{LIMIT})
5V (actually 5.1V)	BC1.2 or QC 2.0	4.8
9V	QC 2.0	4.08
12V	QC 2.0	3.12
3.6V - 6.4V	QC 3.0	4.8
6.6V - 9.6V		4.08
9.8V - 12V		3.12

The current-limit threshold can be calculated with Equation (2):

$$I_{LIMIT}(A) = \frac{V_{LIMIT}}{R_{LIMIT}(k\Omega)} \quad (2)$$

If the current limit is set below 1A, the V_{LIMIT} accuracy cannot be guaranteed.

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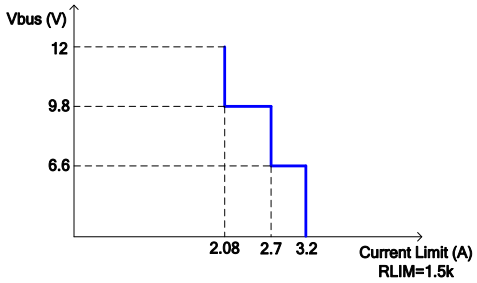


Figure 5: Over-Current Threshold vs. V_{BUS}

For Table 2, the external R_{LIMIT} can set the current-limit threshold. In QC 2.0 mode, the 9V/12V output's current-limit threshold varies accordingly to maintain a fairly constant power limit. In QC 3.0 mode, when 3.6V < V_{OUT} < 6.6V, the MP5032 uses a 5V mode current limit. When 6.6V ≤ V_{OUT} < 9.8V, the MP5032 uses a 9V mode current limit. When V_{OUT} ≥ 9.8V, the MP5032 uses a 12V mode current limit.

If the over-current (OC) is triggered, and V_{OUT} < 3.5V lasts for 2ms, the MP5032 enters hiccup mode. If OC occurs but V_{OUT} > 3.5V, the MP5032 works in constant current (CC) limit mode without hiccup. In this case, V_{OUT} drops while the output current increases slowly. Figure 6 shows the curve of V_{OUT} versus the output current after triggering the 5V current limit.

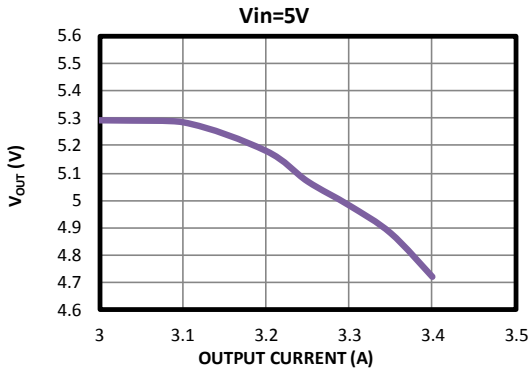


Figure 6: I-V Curve after OC is Triggered

In hiccup mode, the MP5032 turns off the power MOSFET. The hiccup signal resets QC mode to 5V. ADJ starts to change V_{IN} to 5V, and the current-limit threshold changes to the 5V spec. Two seconds (hiccup off-timer) later, the MP5032 restarts to check the OC state. If the OC still remains in 5V mode, the MP5032 follows the previous operation. If the OC does not exist in 5V mode, the MP5032 recovers to operate normally in 5V mode (see Figure 7).

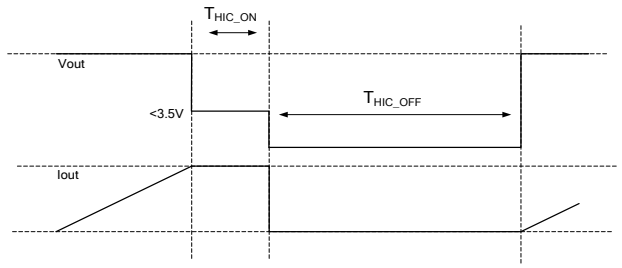


Figure 7: Over-Current Protection

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current-limit level (about 6A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The fast-off response time typical value is 700ns. If the fast-off works, the power MOSFET remains off for 300µs. Afterward, the power MOSFET turns on again. If the part is still in a short-circuit condition, the MP5032 treats this as an over-current condition to enter hiccup mode. After the short-circuit condition is removed, the MP5032 recovers automatically.

Auto Detection

The MP5032 integrates the USB dedicated charging port auto-detect function, which recognizes most mainstream portable devices. It supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Qualcomm quick charge mode 3.0 and 2.0

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 125°C), the chip is enabled again.

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APPLICATION INFORMATION

Selecting the Input Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications. The input capacitor must also consider pre-stage converter stability. The input capacitor of the MP5032 is the output capacitor of the converter. Ensure that the converter is stable with an additional output capacitor.

Selecting the Output Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications.

Selecting the ILIM Resistor

The current limit value can be set by the ILIM resistor. The programmable current limit can be calculated with Equation (2). The minimum current limit should be set higher than the system's full load current.

Selecting the V_{ADJ} Resistor

ADJ has a controlled current sink internally. Through ADJ, the line drop compensation and QC mode transition is achieved. The ADJ sink current capability is 500µA. It is recommended that the pre-side converter use a kΩ level feedback resistor. The current through the high-side feedback resistor must be less than 500µA. There is another V_{ADJ} configuration to limit the maximum output voltage (i.e.: to insert R5 between FB and ADJ). With R5, the maximum output voltage is limited by Equation (3):

$$V_{OUT_MAX}(V) = \frac{R_1 + R_2 // R_5}{R_2 // R_5} \times V_{FB}(V) \quad (3)$$

The required feedback resistor of R1 must be greater than 30kΩ (see Figure 8).

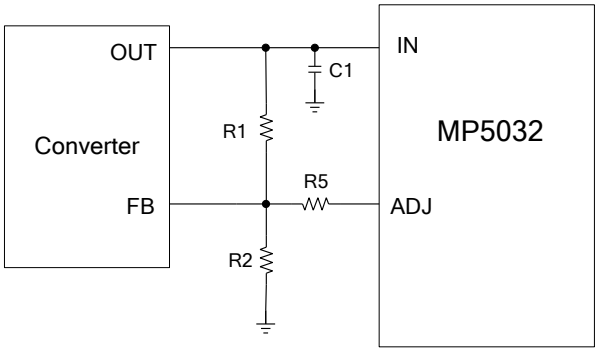


Figure 8: V_{ADJ}-Set Maximum VOUT

Other Considerations

The upstream DC/DC converter must have a current-limit threshold higher than the MP5032's current limit.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 9 and follow the guidelines below.

1. Use short, direct, and wide traces to connect the IC's in/out.
2. Keep the ADJ trace to the upstream converter's FB pin as short as possible.
3. Route the ADJ trace as far from the switching node as possible to avoid noise injection.

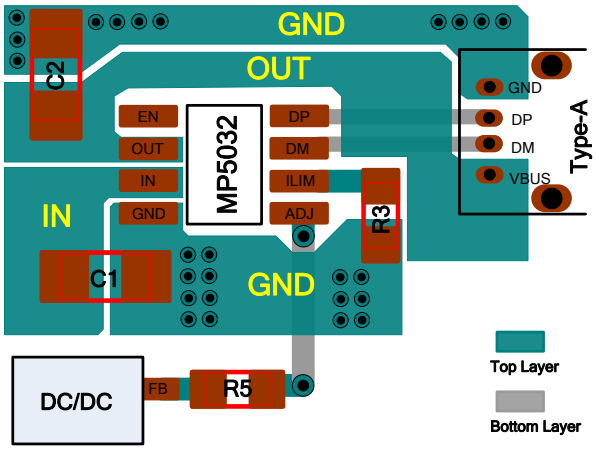


Figure 9: Recommended Layout

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Design Example

Table 3 is a design example following the application guidelines for the given specifications.

Table 3: Design Example

V_{IN} (V)	3.6 - 12
Current Limit (A)	3.2

The detailed application schematic is shown in Figure 10 and Figure 11. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

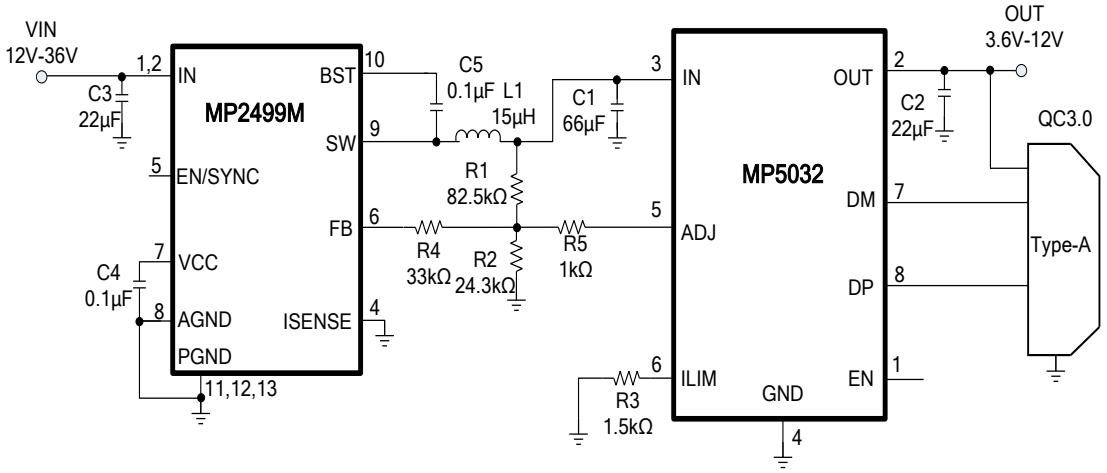


Figure 10: MP5032 + MP2499M for CLA Car Charger

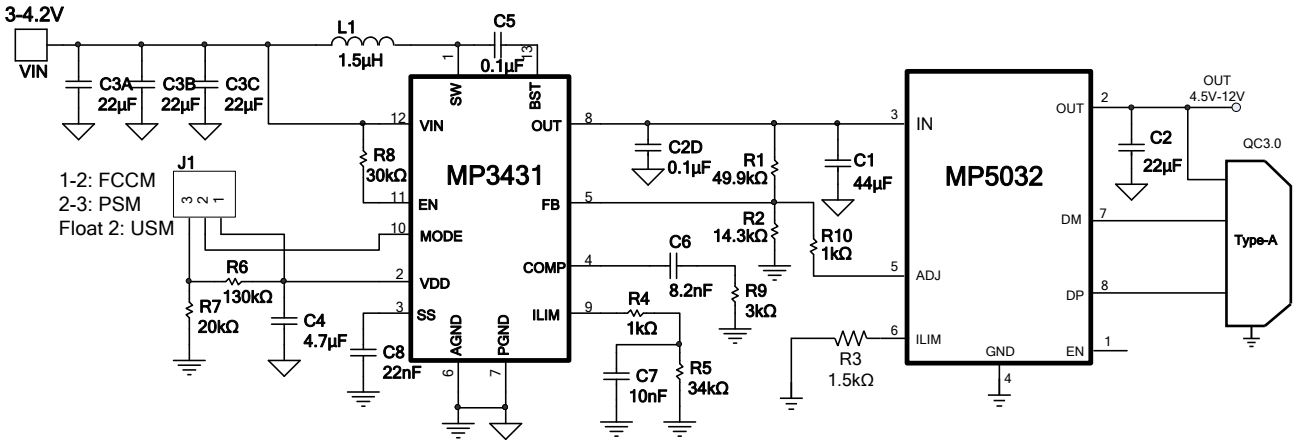
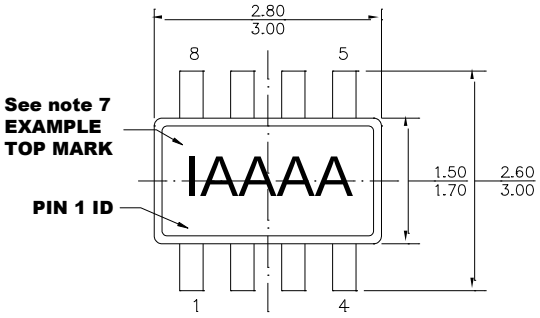


Figure 11: MP5032 + MP3431 for Power Bank

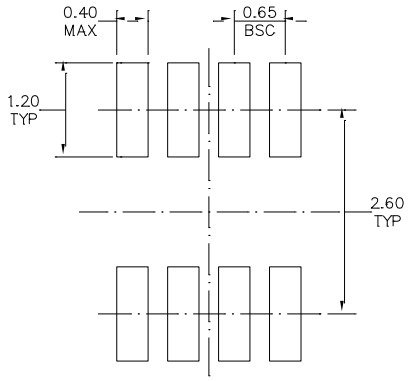
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PACKAGE INFORMATION

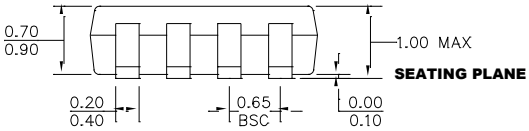
TSOT23-8



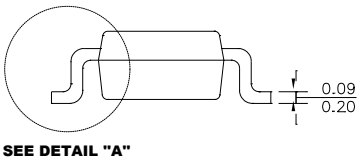
TOP VIEW



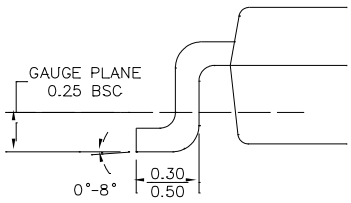
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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