MP5014A

12 V, 5 A, Programmable Current-Limit Switch with Over-Volatge Clamp and Slew-Rate Control in TSOT23-8

The Future of Analog IC Technology

DESCRIPTION

The MP5014A is a protection device designed to protect circuitry on the output (source) from transients on the input (V_{CC}). Also, it protects V_{CC} from undesired shorts and transients coming from the source.

At start-up, the inrush current is limited by restricting the slew rate at the source. The slew rate is controlled by a small capacitor at DV/DT. DV/DT has an internal circuit that allows this pin to float (no connection) and still receive 1 ms ramp time at the source.

The maximum load at the output is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor from I-LIMIT to SOURCE.

An internal charge pump drives the gate of the power device, allowing a very low on-resistance DMOS power FET of just 36 mΩ.

The source is protected from the V_{CC} input going too low or too high. Under-voltage lockout (UVLO) assures that V_{CC} is above the minimum operating threshold before the power device is turned on. If V_{CC} rises above the high output threshold, the source voltage is limited.

FEATURES

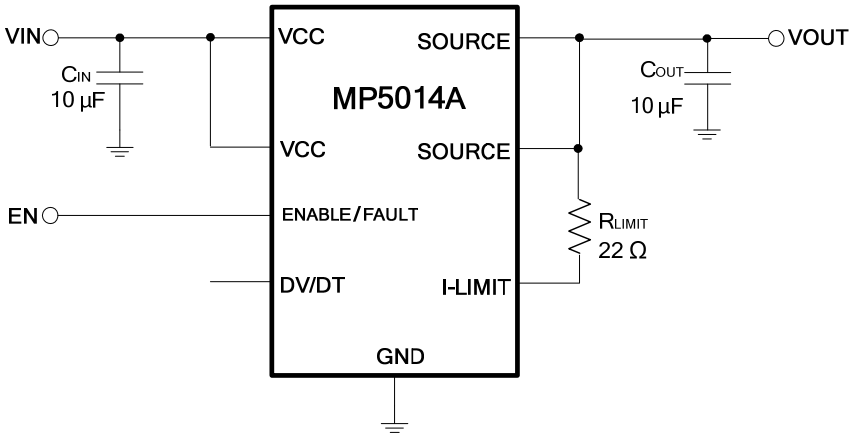
- 10 V to 13.8 V Operating Input Range
- 15 V Typical Output Over-Voltage Clamp
- Absolute Maximum Voltage of 22 V
- Input Under-Voltage Lockout
- Low Inrush Current during Start-Up
- Integrated 36 mΩ Power FET
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit
- Thermal Protection
- TSOT23-8 Package

APPLICATIONS

- Storage (HDDs, SSDs)
- Hot-Swap Systems
- Set-Top Boxes
- Gaming

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5014AGJ	TSOT23-8	*See Below*

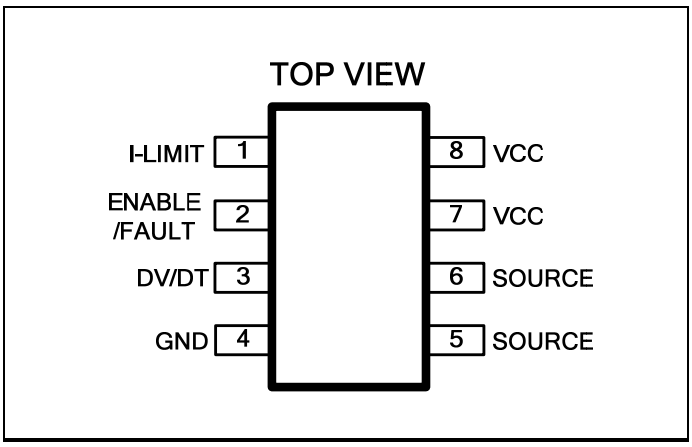
* For Tape & Reel, add suffix –Z (e.g. MP5014AGJ–Z)

TOP MARKING

| AMJY

AMJ: Product code of MP5014AGJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VCC, SOURCE, I-LIMIT.....-0.3 V to 22 V
DV/DT, ENABLE/FAULT.....-0.3 V to 6 V
Storage temperature..... -65°C to +155°C
Continuous power dissipation (T_A = +25°C) (2)
..... 1.25 W
Junction temperature ..... 150°C
Input voltage transient (100 ms) ..... V_{IN} = 25 V

Recommended Operating Conditions (3)

Input voltage operating range…….10 V to 13.8 V
Continuous current 0.5 in^2 pad ..... 4.2 A
For minimum copper, T_A= 80°C ..... 2.3 A
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-8 .....100 ..... 55 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V, R_{LIMIT} = 22 Ω, capacitive load = 10 µF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay time	t_{DLY}	Enabling of chip to I_D = 100 mA with a 1 A resistive load, float DV/DT		0.4		ms
On resistance	R_{DSon}	T_J = 25°C		36		mΩ
		T_J = 85°C (5)		48		
Off-state output voltage	V_{OFF}	V_{CC} = 18 Vdc, V_{ENABLE} = 0 Vdc, R_L= 500 Ω			120	mV
Thermal latch						
Shutdown temperature(5)	T_{SD}			175		°C
Under/over voltage protection						
Output clamping voltage	V_{CLAMP}	Over-voltage protection, V_{CC} = 17 V	13.8	15	16.2	V
Under-voltage lockout	V_{UVLO}	Turn on, voltage goes high	7.7	8.5	9.3	V
Under-voltage lockout (UVLO) hysteresis	V_{HYST}			0.80		V
Current limit(5)						
Hold current	I_{LIM-SS}	R_{LIM} = 22 Ω	2.8	3.8	4.9	A
Trip current	I_{LIM-OL}	R_{LIM} = 22 Ω		5.6		A
DV/DT circuit						
Rise time	T_r	Float DV/DT, output rises from 10% to 90%		1		ms
ENABLE/FAULT						
Low-level input voltage	V_{IL}	Output disabled			0.5	V
Intermediate level input voltage	$V_{I (INT)}$	Thermal fault, output disabled	0.82	1.4	1.95	V
High-level input voltage	V_{IH}	Output enabled	2.5			V
High-state maximum voltage	$V_{I (MAX)}$			5		V
Low-level input current (source)	I_{IL}	V_{ENABLE} = 0 V	15	25	35	µA
Maximum fanout for fault signal		Total number of chips that can be connected for simultaneous shutdown			3	Units
Maximum voltage on ENABLE/FAULT(6)	V_{MAX}				VCC	V
Total device						
Bias current	I_{BIAS}	Device operational		1000	1200	µA
		Enable shutdown		300	400	
		Thermal shutdown		400	500	
Minimum operating voltage for UVLO	V_{MIN}	Enable < 0.5 V			5	V

NOTES:

5) Guaranteed by characterization test.

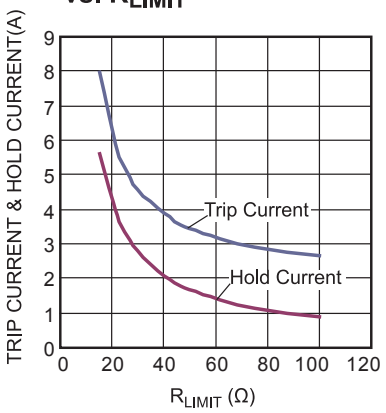
6) Maximum input voltage on ENABLE/FAULT is ≤ 6 V if VCC ≥ 6 V. Maximum input voltage on ENABLE/FAULT is VCC if VCC ≤ 6 V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

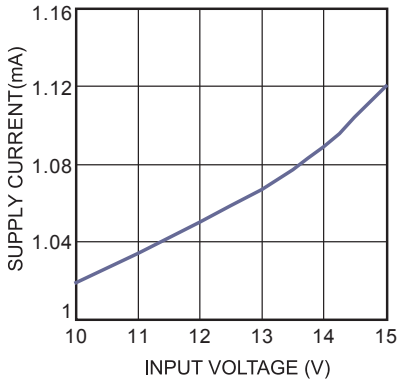
V_{IN} = 12 V, V_{EN} = 5 V, R_{LIMIT} = 22 Ω, C_{OUT} = 10 µF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

Trip Current & Hold Current vs. R_{LIMIT}



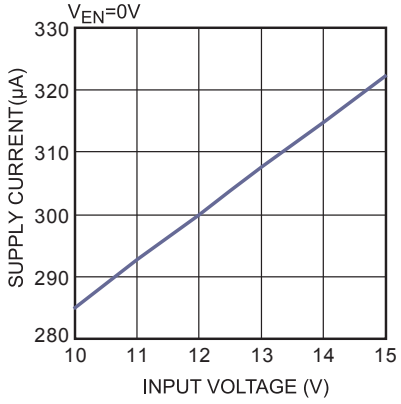
Supply Current, Output Enable vs. Input Voltage

No Load



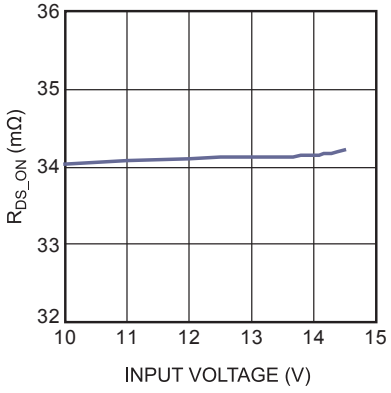
Supply Current, Output Disable vs. Input Voltage

V_{EN}=0V

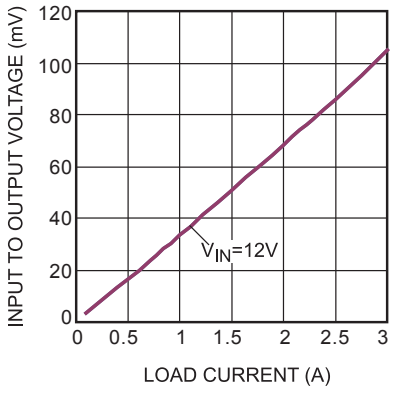


R_{DS_ON} vs. Input Voltage

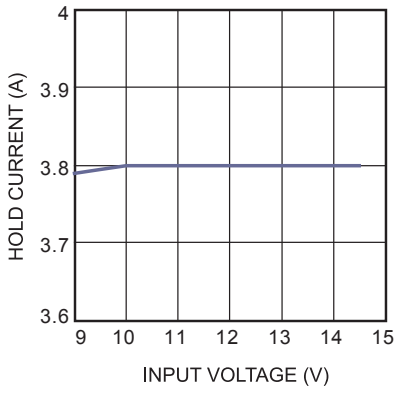
I_{OUT}=0.5A



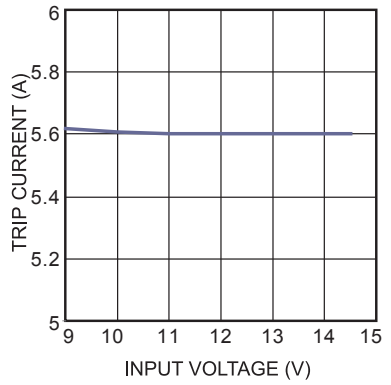
Input to Output Voltage vs. Load Current



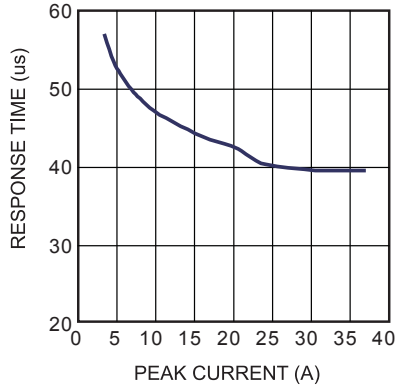
Hold Current vs. Input Voltage



Trip Current vs. Input Voltage



Current Limit Response vs. Peak Current

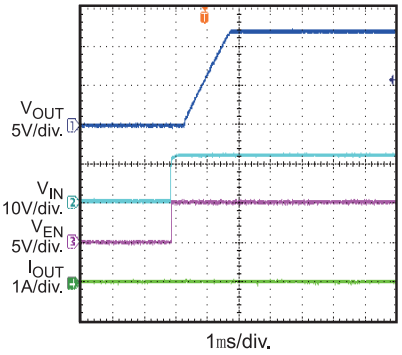


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

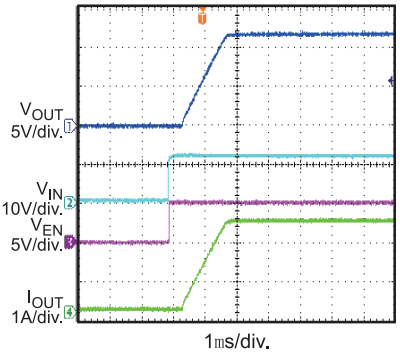
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12 V, V_{EN} = 5 V, R_{LIMIT} = 22 Ω, C_{OUT} = 10 µF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

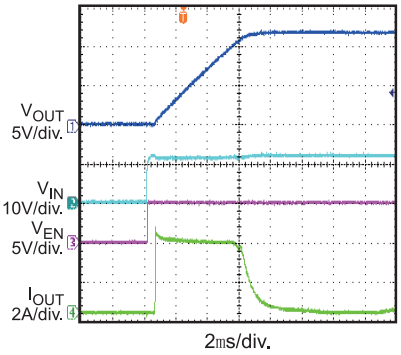
Start-Up through Input Voltage
No Load



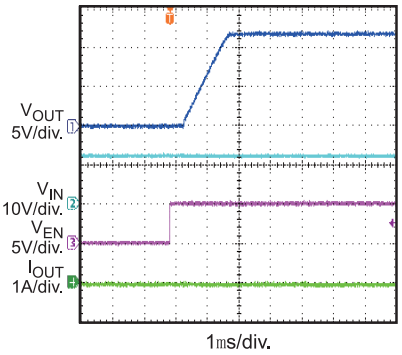
Start-Up through Input Voltage
R_{LOAD} = 5Ω



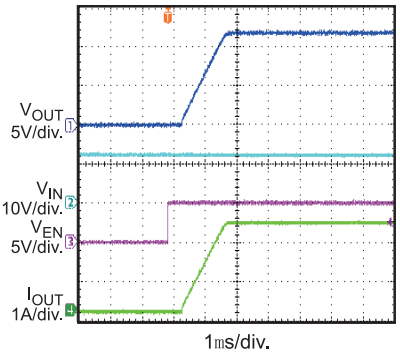
Start-Up through Input Voltage
C_{OUT} = 2200µF



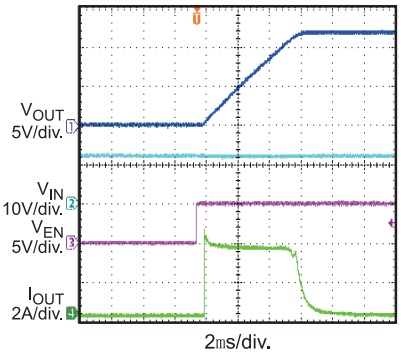
Start-Up through Enable
No Load



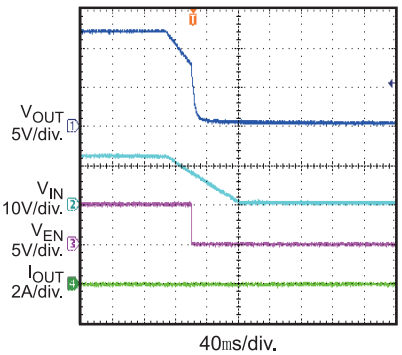
Start-Up through Enable
R_{LOAD} = 5Ω



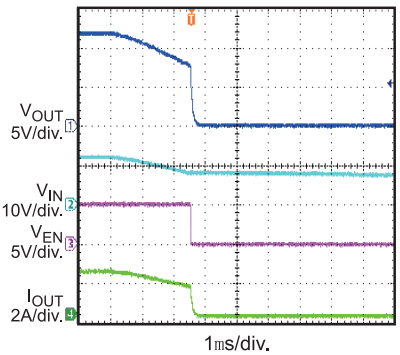
Start-Up through Enable
C_{OUT} = 2200µF



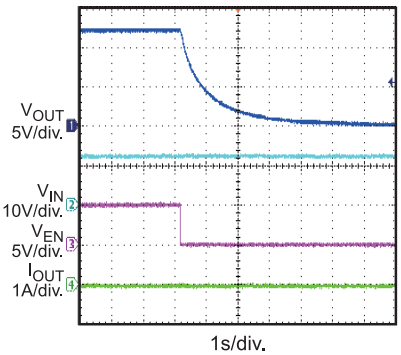
Shutdown through Input Voltage
No Load



Shutdown through Input Voltage
R_{LOAD} = 5Ω



Shutdown through Enable
No Load



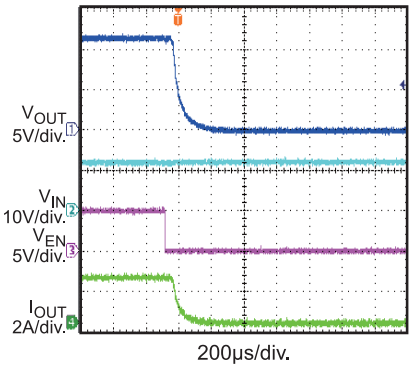
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

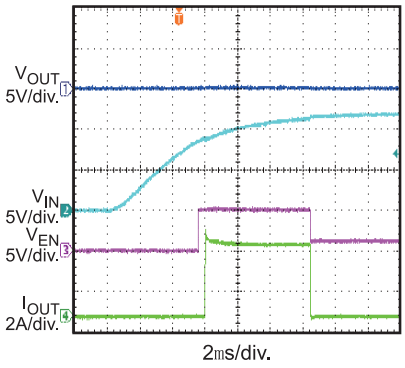
V_{IN} = 12 V, V_{EN} = 5 V, R_{LIMIT} = 22 Ω, C_{OUT} = 10 µF, $C_{DV/DT}$ = Float, T_A = 25°C, unless otherwise noted.

Shutdown through Enable

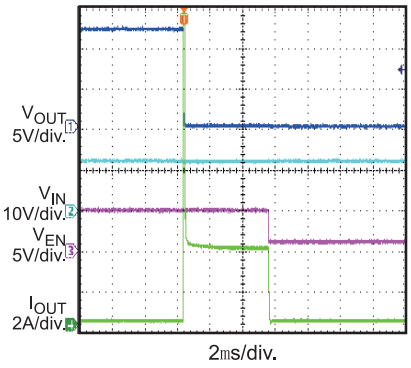
R_{LOAD} = 5Ω



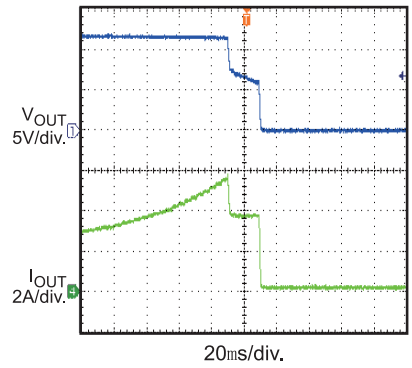
Short Circuit before Input Voltage Start-Up and Thermal Shutdown



Short Circuit during Normal Operation and Thermal Shutdown

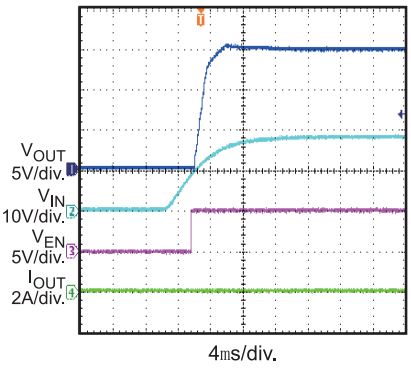


Current Limit



Start-Up into OVP

V_{IN} = 18V



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	I-LIMIT	**Current limit set.** A resistor between I-LIMIT and SOURCE sets the overload and short-circuit current limit levels.
2	ENABLE/FAULT	**Tri-state, bi-directional interface**. ENABLE/FAULT is floated to enable the output of the device. ENABLE/FAULT disables the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on ENABLE/FAULT enters an intermediate state, which signals a monitoring circuit that the device is in thermal shutdown.
3	DV/DT	**Slew rate of the output voltage at turn on control**. DV/DT has an internal capacitor that allows it to ramp up over 1 ms. An external capacitor can be added to DV/DT to increase the ramp time. If an additional time delay is not required, DV/DT should be left open.
4	GND	**Negative input voltage to the device.** This is used as the internal reference for the IC.
5,6	SOURCE	**Source of the internal power FET and the output terminal of the IC**.
7,8	VCC	**Input.** Positive input voltage.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

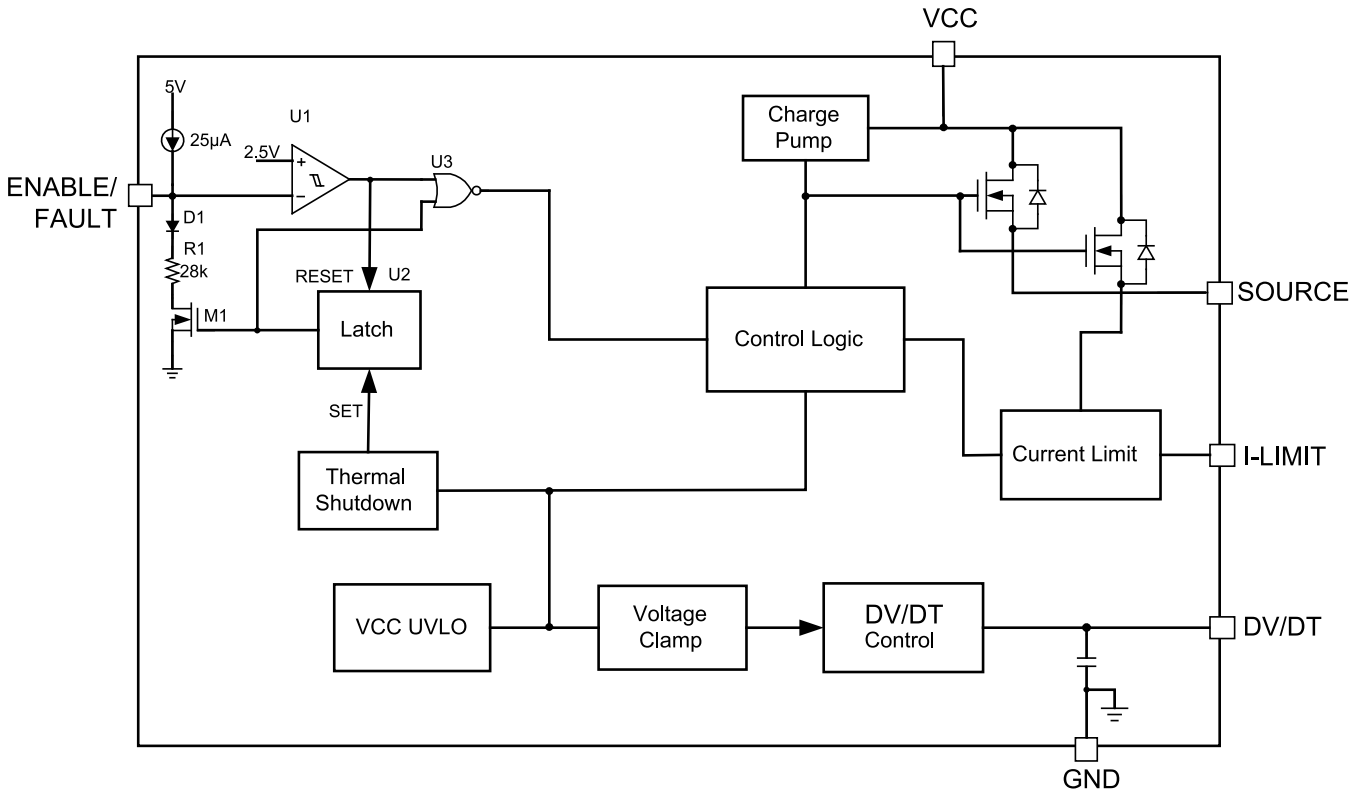


Figure 1—Functional block diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

OPERATION

The MP5014A limits the inrush current to the load when a circuit card connects to a live backplane power source, thereby limiting the backplane's voltage drop and the dv/dt of the voltage to the load. It offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature, eliminating the external current-sense power resistor, power MOSFET, and thermal sensor.

Under-Voltage Lockout Operation (UVLO)

If the supply (input) is below the UVLO threshold, the output is disabled, and the ENABLE/FAULT line is driven low.

When the supply rises above the UVLO threshold, the output is enabled and the fault line is released. When the fault line is released, the supply is pulled high by a 25 µA current source. No external pull-up resistor is required. In addition, the pull-up voltage is limited to 5 V.

Output Over-Voltage Protection (OVP)

If the input voltage is higher than the OVP threshold, the output is clamped at 15 V, typically.

Current Limit

When the part is active, if the load reaches the trip current (the minimum threshold current triggers over-current protection) or a short is present, the part switches into constant-current (hold current) mode. The part is shutdown only if the over-current condition remains long enough to trigger thermal protection.

However, when the part is powered up by VCC or EN, the load current should be less than the hold current. Otherwise, the part cannot be turned on fully.

In a typical application using a current limit resistor of 22 Ω, the trip current is 5.6 A, and the hold current is 3.8 A. If the device is in its normal operating state and passing 2 A, it will need to dissipate only 144 mW with the very low on resistance of 36 mΩ. For the package dissipation of 100°C/W, the temperature rise is only +14°C. Combined with a 25°C ambient temperature, this is only a 39°C total package temperature.

During a short-circuit condition, the device has 12 V across it. The hold current clamps at 3.8 A and therefore must dissipate 45.6 W. At 100°C/W (if uncontrolled), the temperature will rise above the MP5014A thermal protection (+175°C) and shut down the device to cause the temperature to drop. Proper heat sink must be used if the device is intended to supply the hold current and not shut down. Without a heat sink, the hold current should be maintained below 125 mA at +25°C and below 75 mA at +85°C to prevent the device from activating a thermal shutdown.

Thermal protection

When thermal protection is triggered, the output is disabled, and the ENABLE/FAULT line is driven to the middle level. The thermal fault condition is latched, and the part will remain in a latched off state until the power is re-started, or ENABLE/FAULT is re-set.

ENABLE/FAULT

ENABLE/FAULT is a bi-directional, three level I/O with a weak pull-up current (25 µA typically). The three levels are low, mid, and high. ENABLE/FAULT functions to enable/disable the part and to relay fault information.

ENABLE/FAULT as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

ENABLE/FAULT as an output:

1. The pull-up current may (if not over ridden) allow a "wired nor" pull up to enable the part.
2. An under voltage causes a low on ENABLE/FAULT and clears the fault flag.
3. A thermal fault causes a mid level on ENABLE/FAULT and sets the fault flag.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

The ENABLE/FAULT line must be high level for the output to turn on.

The fault flag is an internal flip-flop that can be set or re-set under the conditions below:

1. Thermal Shutdown: sets fault flag.
2. Under Voltage: re-sets fault flag.
3. Low Voltage on ENABLE/FAULT: re-sets fault flag.
4. Mid Voltage on ENABLE/FAULT: no effect.

During a thermal shutdown, ENABLE/FAULT is driven to the mid level.

There are four types of faults, and each fault has a direct and indirect effect on ENABLE/FAULT and the internal fault flag (see Table 1).

In a typical application there are one or more of the MP5014A chips in a system. The ENABLE/FAULT lines will be connected to each other typically.

Table 1—Fault function influence in application

Fault Description	Internal Action	Effect on Fault Pin	Effect on Flag	Effect on Secondary Part
Short/over current	Limits current	None	None	None
Under voltage	Output is turned off	Internally drives ENABLE/FAULT to logic low	Flag is re-set	Secondary part output is disabled, and the fault flag is re-set
Over voltage	Limits output voltage	None	None	None
Thermal shutdown	Shuts down the part. The part is latched off until UVLO or driven to ground externally	Internally drives ENABLE/FAULT to mid level	Flag is set	Secondary part output is disabled

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

APPLICATION INFORMATION

Current Limit

The desired current limit is a function of the external current limit resistor (see Table 2).

Table 2—Current limit vs. current limit resistor (V_{CC} = 12 V)

R_{LIMIT} (Ω)	15.4	22	24.9	30	49.9	100
Trip current (A)	7.95	5.62	5.23	4.57	3.43	2.64
Hold current (A)	5.61	3.81	3.35	2.78	1.69	0.88

Rise Time

The rise time is a function of the capacitor ($C_{DV/DT}$) on DV/DT (see Table 3).

Table 3—Rise time vs. $C_{DV/DT}$

$C_{DV/DT}$	none	33 pF	470 pF	1 nF
Rise time (typically, ms)	1	1.45	9.6	20.3

* **NOTE:** Rise Time = K_{RT}*(50 Pf + $C_{dv/dt}$), K_{RT} = 18.1E6

The rise time is measured from 10 percent to 90 percent of the output voltage (see Figure 2).

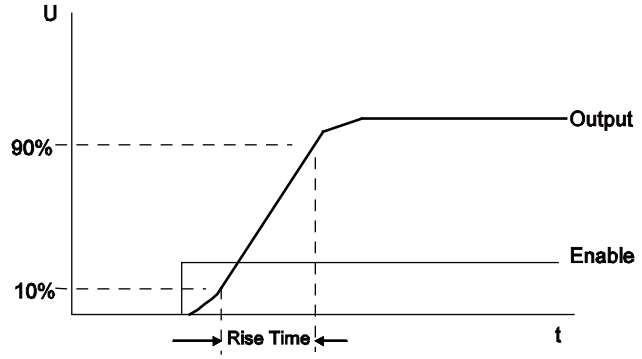
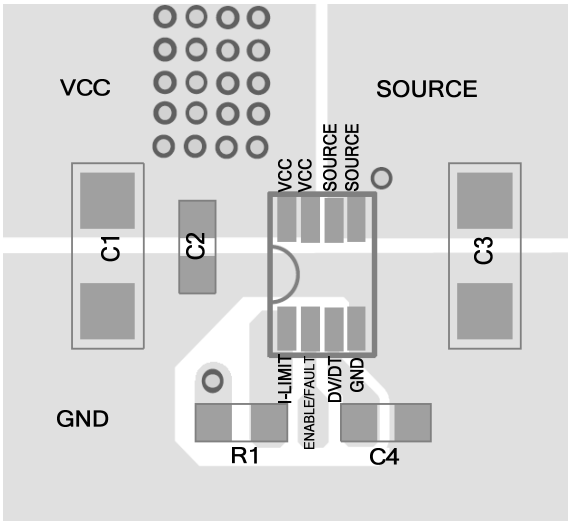


Figure 2—Rise time

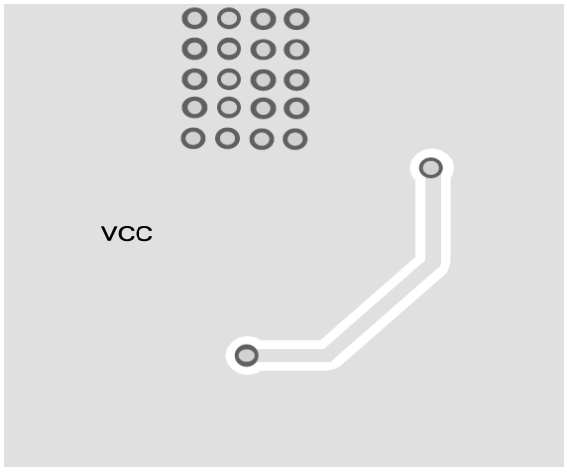
PCB LAYOUT GUIDELINES

Efficient PCB layout is critical to achieve stable operation. Please refer to Figure 3 and follow the guidelines below:

1. Place R_{LIMIT} close to I-LIMIT.
2. Place $C_{DV/DT}$ close to DV/DT and the input capacitor close to VCC.
3. Ensure there is a large enough copper area near VCC and source to achieve better thermal performance.



Top Layer



Bottom Layer

Figure 3—Recommended PCB layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

Design Example

Table 4 is a design example following the application guidelines for the given specifications:

Table 4—Design example

V_{IN}	12 V
Trip current	5.6 A
Hold current	3.8 A

Figure 4 shows the application schematic. The Typical Performance Characteristics section shows the circuit waveforms. For additional device applications, please refer to the related evaluation board datasheet.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

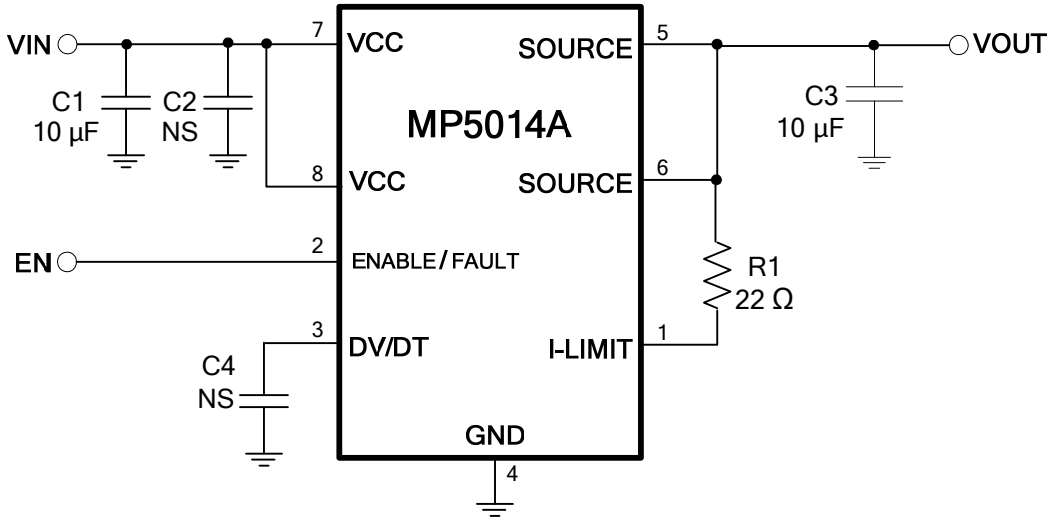
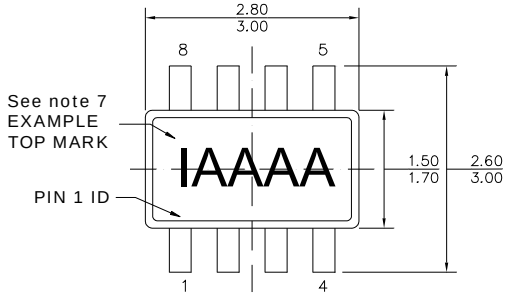


Figure 4—Typical application schematic

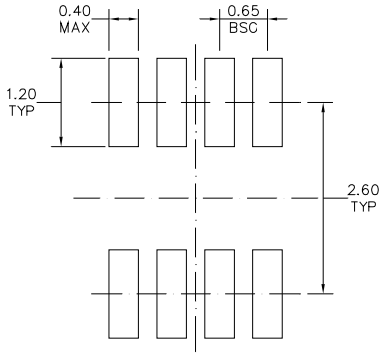
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE INFORMATION

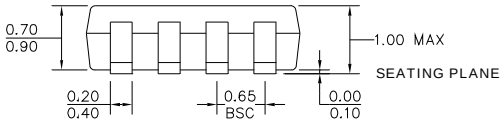
TSOT23-8



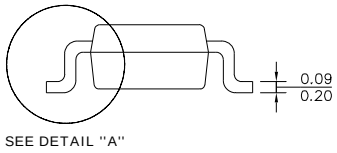
TOP VIEW



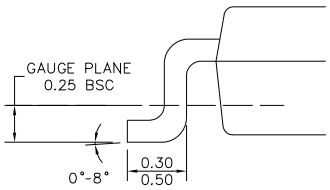
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.