MP4410

36V, 100mA Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP4410 is a high-frequency, step-down, switching regulator with integrated high-side/low-side, high-voltage power MOSFETs. It provides a highly efficient output of up to 100mA.

42V rated MOSFETs and 4.5V to 36V operation range accommodates a variety of step-down applications in automotive input environment. A 5μA shutdown mode quiescent current allows use in battery-powered applications.

It allows for high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load condition to reduce the switching and gate driver losses.

The switching frequency during start-up and short circuit also can be scaled down to helps prevent inductor current runaway. Thermal shutdown provides reliable, fault-tolerant operation.

The MP4410 is available in a 3mmx3mm QFN10 package.

FEATURES

- 20μA Quiescent Current
- Wide 4.5V to 36V Operating Range
- 42V Integrated MOSFETs with 0.7Ω and 2.25Ω Ron
- Programmable Switching Frequency
- Stable with Ceramic Output Capacitors
- Low Output Ripple
- Programmable Soft-Start
- Adjustable Input UVLO Hysteresis
- Precision Peak Current Limit without Current-Sensing Resistor
- Programmable Peak Current Limit
- >90% Efficiency at 10V VIN to 5V V_{OUT}/2mA
- 1.0V Feedback Reference Voltage
- Low Shutdown Mode Current: <5μA
- 3mmx3mm QFN10 Package

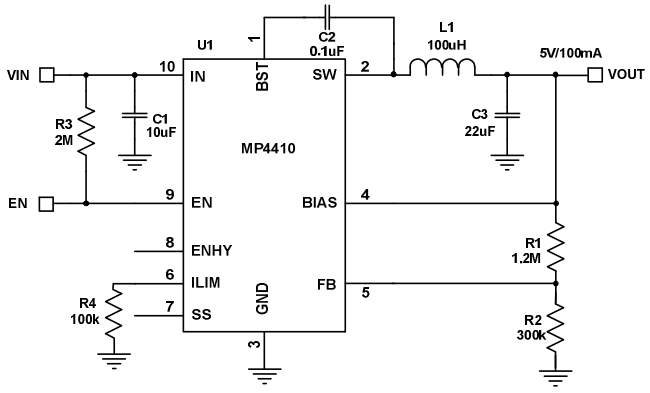
APPLICATIONS

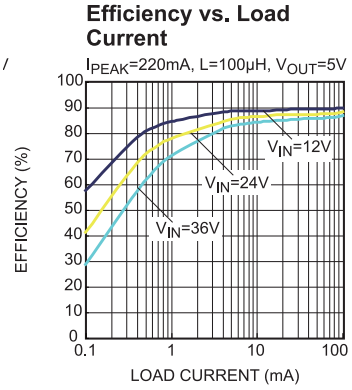
- 4mA to 20mA Current Loops
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4410GQ	QFN-10 (3mmx3mm)	*See Below*

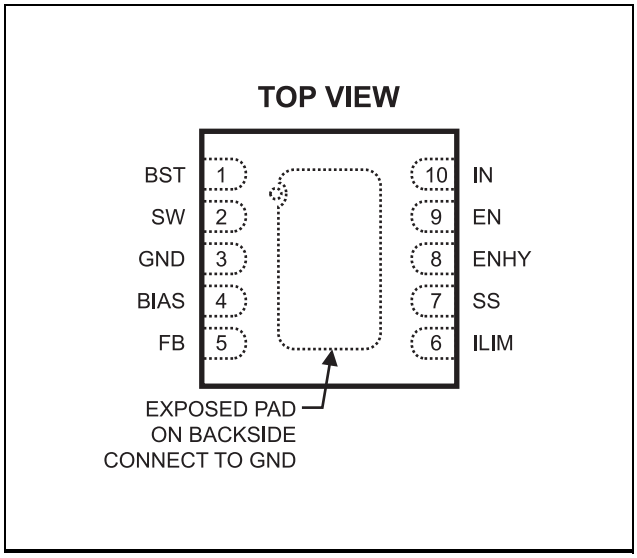
* For Tape & Reel, add suffix –Z (e.g. MP4410GQ–Z).

TOP MARKING

ANHY
LLL

ANH: product code of MP4410GQ;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN})..... -0.3V to +42V
Switch Voltage (V_{SW})…….-0.3V to (V_{IN} + 1V)
BST to SW.....-0.3 to +6.0V
All Other Pins..... -0.3V to +6.0V
Continuous Power Dissipation (T_A = +25°C) (2)
…….....2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 36V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (3mmx3mm).....	50	12 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J= 25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
Supply Quiescent Current	No load, V_{FB}=1.2V		20	25	μA
Shutdown Supply Current	V_{EN} < 0.3V		2	5	μA
VIN UVLO Rising Threshold			4.0	4.2	V
VIN UVLO Hysteresis			0.5		V
Feedback Voltage	V_{IN} = 4.5V to 36V	0.99	1	1.01	V
Feedback Current	V_{FB}=1V	-50	2	50	nA
FB OVP Hysteresis		35	60	85	mV
Upper Switch On Resistance	V_{BST}-V_{SW}=5V, Isw=50mA		2.25		Ω
Lower Switch On Resistance	V_{BIAS}=5V, Isw=50mA		0.7		Ω
Switch Leakage	V_{EN} = 0V, V_{SW} = 0V or 12V		0.01	1	μA
Peak Current Limit	I_{LIM} floating	30	55	80	mA
	I_{LIM}=200kΩ	75	110	135	mA
	I_{LIM}=0	200	260	320	mA
Minimum Switch On Time(5)			100		ns
Enable Rising Threshold	Low-to-High	1.45	1.6	1.75	V
Enable Falling Threshold	High-to-Low	1.1	1.2	1.3	V
Enable Current	V_{EN}=2.4V		1.2		μA
ENHY Sink Current Capability	Sink 4mA			0.4	V
Soft Start Current	Iss	2.5	3	4	μA
Built-in Soft Start time	SS pin floating		1		ms
Thermal Shutdown(5)			160		°C
Thermal Shutdown Hysteresis(5)			20		°C

Notes:

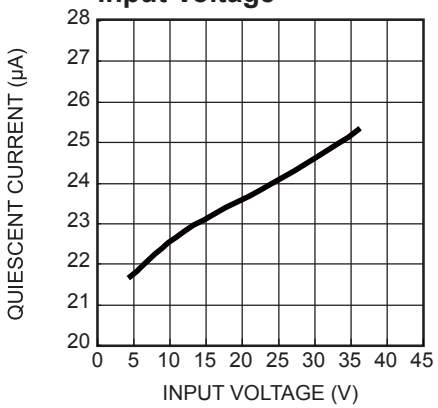
5) Derived from bench characterization. Not tested in production.

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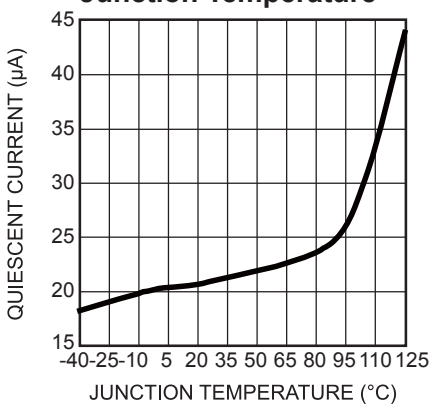
TYPICAL CHARACTERISTICS

V_{IN}=12V, T_J=25°C, unless otherwise noted.

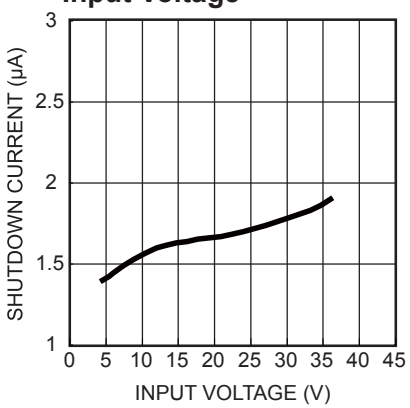
Quiescent Current vs. Input Voltage



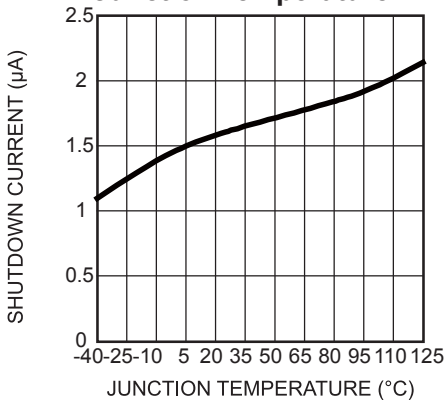
Quiescent Current vs. Junction Temperature



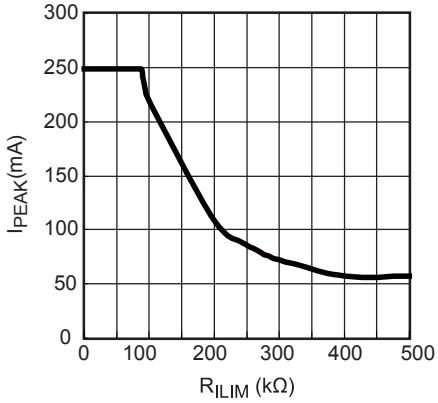
Shutdown Current vs. Input Voltage



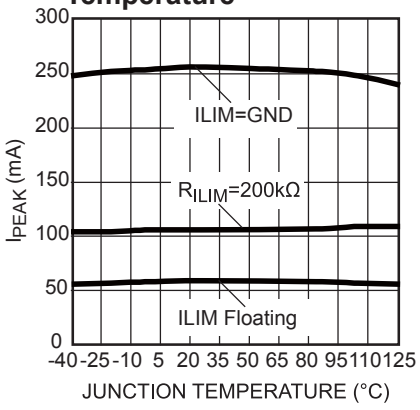
Shutdown Current vs. Junction Temperature



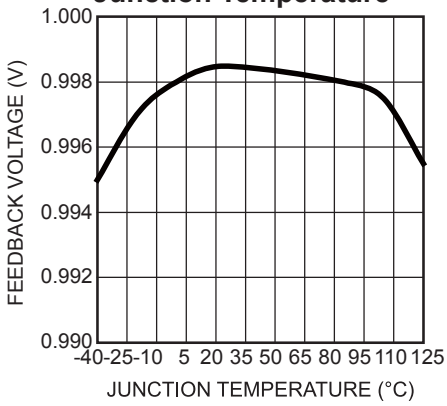
I_{PEAK} vs. R_{ILIM}



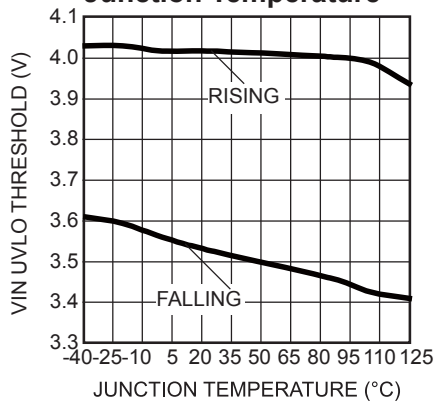
I_{PEAK} vs. Junction Temperature



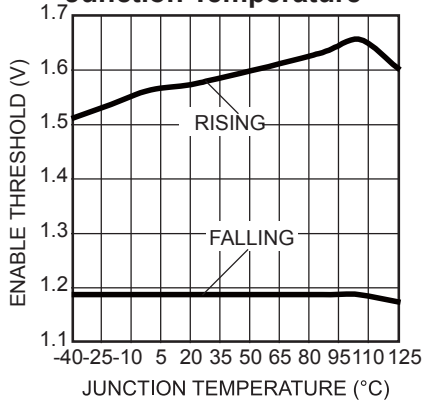
Feedback Voltage vs. Junction Temperature



VIN UVLO Threshold vs. Junction Temperature



Enable Threshold vs. Junction Temperature

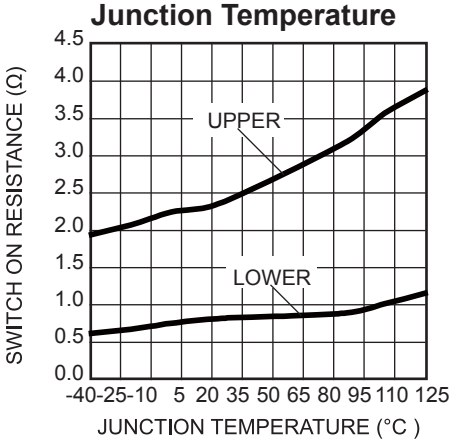


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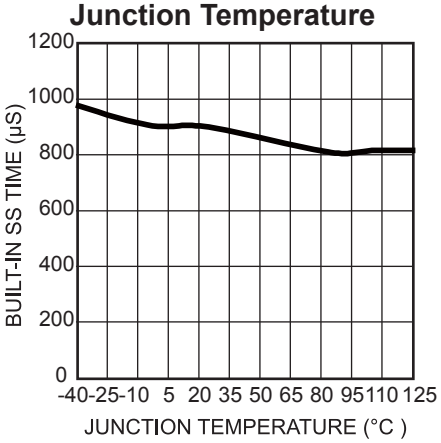
TYPICAL CHARACTERISTICS *(continued)*

V_{IN}=12V, T_J=25°C, unless otherwise noted.

Switch On Resistance vs. Junction Temperature



Built-in SS Time vs. Junction Temperature

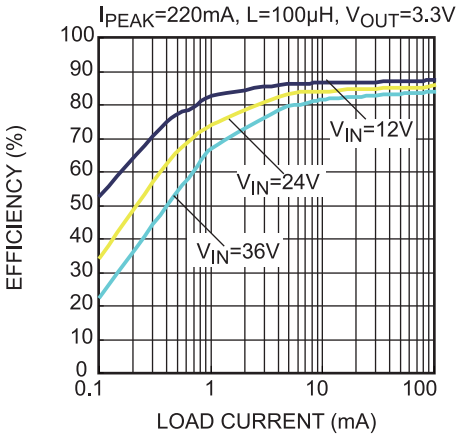


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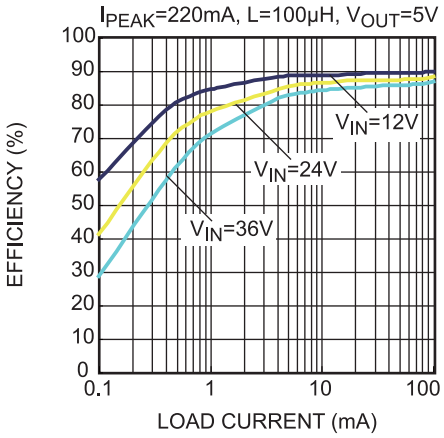
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=3.3V, C1 =10µF, C3 = 22µF, L1 = 100µH, and T_A = 25°C, unless otherwise noted.

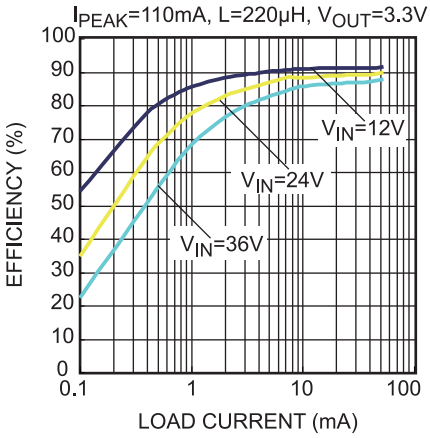
Efficiency vs. Load Current



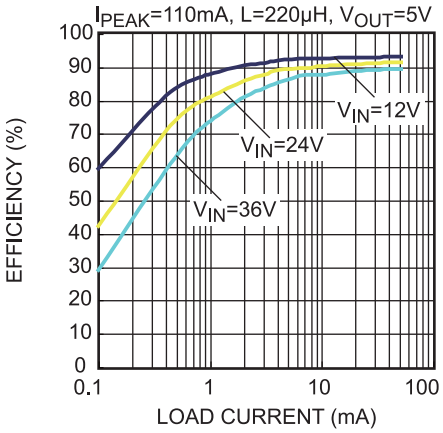
Efficiency vs. Load Current



Efficiency vs. Load Current



Efficiency vs. Load Current

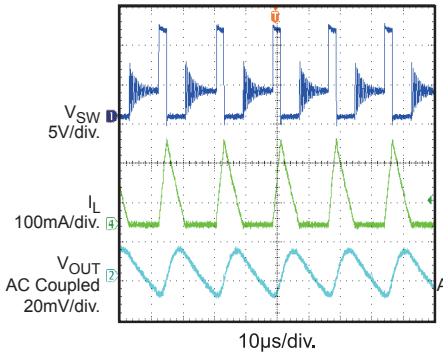


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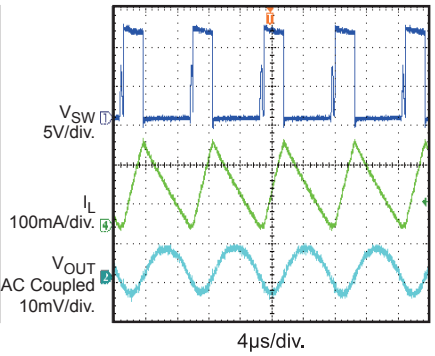
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=3.3V, C1 =10µF, C3 = 22µF, L1 = 100µH, and T_A = 25°C, unless otherwise noted.

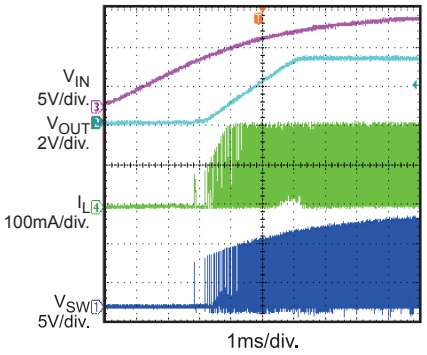
Output Ripple
I_{OUT}=50mA



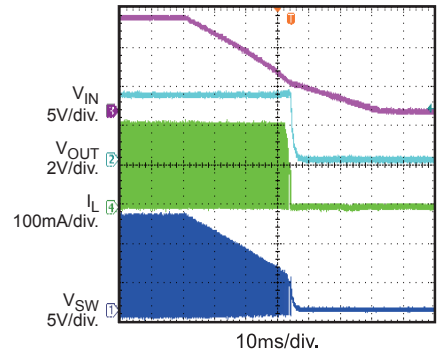
Output Ripple
I_{OUT}=100mA



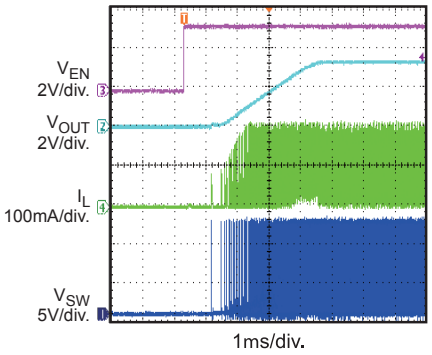
Startup Through Input Voltage
I_{OUT}=100mA



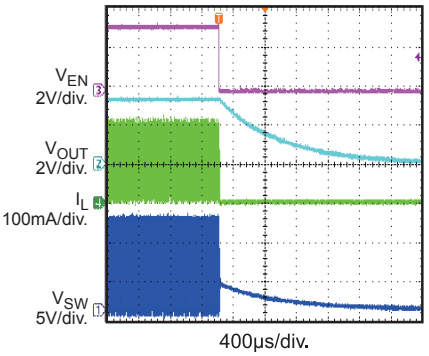
Shutdown Through Input Voltage
I_{OUT}=100mA



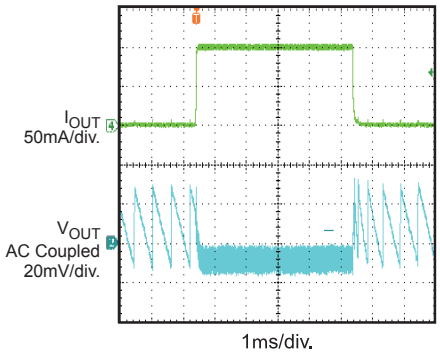
Startup Through EN
I_{OUT}=100mA



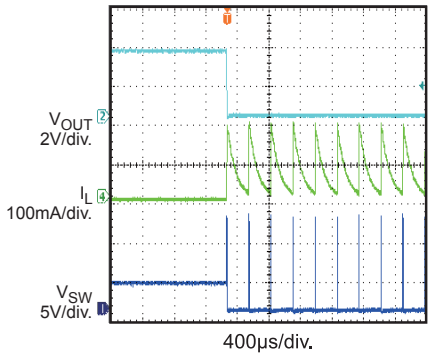
Shutdown Through EN
I_{OUT}=100mA



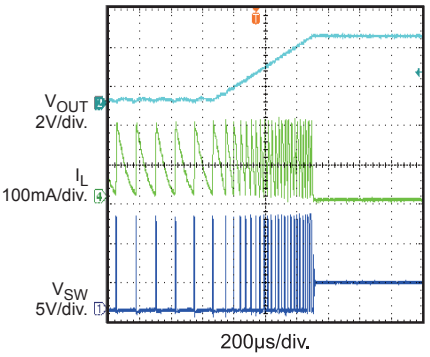
Load Transient
I_{OUT}=1mA to 100mA



Short Circuit Entry
I_{OUT}=0 to Short Circuit



Short Circuit Recovery
Short Circuit to I_{OUT}=0



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PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. Positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
2	SW	Switch Node. Output from the high-side switch and internal Schottky diode.
3	GND	Ground. Connected the output capacitor as close as possible to avoid high-current switch paths.
4	BIAS	Controller Bias Input. Supplies current to the internal circuit when V_{BIAS}>2.9V and power LS driver when VBIAS>4.5V.
5	FB	Feedback. Input to the error amplifier. Connected to the tap of an external resistive divider between the output and GND. Sets the regulation voltage when compared to the internal 1V reference.
6	ILIM	Peak Current Limit. A resistor from ILIM to GND sets the peak current limit.
7	SS	Soft-Start Control Input. Connect a capacitor from SS to GND to set the soft-start period.
8	ENHY	EN Indicator Open Drain Output. Goes low when EN falls below 1.2V.
9	EN	Enable Input. Pull this pin below the low threshold to shut the chip down. Pull it above the high threshold enables the chip. Float this pin to shut the chip down.
10	IN	Input Supply. Requires a decoupling capacitor to ground to reduce switching spikes.

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FUNCTIONAL BLOCK DIAGRAM

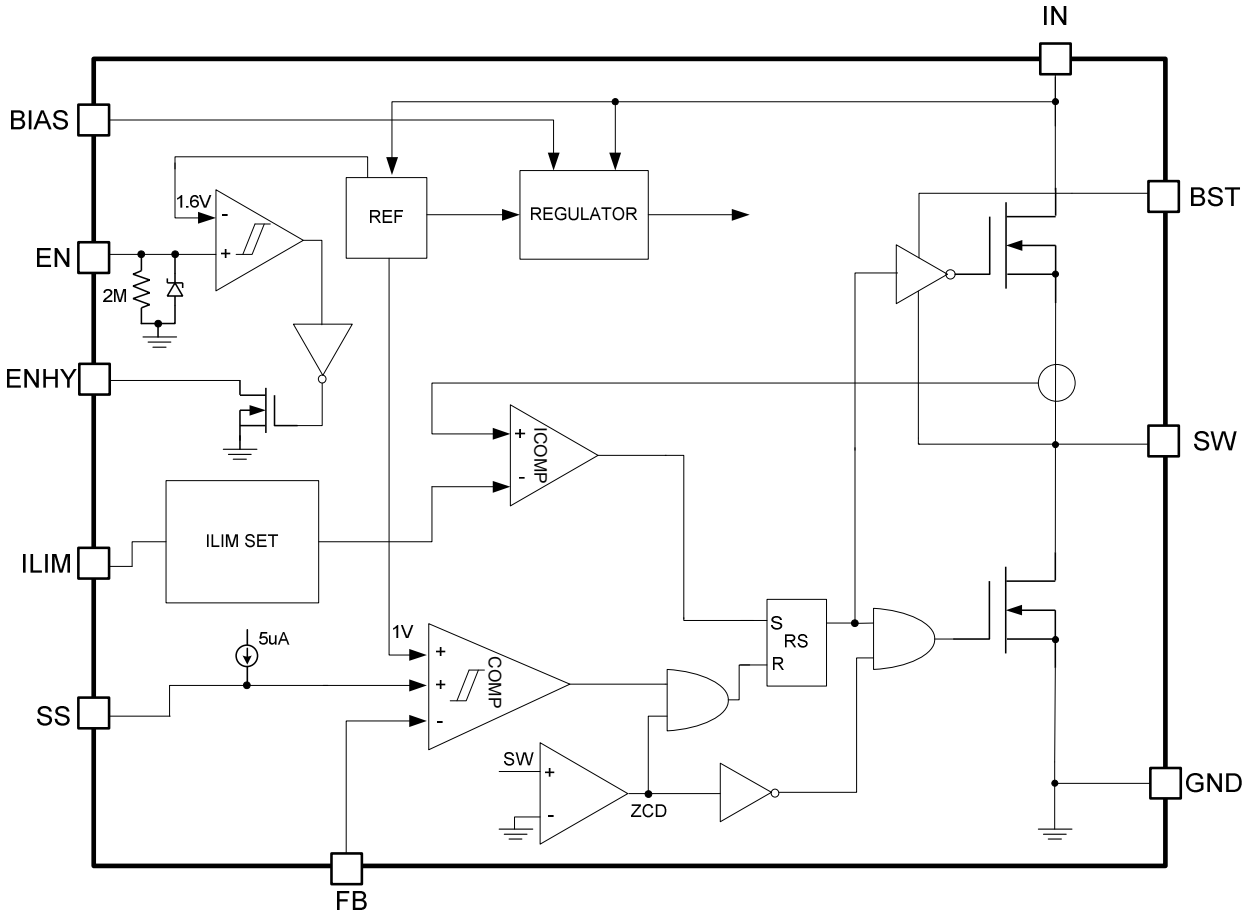


Figure 1—Functional Block Diagram

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OPERATION

The MP4410 is a 36V, 100mA, synchronous, step-down switching regulator with integrated high-side and low-side high-voltage power MOSFETs (HS_FET and LS_FET, respectively). It provides a highly-efficient, 100mA output. It features a wide input voltage range, internal/external soft-start control, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

PWM Control

The ILIM comparator, FB comparator and zero current detector (ZCD) block control the PWM. If V_{FB} is below the 1V reference and the inductor current drops to zero, HS-FET turns on and the ILIM comparator starts to sense the HS-FET current: When the HS-FET current reaches the limit set by the ILIM pin, or FB reaches the OVP threshold, the HS-FET turns off and LS-FET turns on together with the ZCD block. Meanwhile, the ILIM comparator is turned off to reduce the quiescent current. The LS-FET turns off together with ZCD block after the inductor current drops to zero. If V_{FB} is less than the 1V reference at this time, the HS-FET turns on at once and commences another cycle. If V_{FB} is still higher than 1V reference, HS-FET would not turn on till V_{FB} drops below 1V.

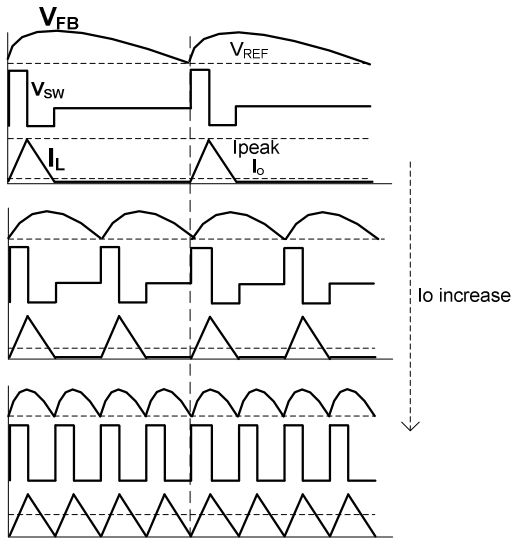


Figure 2 – PWM Control

Internal Regulator and BIAS

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} is greater than 3.0V, the output of the regulator is in full regulation. Lower values of V_{IN} result in lower output voltages.

When V_{BIAS}>2.9V, the BIAS supply overrides the input voltage and supplies power to the 2.6V internal regulator. When V_{BIAS}>4.5V, it can power LS driver furthermore. Using BIAS to power internal regulator can improve the efficiency. It is recommended to connect BIAS to the regulated output voltage when it is in the range of 2.9V to 5.5V. When output voltage is out of above range, an external supply that is >2.9V or even better >4.5V is needed to power BIAS.

Enable Control

The MP4410 has a dedicated enable-control pin, EN: when V_{IN} goes high, the EN pin enables and disables the chip. This is HIGH effective logic. Its trailing threshold is 1.2V typically and its rising threshold is about 400mV higher. When floating, EN pin is internally pulled down to GND through a 2M resistor to disable the chip.

When EN = 0V, the chip goes into the lowest shutdown-current mode. When EN is higher than zero but lower than its rising threshold, the chip remains in a shutdown mode but with a slightly larger shutdown current.

Internally a zener diode is connected from EN pin to GND pin. The typical clamping voltage of the zener diode is 7.5V. So VIN can be connected to EN through a high ohm resistor if the system doesn't have another logic input acting as enable signal. The resistor needs to be designed to limit the EN pin sink current less than 100μA. Just note that there is an internal 2M resistor from EN to GND, so the external pull up resistor should be smaller than $\frac{[V_{IN(MIN)} - 1.6V] \times 2M}{1.6V}$ to make sure the part can EN on at the lowest operation VIN.

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Under-Voltage Lockout

V_{IN} under voltage lockout (UVLO) protects the chip from operating below the operational supply voltage range. The UVLO-rising threshold is about 4V while its trailing threshold is about 3.5V.

Soft-Start

Reference-type soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a constant current to charge external SS capacitor. The soft-start (SS) voltage slowly ramps up from 0V at a slow pace set by the soft-start time. When V_{SS} is less than the V_{REF}, V_{SS} overrides V_{REF} so the error amplifier uses V_{SS} instead of V_{REF} as the reference. When V_{SS} is higher than V_{REF}, V_{REF} resumes control.

V_{SS} is also associated with V_{FB}. Though V_{SS} can be much smaller than V_{FB}, it can only barely exceed V_{FB}. If somehow V_{FB} drops, V_{SS} tracks V_{FB}. This function aides in short-circuit recovery: when a short-circuit is removed, the SS ramps up as if it is a fresh soft-start process. This prevents output voltage overshoot.

Thermal Shutdown

Thermal shutdown prevents the chip from thermally running away. When the silicon die temperature exceeds its upper threshold, the thermal shutdown feature shuts down the whole chip. When the temperature falls below its lower threshold, the chip resumes function.

Floating Driver and Bootstrap Charging

The external bootstrap capacitor powers the floating MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of about 2.4V with a hysteresis of about 300mV. During this UVLO, the SS voltage of the controller resets to zero. When the UVLO is disabled, the controller follows the soft-start process.

The dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage difference between

BST and SW falls below its working parameters, a PMOS pass transistor connected from V_{IN} to BST turns on to charge the bootstrap capacitor. The current path is from V_{IN} to BST and then to SW. The external circuit must have enough voltage headroom to accommodate charging.

As long as V_{IN} is sufficiently higher than SW, the bootstrap capacitor can charge. When the power MOSFET is ON, V_{IN} is about equal to SW so the bootstrap capacitor cannot charge. The best charging period occurs when the external free-wheeling diode is on so that V_{IN} - V_{SW} is at its largest. When there is no current in the inductor, V_{SW} equals V_{OUT} so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

Under higher duty cycle operating conditions, the time period may not fully-charge the capacitor.

If the external circuit does not have sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage in normal operation region.

Startup and Shutdown

If both V_{IN} and V_{EN} are higher than their appropriate thresholds, the chip starts operating. The reference block starts first, generating stable reference voltage and currents, and then enables the internal regulator. The regulator provides stable supply for the rest device.

While the internal supply rail is high, an internal timer holds the power MOSFET off for about 50μsec to blank startup glitches. When the internal soft-start block is enabled, it first holds its SS output low and then slowly ramps up.

Three events shut down the chip: V_{EN} low, V_{IN} low, and junction temperature triggers the thermal shutdown threshold. For shutdown, the signaling path is blocked first to avoid any fault triggering. Internal supply rail are pulled down then. The floating driver is not subject to this shutdown command, but its charging path is disabled.

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APPLICATION INFORMATION

Setting Peak Current

The peak current can be programmed from 55mA to 260mA by changing the resistor between ILIM pin and ground. The peak current setting resistor R_{ILIM} can be calculated by the formula:

$$R_{ILIM} = \frac{22}{I_{peak}} (k\Omega)$$

Where 55mA≤Ipeak≤260mA.

When R_{ILIM}≤84kΩ, Ipeak is clamped at its maximum value 260mA; when R_{ILIM}≥400kΩ, Ipeak is clamped to its minimum value 55mA. To be convenient, ILIM pin can be just shorted to GND when Ipeak is set at 260mA and floating when Ipeak is set at 55mA.

When setting Ipeak, be noticed that the maximum output current is equal to half of the Ipeak. Make sure the Ipeak is high enough for the output current requirement. Also be noticed that higher Ipeak would result in higher inductor current ripple, larger input and output voltage ripple, which means bigger components (inductor, input and output capacitors).

Selecting the Inductor

As the Ipeak is determined, for given input voltage and output voltage, the inductor value can be determined by the following formula:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{peak} \times f_s}$$

Where fs is the switching frequency at the maximal output current.

Larger inductor value results in lower switching frequency, as well as higher efficiency. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current as well as the slow load transient dynamic performance. There is also a lower limit of the inductor value, which is determined by the minimum on time. In order to keep the inductor working under control, the inductor value should be chosen higher than Lmin that is derived from below formula:

$$L_{MIN} = \frac{V_{IN(MAX)} \times T_{ON(MIN)}}{I_{peak}}$$

Where $V_{IN(MAX)}$ is the max value of input voltage. $T_{ON(MIN)}$ is the designed 100ns minimum switch on time.

Switching Frquency

Switching frequency can be estimated by below equation.

$$f_s = \frac{2 \times Io \times V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak}^2 \times V_{IN} \times L}$$

Higher Ipeak and inductor can get lower fs. And fs inceases as Io increasing. When Io increases to its maximal value Ipeak/2, fs also reaches its highest value and can be derived by:

$$f_{s(max)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak} \times V_{IN} \times L}$$

Below figures show the calculated fs(max) at different VIN and inductor with typical Vo (3.3V and 5V) and Ipeak (220mA).

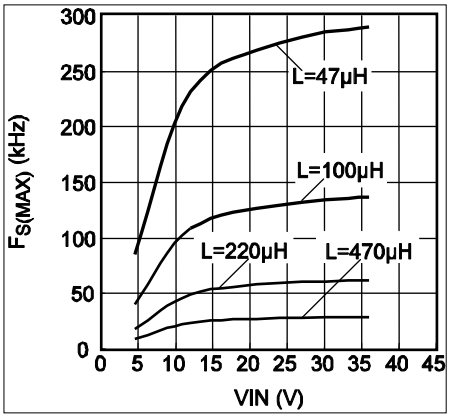


Figure 3 – $f_{s(max)}$ at V_{OUT}=3.3V

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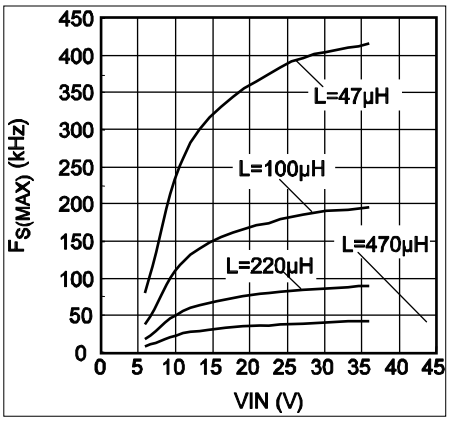


Figure 4 – $f_{s(max)}$ at V_{OUT}=5V

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. To get the desired output voltage, divider resistor can be chosen through below formula:

$$\frac{R1}{R2} = \frac{V_{OUT}}{V_{REF}} - 1$$

Where V_{REF} is the FB reference voltage 1V.

The current flows into divider resistor would increase the supply current, especially at no load and light load condition. The Vin supply current caused by the feedback resistors can be calculated from:

$$I_{IN_FB} = \frac{V_{OUT}}{R1+R2} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta}$$

To reduce this current, resistors in the megohm range are recommended. The recommended value of the feedback resistors are shown in Table 1.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	1200	523
5	1200	300

Under Voltage Lock Out Point Setting

MP4410 has internal fix under voltage lock out (UVLO) threshold: rising threshold is about 4V while trailing threshold is about 3.5V. For the application needs higher UVLO point, can use external resistor divider between EN and VIN as shown in Figure 5 to get higher equivalent UVLO threshold.

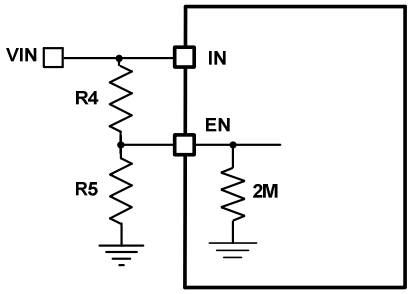


Figure 5 – Adjustable UVLO using EN pin

The UVLO threshold can be computed from below two equations.

$$UVLO_{TH_Rising} = (1+\frac{R4}{2M//R5}) \times EN_{TH_Rising}$$

$$UVLO_{TH_Falling} = (1+\frac{R4}{2M//R5}) \times EN_{TH_Falling}$$

Furthermore, ENHY pin can be used to get additional UVLO hysteresis as shown in Figure 6.

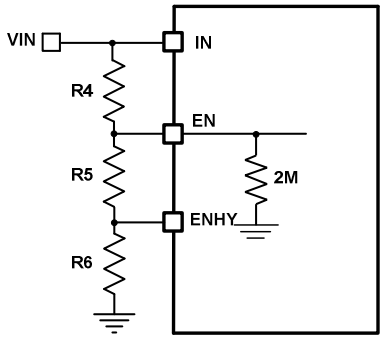


Figure 6 – Adjustable UVLO using EN & ENHY pin

The ENHY pin is an open drain output that goes low when EN falls below its falling threshold 1.2V. The UVLO rising threshold in Figure 6 is same to the one in Figure 5. But the falling threshold is lowered by adding R6 and the detailed value can be calculated by below formula.

$$UVLO_{TH_Falling} = [1+\frac{R4}{2M//(R5+R6)}] \times EN_{TH_Rising}$$

Inversely, when the special UVLO threshold is determined, resistor divider also can be calculated by above equations. Just note again the current flows through this divider. To reduce the current, resistors in the megohm range are recommended.

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Soft Start Capacitor

There is an internal 1ms soft start when float SS pin and this is the shortest soft start time. To get longer soft start, it needs to add capacitor between SS pin and GND. The soft start time is the duration when SS is charged from 0 to FB reference voltage 1V by an internal 3μA current source. So the capacitor at SS pin can be chosen according to below formula:

$$C_{SS} = 3 \times T_{SS}\ (\mu F)$$

To get the soft start time longer than 1ms, a capacitor bigger than 3nF is needed. When using a capacitor smaller than 3nF, the soft start time is the internal 1ms soft start.

Feedforward Capacitor

As described above that the PWM control scheme of MP4410 is very special and the HS turn on when FB drops lower than reference voltage. This brings good load transient performance. However, this also makes the HS turn on moment is very sensitive to the FB voltage. Once there is noise on FB, the moment HS turns on is easy to be affected, and then Fsw jitter would occur. The Fsw jitter is easy to happen especially when Vo ripple is very small. To improve the jitter performance, a small feedforward capacitor between Vo and FB can be used and typical 39pF is recommended.

PCB Layout

1) Keep the path of switching current short and minimize the loop area formed by input capacitor, high-side, low-side MOSFET and output capacitor.
2) Bypass ceramic capacitors should be as close as possible to the VIN pin.
3) Make sure that all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.
4) Keep SW away from sensitive analog areas such as FB.
5) For better thermal performance and long-term reliability consideration, VIN, SW and GND should be connected to a large copper area respectively to cool the chip.

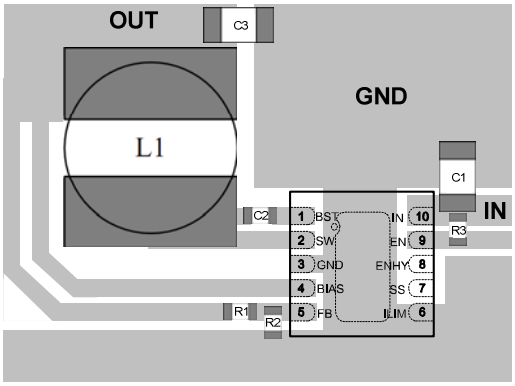


Figure 7 – PCB Layout Example

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2— Design Example

V_{IN}	4.5V – 36V
V_{OUT}	3.3V
Io	100mA

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

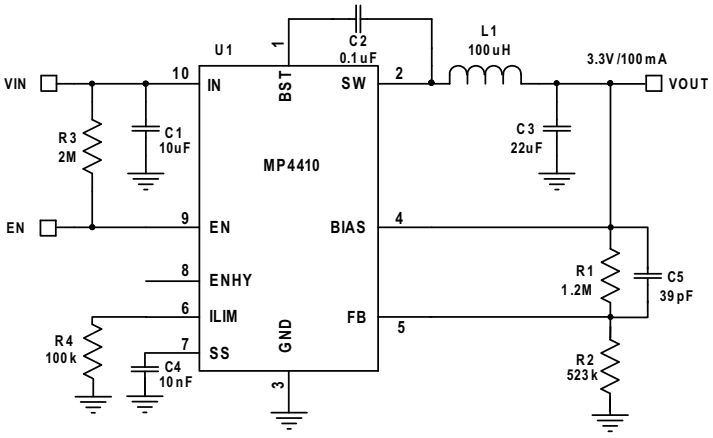


Figure 8 — Detailed Application Schematic

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TYPICAL APPLICATION CIRCUITS

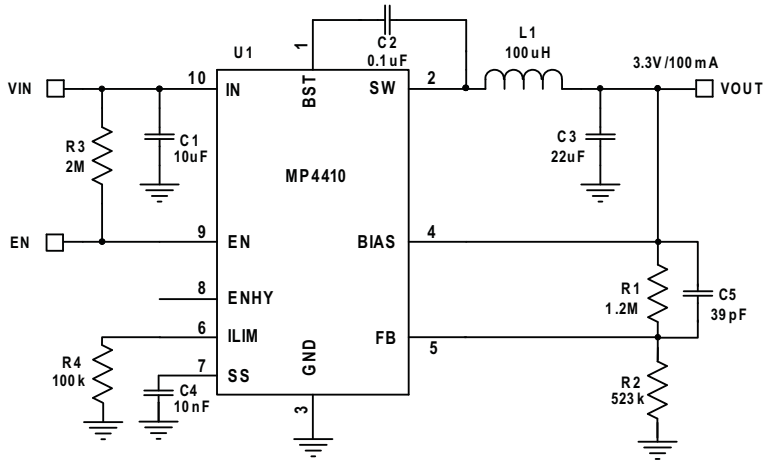


Figure 9 – 3.3V/100mA Output Typical Application Circuit

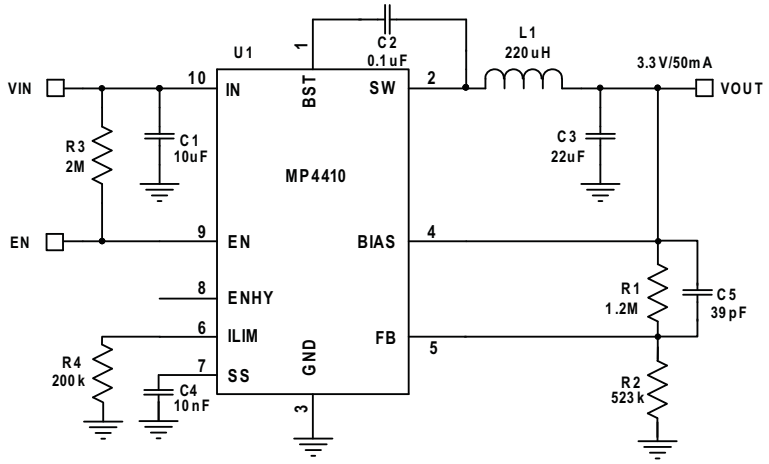


Figure 10 – 3.3V/50mA Output Typical Application Circuit

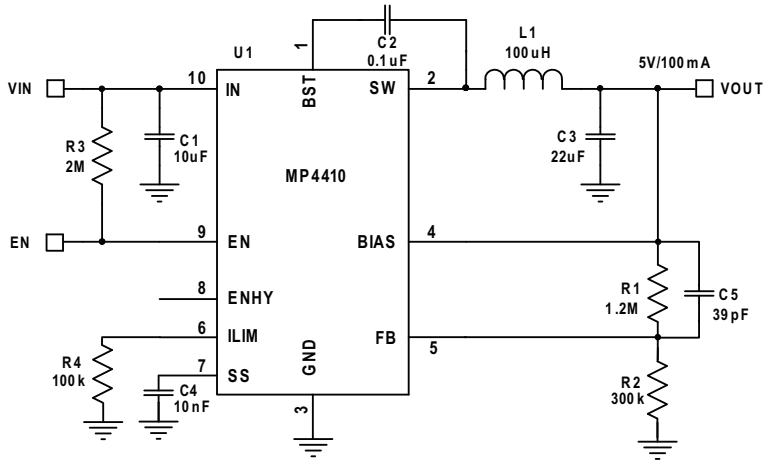
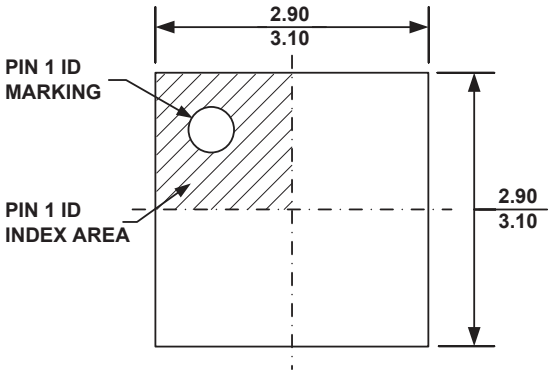


Figure 11 – 5V/100mA Output Typical Application Circuit

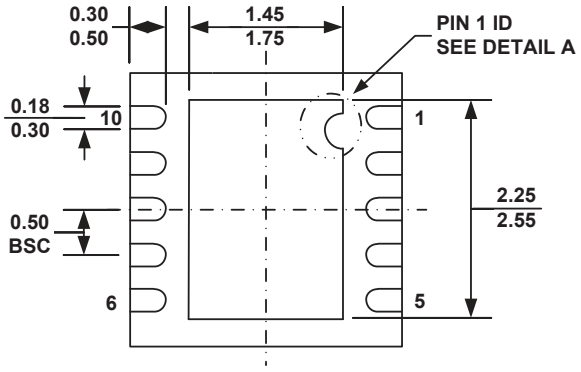
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PACKAGE INFORMATION

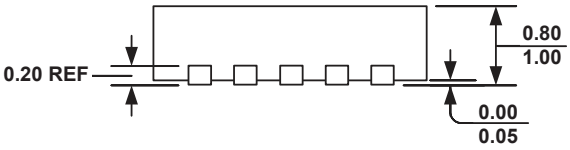
QFN-10 (3mmx3mm)



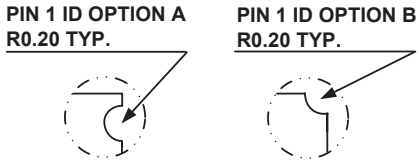
TOP VIEW



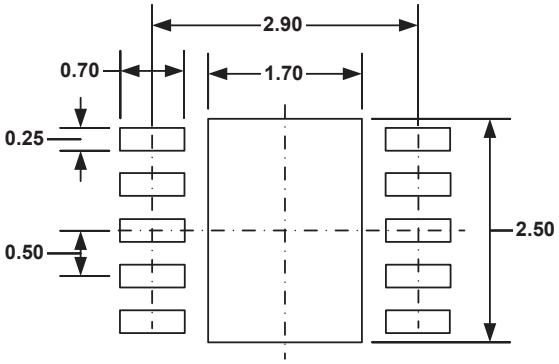
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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