DESCRIPTION

The MP3388S is a step-up converter with 8 current-source channels designed to drive arrays of white LED for LCD-panel backlighting applications.

The MP3388S uses current-mode, fixed-frequency architecture, and users can select a switching frequency of either 625kHz or 1.25MHz. It generates an output voltage up to 50V from a 4.3V-to-25V input supply. The MP3388S independently regulates the current in each LED string set by an external current setting resistor to a user-programmed value.

The MP3388S applies an internal current source to each LED string terminal, and can achieve a current balance of 2.5% regulation accuracy between strings. Its low 600mV regulation voltage on LED current sources reduces power loss and improves efficiency.

The MP3388S features external PWM dimming or DC-input PWM dimming, which allows for flexible backlight luminance control. The dimming PWM signal can be generated internally, and the dimming frequency is programmed by an external setting capacitor.

FEATURES

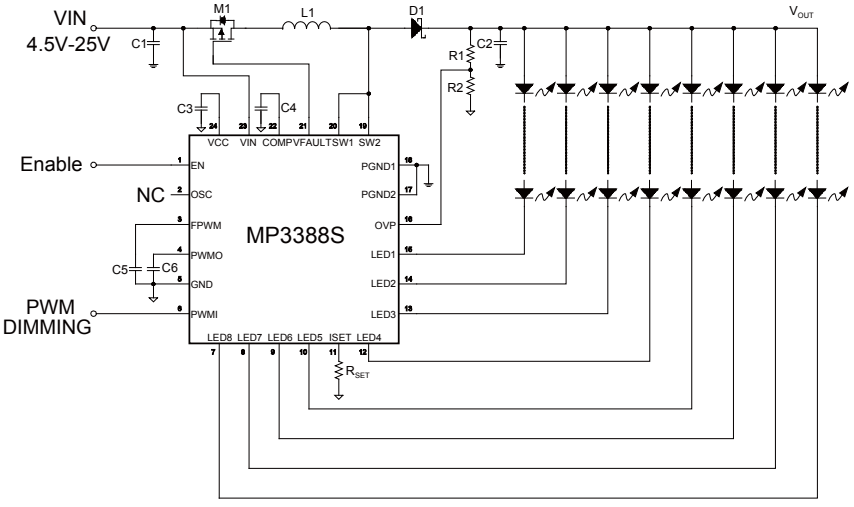
- High Efficiency
- Compact Size
- 4.3V-to-25V Input Voltage Range
- 50V Maximum Step-Up Voltage
- Balanced Driver for 8 WLED Strings
- 2.5% Current-Matching Accuracy between Strings
- Selectable Switching Frequency of 625kHz or 1.25MHz
- PWM or DC Input-Burst PWM Dimming
- Programmable Over-Voltage Protection
- Under-Voltage Lockout
- Open- and Short-LED Protection
- Thermal Shutdown
- Small QFN24 (4mm × 4mm) Package

APPLICATIONS

- Notebook PCs
- Tablet Computers
- Small LCD TV
- Handheld Terminal Displays
- Automotive Electronics Equipments

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TYPICAL APPLICATION



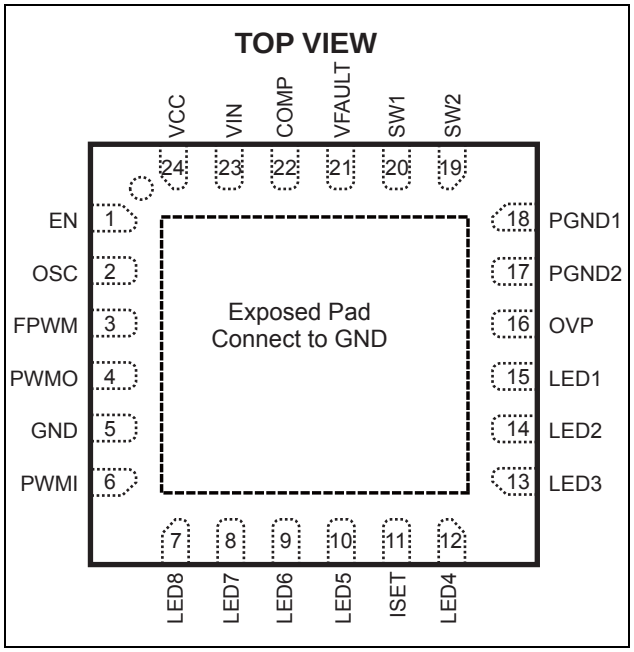
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP3388SGR*	QFN24 (4x4mm)	M3388S

* For Tape & Reel, add suffix –Z (e.g. MP3388SGR–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +30V
V_{VFAULT}..... V_{IN} –6V to V_{IN}
V_{SW}, V_{LED1} to V_{LED8}.....-1V to +50V
All Other Pins.....-0.3V to +6V
Continuous Power Dissipation... (T_A = +25°C) (2)
QFN24(4mm×4mm)..... 2.9W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.3V to 25V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN24 (4 x 4mm)	42	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ(MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD(MAX)=(TJ(MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} =12V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		4.3		25	V
Supply Current (Quiescent)	I_Q	V_{IN}=12V, V_{EN}=5V, no load.		1.8		mA
Supply Current (Shutdown)	I_{ST}	V_{EN}=0V, V_{IN}=12V			2	μA
LDO Output Voltage	V_{CC}	V_{EN}=5V, 6V<V_{IN}<25V, 0<I_{VCC}<10mA	4.5	5	5.5	V
Input UVLO Threshold	V_{IN_UVLO}	Rising Edge	3.4	3.9	4.3	V
Input UVLO Hysteresis				200		mV
EN ON Threshold	V_{EN_ON}	V_{EN} Rising	1.5			V
EN OFF Threshold	V_{EN_OFF}	V_{EN} Falling			0.8	V
EN Pull-Down Resistor	$R_{EN\ PD}$			500		kΩ
EN Source Current	$I_{EN\ SOURCE}$	V_{EN}=5V		10	15	μA
EN Sink Current	$I_{EN\ SINK}$	V_{EN}=0V			1	μA
STEP-UP CONVERTER						
SW ON-Resistance	R_{DS_ON}	I_{DS}=20mA		0.18	0.3	Ω
SW Leakage Current	I_{SW_LK}	V_{SW}=45V			1	μA
Switching Frequency	f_{SW}	V_{OSC}=V_{CC} or Floating	1.0	1.25	1.5	MHz
		V_{OSC}=0V	500	625	750	kHz
OSC High-Level Threshold	V_{OSC_H}	f_{SW}=1.25MHz	2.1			V
OSC Low-Level Threshold	V_{OSC_L}	f_{SW}=625kHz			0.8	V
Minimum ON Time	T_{ON_MIN}	PWM Mode, when no pulse skipping happens		100		ns
Maximum Duty Cycle	D_{MAX}		90	93	96	%
SW Current Limit	I_{SW_LIMIT}	Duty=90%	2.0			A
COMP Transconductance	G_{COMP}	ΔI_{COMP}=±10μA		100		μA/V
COMP Output Current	I_{COMP}			60		μA
PWM DIMMING						
PWMI HIGH Threshold	V_{PWMI_H}		1.5			V
PWMI LOW Threshold	V_{PWMI_L}				0.8	V
PWMO Output Impedance	R_{PWMO}		300	400	500	kΩ
PWMI Leakage Current	I_{PWMI_LK}		-1		+1	μA
PWMI Source Current	$I_{PWM\ SOURCE}$	V_{PWMI}=5V			1	μA
PWMI Sink Current	$I_{PWM\ SINK}$	V_{PWMI}=0V		3	6	μA
DPWM Frequency	f_{DPWM}	C_{FPWM}=2.2nF	1.2	1.6	2	kHz

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} =12V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LED CURRENT REGULATION						
LEDx Average Current	I_{LED}	R_{ISET}=60.4kΩ	19.4	20	20.6	mA
Current Matching (5)		I_{LED}=20mA			2.5	%
Maximum LED Current per String	I_{LEDmax}				30	mA
ISET Regulation Voltage			1.18	1.22	1.26	V
LEDx Regulation Voltage	V_{LEDX}	I_{LED}=20mA	500	600	700	mV
PROTECTION						
OVP Over-Voltage Threshold	V_{OVP_OV}	Rising Edge	1.17	1.23	1.3	V
OVP UVLO threshold	V_{OVP_UV}	Step-up Converter Fails	48	70	102	mV
LEDx Over-Voltage Threshold	V_{LEDX_OV}	V_{IN}>5.5V	5.1	5.5	5.9	V
LEDx UVLO Threshold	V_{LEDX_UV}		150	200	250	mV
Thermal Shutdown Threshold(6)	T_{ST}		130	150		℃
LEDx Over-Voltage Fault Timer		Vosc=high	1.3	1.6	1.9	ms
VFAULT Pull-Down Current	I_{FAULT}		40	55	70	μA
VFAULT Blocking-Off Voltage (with Respect to V_{IN})	V_{FAULT}	V_{IN} =12V, V_{IN}–V_{FAULT}		6		V

Notes:

5) Matching is defined as the difference of the maximum to minimum current divided by 2 times average currents.

6) Guarantee by design.

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PIN FUNCTIONS

Pin #	Name	Description
1	EN	Enable Control Input. Do not let this pin floating.
2	OSC	Switching-Frequency Selection. When left floating or connected to VCC, the step-up converter switching frequency is 1.25MHz. When connected to GND, the step-up converter switching frequency is 625kHz.
3	FPWM	Dimming PWM Frequency Setting. Connect a capacitor, C_{FPWM}, between FPWM and GND to set the DPWM frequency using the equation: $f_{DPWM}=3.5\mu F/C_{FPWM}$.
4	PWMO	PWM Filter Output. For external PWM dimming, connect a capacitor between PWMO and GND. For DC-input PWM dimming, directly apply a DC voltage between 0.2V and 1.2V. The DC-input PWM dimming polarity is negative.
5	GND	Analog Ground.
6	PWMI	PWM Signal Input. For external PWM dimming mode, apply a PWM signal. For DC-input PWM dimming mode, leave floating.
7	LED8	LED String 8 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 8 cathode to this pin.
8	LED7	LED String 7 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 7 cathode to this pin.
9	LED6	LED String 6 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 6 cathode to this pin.
10	LED5	LED String 5 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 8 cathode to this pin.
11	ISET	LED Current Setting. Tie a current setting resistor from this pin to ground to program the current in each LED string. $I_{LED} = 1000 \times 1.21V / R_{SET}$
12	LED4	LED String 4 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 4 cathode to this pin.
13	LED3	LED String 3 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 3 cathode to this pin.
14	LED2	LED String 2 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 2 cathode to this pin.
15	LED1	LED String 1 Current Input. This pin is the open-drain output of an internal dimming-control switch. Connect the LED String 1 cathode to this pin.

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PIN FUNCTIONS *(continued)*

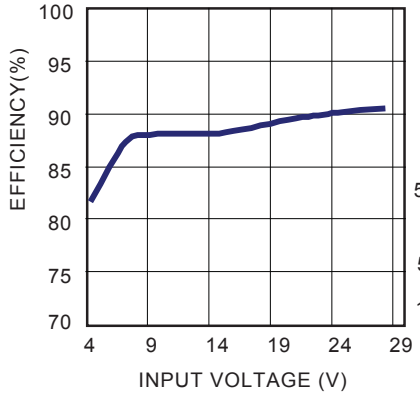
Pin #	Name	Description
16	OVP	Over-Voltage Protection Input. Connect to the tap of a resistor divider from the output to AGND to program the OVP threshold. When this pin voltage reaches 1.23V, the MP3388S triggers OVP mode.
17	PGND2	Step-Up Converter Power Ground. PGND1 and PGND2 should be shorted externally.
18	PGND1	Step-Up Converter Power Ground. PGND1 and PGND2 should be shorted externally.
19	SW2	Step-Up Converter Power Switch Output. SW2 is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW2. SW2 can swing between GND and 50V. SW1 and SW2 should be shorted externally.
20	SW1	Step-Up Converter Power Switch Output. SW1 is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW1. SW1 can swing between GND and 50V. SW1 and SW2 should be shorted externally.
21	VFAULT	Fault-Disconnection–Switch Driver Output. When the system starts up normally, this pin turns on the external PMOS. When the MP3388S is disabled, the external PMOS turns off to disconnect the input and output.
22	COMP	Step-Up Converter Compensation. This pin compensates the regulation control loop. Connect a capacitor or a series RC network from COMP to GND.
23	VIN	Supply Input. VIN supplies the power to the MP3388S chip. Drive VIN with a 4.3V-to-25V power source. Must be locally bypassed.
24	VCC	The Internal 5V Linear Regulator Output. VCC provides power for the internal MOSFET gate driver and the internal control circuitry. Bypass VCC to GND with a ceramic capacitor. If VIN is less than 5.5V, apply an external 5V supply directly on VCC.

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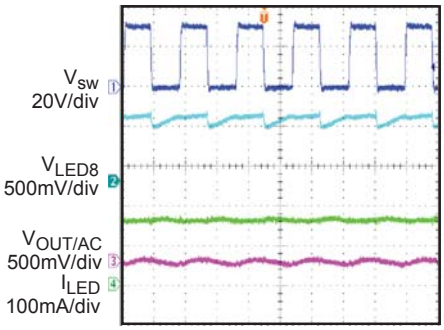
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =15V, 10 LEDs in series, 8 strings in parallel, 20mA/string, unless otherwise noted.

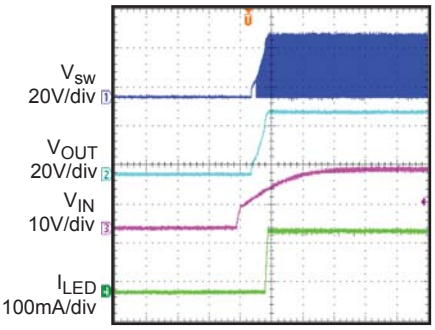
Efficiency vs. Input Voltage



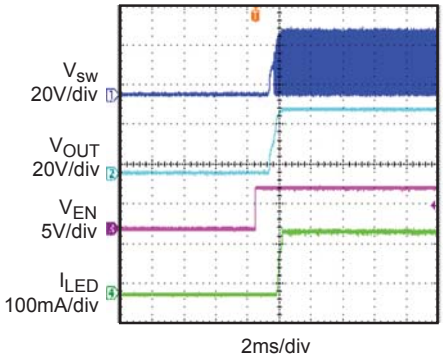
Steady State



Vin Startup

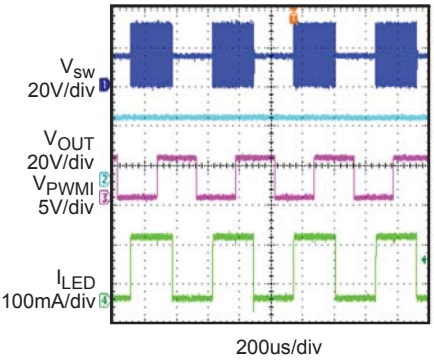


Ven Startup



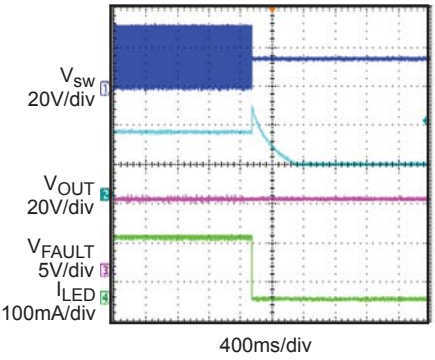
PWM Dimming

f_{PWM}=2kHz, D_{PWM}=50%



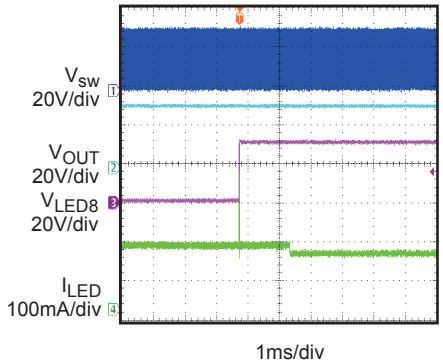
Open LED Protection

open all LED strings at working



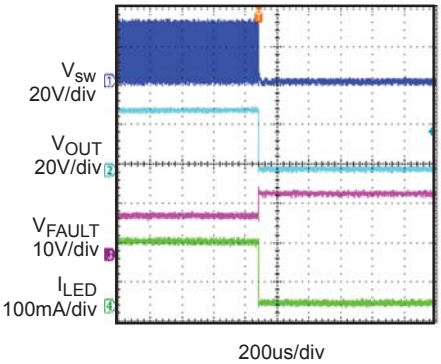
Short LED Protecton

short Vout to LEDx at working



Short LED Protection

short Vout to GND at working



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BLOCK DIAGRAM

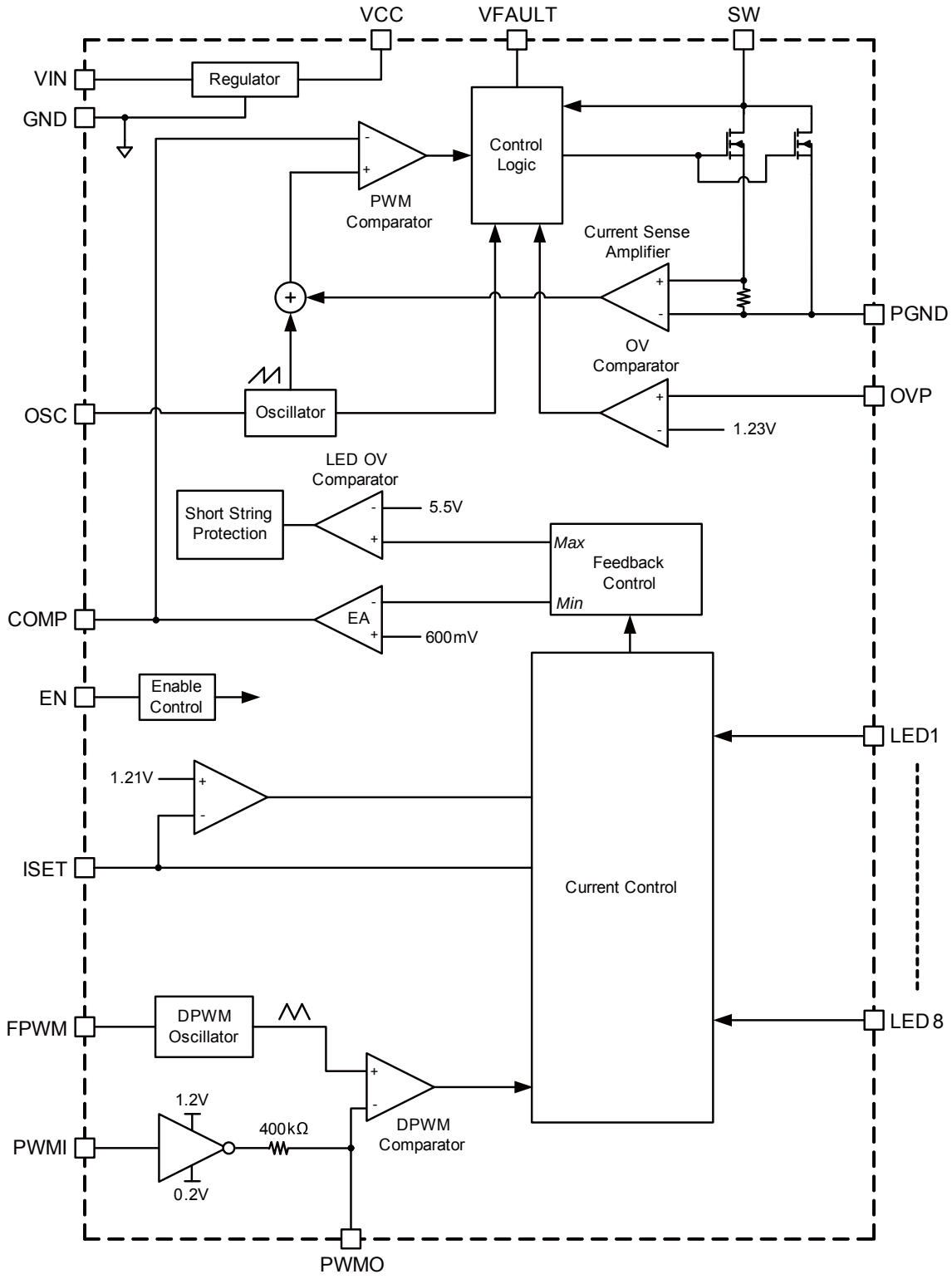


Figure 1: Functional Block Diagram

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OPERATION

The MP3388S employs a constant-frequency, peak-current–mode step-up converter and 8 channels of regulated current sources to regulate up to 8 strings of white LEDs.

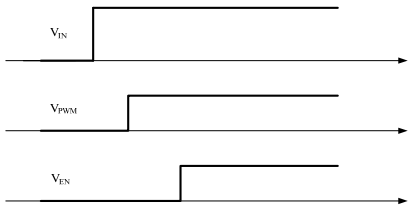
Internal 5V Regulator

The MP3388S includes an internal linear regulator (VCC). When VIN exceeds 5.5V, this regulator provides a 5V power supply for the internal MOSFET switch gate driver and the internal control circuitry. VCC drops to 0V when the chip shuts down. In applications where VIN is less than 5.5V, tie VCC and VIN together. The MP3388S features under-voltage lockout (UVLO). The chip is disabled until VCC exceeds the UVLO threshold. The UVLO hysteresis is approximately 200mV.

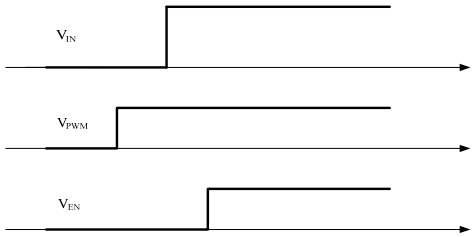
System Startup

When the MP3388S is enabled, the chip checks the topology connection first. The VFAULT pin slowly turns on the external fault disconnection PMOS. And after a 400μs delay, the chip monitors the OVP pin to check for the Schottky diode or if the boost output is shorted to GND. If the OVP voltage is below 70mV, the chip is disabled and the external PMOS is turned off together. The MP3388S also checks other safety limits, including UVLO and OTP if the OVP test passes. If the circuit passes all tests, then the MP3388S uses an internal soft-start to boosting the step-up converter.

For best results, use the following start-up sequence: either V_{IN} or the PWM dimming signal first, and then the enable signal (see Figure 2). The MP3388S does not require a power-off sequence (see Figure 4)



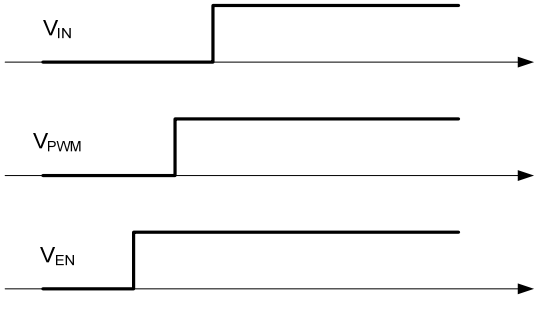
(a)



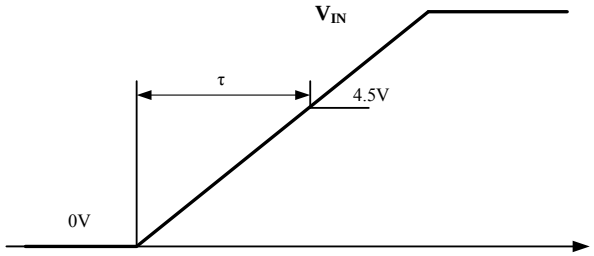
(b)

Figure 2: Recommended Start-Up Sequence

If using any other start-up sequence, as shown in Figure 3(a), and the unused LEDx pins are not connected to V_{OUT}, then decrease the input-voltage rise-time (τ). For a 6-string LED application, select τ less than 20ms as shown in Figure 3(b)



(a)



(b)

Figure 3: Input Voltage Rise-Time Indicator for a 6-String LED Application

Note: Use any power sequence if the V_{IN} rise-time from 0V to 4.5V is less than 20ms**.**

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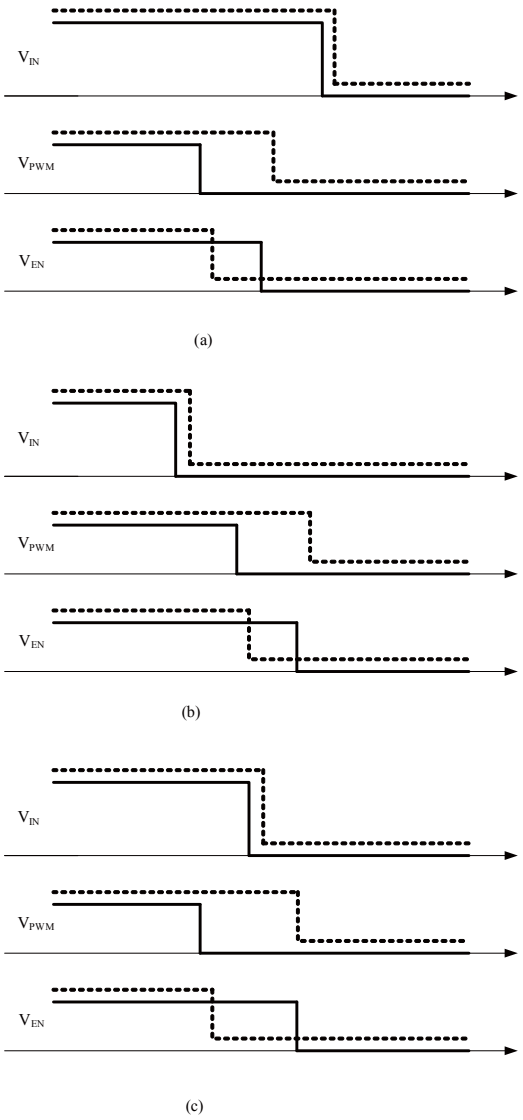


Figure 4: Recommended Power-Off Sequence

Step-Up Converter

The converter operation frequency is selectable (625kHz or 1.25MHz), which can optimize for external component sizes and improve efficiency.

At the beginning of each cycle, the internal clock turns on the power MOSFET. To prevent sub-harmonic oscillations at D>50%, add a stabilizing ramp to the output of the current-sense amplifier; the output goes to the positive input of the PWM comparator. When the PWM comparator's positive input voltage equals the output voltage of the error amplifier (V_{COMP}) the power MOSFET turns off.

The internal error amplifier amplifies the difference between the 600mV reference voltage and the feedback voltage. The converter automatically chooses the lowest active LEDx pin voltage to provide the bus voltage to power all the LED arrays.

If the feedback voltage drops below the 600mV reference, the output of the error amplifier increases to increase the current flowing through the power MOSFET, thus increasing the power delivered to the output. This forms a closed loop to regulate the output voltage.

At light-load operation—or V_{OUT}≈VIN—the converter enters pulse-skipping mode where the MOSFET turns on for a minimum ON-time of approximately 100ns before the converter discharges the power to the output. The MOSFET repeats this cycle until the output voltage requires a boost.

Dimming Control

The MP3388S provides two PWM dimming methods: external PWM signal from the PWMI pin or DC-input PWM dimming mode (see Figure 5).

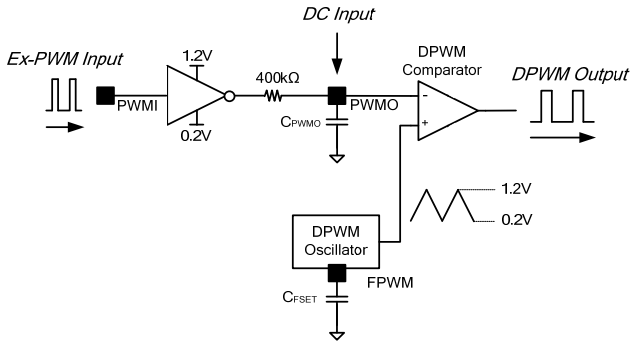


Figure 5: PWM Dimming

When applying a PWM signal to the PWMI pin, the MP3388S generates a DC voltage on the PWMO pin that is proportional to the duty cycle of the PWMI signal. By comparing the PWMO pin signal to the FPWM pin triangle waveform, the converter gets a choppy low-frequency signal with a duty cycle the same as the input's. This choppy low-frequency signal modulates the LED current.

Directly applying a DC analog signal to the PWMO pin also modulates the LED current: the DC signal is converted to a DPWM signal set at the oscillation frequency. The polarity is negative. The brightness of the LED array is proportional to the duty cycle of the DPWM signal. The capacitor at the FPWM pin sets the DPWM signal frequency.

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Open-String Protection

The open string protection is achieved through over-voltage protection (OVP). If one or more strings are open, the device pulls the respective LEDx pins to ground and the output voltage continues rising until it reaches the OVP threshold. Then the device records and disable the open LEDx strings with pin voltages less than 175mV. Once recording completes, the remaining LED strings force the output voltage back into tight regulation. The string with the highest voltage drop determines the output regulation level.

The MP3388S will always try to light at least one string. If all strings in use are open, the MP3388S shuts down the step-up converter. The part retains low-voltage LEDx string information until the part shuts down.

Short-String Protection

The MP3388S monitors each LEDx pin voltage to determine if there is a short string. If one or more strings are shorted, the respective LEDx pins will be pulled up to the boosted output and tolerate high voltage stress. If the LEDx pin voltage exceeds 5.5V, the device treats this condition as a short string fault (LEDx over-voltage fault). If the voltage remains above 5.5V more than than 1.6ms (V_{OSC}=HIGH), the device records the string and disables it. Once a string is recorded as a short, its current regulation is forced to disconnect from the output voltage loop regulation. The recorded LED strings remain OFF until the part restarts. If all strings in use are shorted, the MP3388S shuts down the step-up converter.

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APPLICATION INFORMATION

Selecting the Switching Frequency

The user can select either a 625kHz or a 1.25MHz step-up converter switching frequency. A bi-level switching frequency selection input (the OSC pin) sets the internal oscillator frequency. Tie the OSC pin to GND corresponds for 625kHz, and to VCC or float for 1.25MHz.

Setting the LED Current

The ISET pin sets the LED string currents to the same level as per the equation below:

$$I_{LED} = 1000 \times \frac{1.21V}{R_{SET}}$$

For R_{SET}=60.4kΩ, the LED current is 20mA. Do not leave the ISET pin open.

Setting the Over-Voltage Protection Threshold

The open string protection is achieved through OVP. In some cases, an LED string failure results in a 0V feedback voltage. The MP3388S then continues boosting the output voltage. OVP triggers if the output voltage reaches the programmed OVP threshold.

To ensure proper chip function, set the OVP setting resistor divider with appropriate values. Select an OVP threshold about 1.3x higher than the output voltage for normal operation.

$$V_{OVP} = 1.23 \times \frac{R_1 + R_2}{R_2}$$

Selecting the Dimming-Control Mode

The MP3388S provides four different dimming methods:

PWM Dimming Mode with Internal Triangle Waveform Generator

Apply a 100Hz-to-50kHz square waveform to the PWMI pin. The internal 400kΩ resistor and the external capacitor on the PWMO pin filters the dimming signal to a DC voltage (0.2V to 1.2V). Then an internal PWM dimming signal whose frequency is set by a capacitor on the FPWM pin modulates the DC voltage, where:

$$f_{DPWM} = \frac{3.5\mu F}{C_{FPWM}}$$

The minimum recommended PWM signal amplitude is 2.1V (See Figure 6).

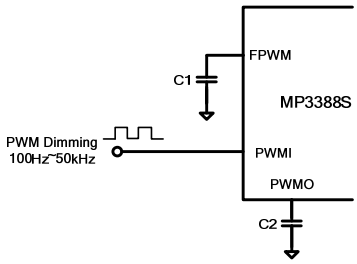


Figure 6: PWM Dimming with Internal Triangle Waveform Generator

Direct PWM Dimming with Positive Logic

To use a direct external PWM dimming signal, connect a 100kΩ resistor from the FPWM pin to GND and apply a 100Hz-to-30kHz (high SW frequency) PWM dimming signal to the PWMI pin. The minimum recommended amplitude of the PWM signal is 1.5V (See Figure 7).

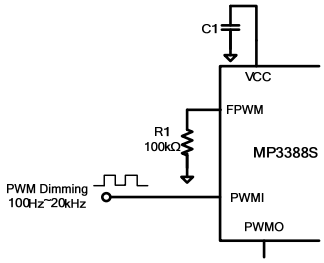


Figure 7: Direct PWM Dimming with Positive Logic

Table 1 shows the PWM dimming duty range with different PWM dimming frequencies.

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Table 1: PWM Frequency Range and Dimming Duty Cycle

f_{PWM}(Hz)	D_{MIN}	D_{MAX}
100<f≤200	0.16%	100%
200<f≤500	0.40%	100%
500<f≤1k	0.80%	100%
1k<f≤2k	1.60%	100%
2k<f≤5k	4.00%	100%
5k<f≤10k	8.00%	100%
10k<f≤20k	16.00%	100%
20k<f≤22k	18.00%	100%
22k<f≤25k	20.00%	100%
25k<f≤30k	24.00%	100%

Direct PWM Dimming with Negative Logic

Similar to direct PWM dimming with positive logic. Apply a 100Hz-to-30 kHz external square waveform to the PWMO pin for negative-logic PWM dimming. The minimum recommended amplitude of the PWM signal is 1.5V (see Figure 8).

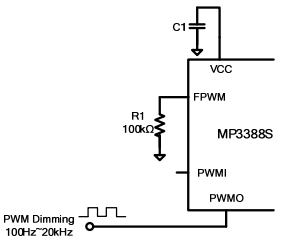


Figure 8: Direct PWM Dimming

DC-Input PWM Dimming with Negative Logic

For negative-logic DC-input PWM dimming, apply an analog signal (from 0.2V to 1.2V) to the PWMO pin. If applying a PWMO DC voltage <0.2V, the PWM duty cycle will be 100%. For PWMO DC voltages >1.2V, the output will be 0% (See Figure 9). The capacitor on the FPWM pin sets the internal triangle waveform frequency.

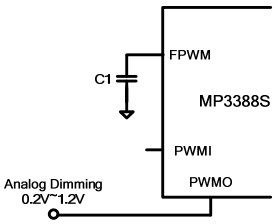


Figure 9: DC-Input PWM Dimming

Selecting the Inductor

A larger inductor results in less ripple current, lowering both the peak inductor current and stress on the internal N-channel MOSFET. However, a larger value inductor is larger physical size with a higher series resistance and a lower saturation current.

Choose an inductor that does not saturate under worst-case load conditions. Select the minimum inductance value to ensure that the boost converter works in continuous conduction mode, for high efficiency and good EMI performance.

Calculate the minimum inductance value with:

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times I_{LOAD} \times f_{SW}}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{LOAD} is the LED load current, and η is the efficiency.

Use either a 10μH (at a 1.25MHz switching frequency) or a 22μH (at a 625kHz switching frequency) inductor with a DC current rating of at least 40% higher than the maximum input current for most applications. Select an inductor with the smallest-possible DC resistance for greatest efficiency.

Selecting the Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency switching current from passing through the input. For best results, use ceramic capacitors with X5R or X7R dielectrics because of their low ESR and small temperature coefficients. For most applications, use a 4.7μF capacitor.

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Selecting the Output Capacitor

The output capacitor minimizes the output voltage ripple and ensures a stable feedback loop. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X7R dielectrics for their low ESR characteristics.

The output voltage ripple is estimated as:

$$V_{RIPPLE} \approx \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{LED}}{C2 \times f_{SW}}$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the input and output voltages respectively, I_{LED} is the LED current, f_{SW} is the switching frequency, and C2 is the output capacitor.

For most applications, use a 2.2μF ceramic capacitor.

LAYOUT CONSIDERATIONS

Layout and component placement on the PCB requires careful attention. Proper high-frequency switching-path layout can prevent noise and electromagnetic interference problems. The loop from SW (U1), to the output diode (D1), to the output capacitor (C3), to PGND (U1) carries a high-frequency pulse current: minimize the loop length and enclosed area (See Figure 10).

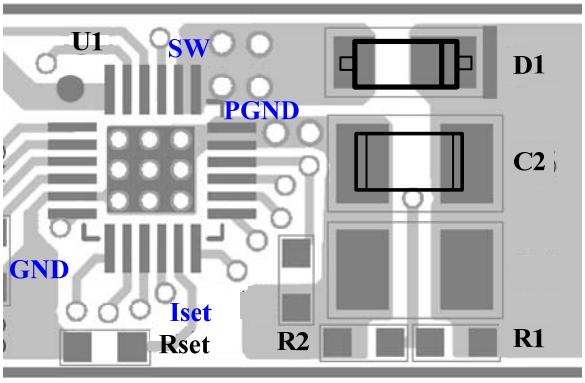


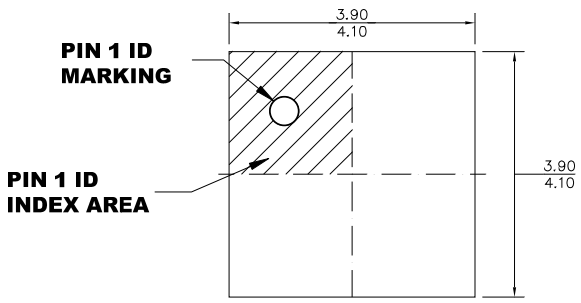
Figure 10: Sample Layout

The IC exposed pad is internally connected to GND pin, and all logic signals are refer to the GND. Externally connects PGND to GND, and avoid placing PGND near logic signals.

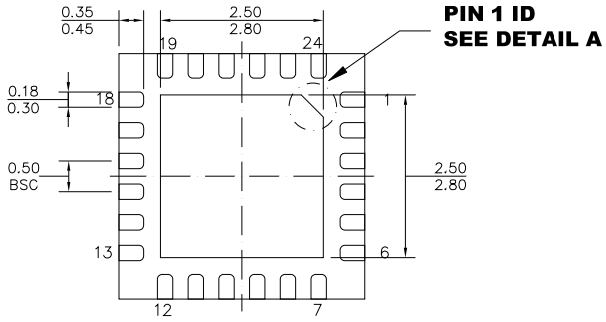
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PACKAGE INFORMATION

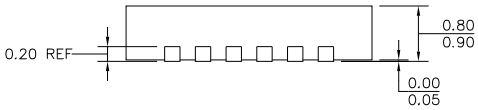
QFN24 (4mm × 4mm)



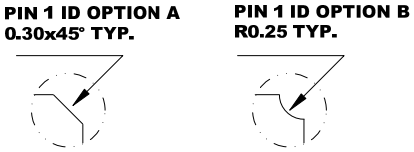
TOP VIEW



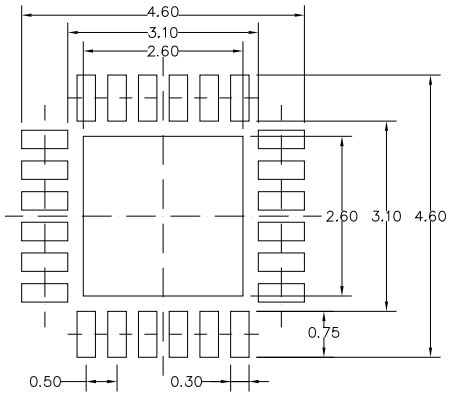
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VGGD.
5) DRAWING IS NOT TO SCALE.
6) ROUNDED FINGER PADS ARE RECOMMENDED TO PREVENT SOLDER BRIDGING.

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