MP2905

3V-28V Input, Hysteretic Synchronous Step-Down Controller

The Future of Analog IC Technology

DESCRIPTION

The MP2905 is a hysteretic voltage-mode control, synchronous PWM buck controller. The output voltage can be regulated from 0.6V to 0.9*VIN. It achieves high output current over a wide input supply range from 3V-28V.

MP2905 integrates an internal LDO regulator that makes the controller function at a wide input supply.

Hysteretic voltage-mode control provides fast transient response without additional loop compensation.

An adjustable soft-start prevents inrush current at turn-on. The device senses high-side switch voltage drop for hiccup current limit and short current protection. The frequency is adjustable from 200kHz to 500kHz.

The MP2905 is available in 10-pin MSOP package, provides a very compact system solution with minimal reliance on external components.

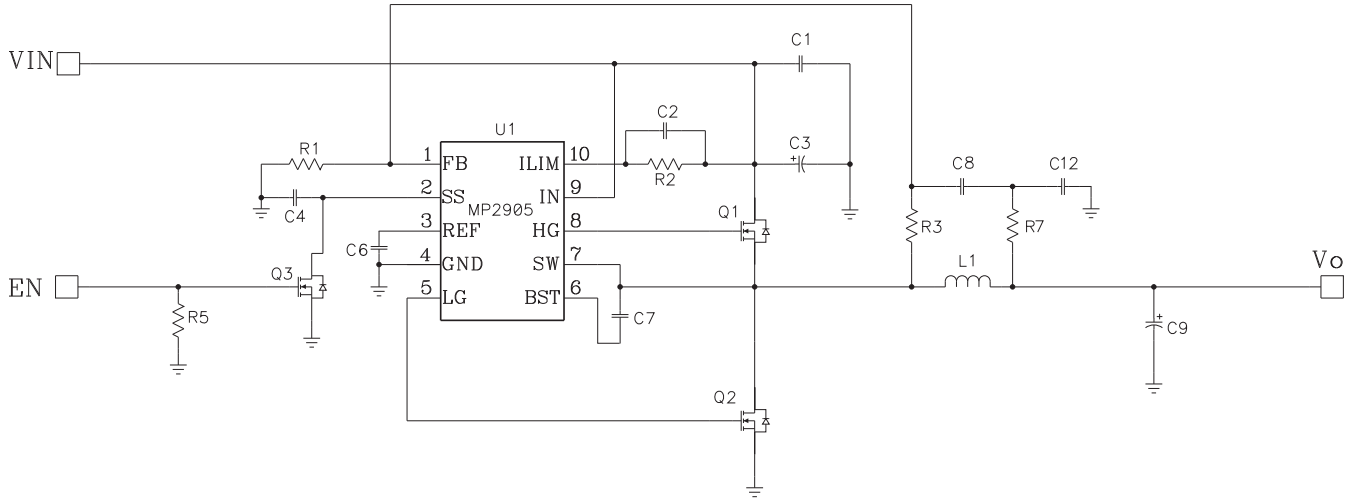
FEATURES

- Wide 3V to 28V Operating Input Range
- Output Adjustable from 0.6V to 0.9*Vin
- Switching frequency from 200kHz to 500kHz
- Programmable Soft-Start
- Hiccup current limit
- Lossless peak current sensing
- MSOP-10 package

APPLICATIONS

- Motherboard Power Supplies
- AGP and PCI-Express Power Supplies
- Graphic-Card Power Supplies
- Set-Top Boxes
- Point-of-Load Power Supplies

TYPICAL APPLICATION



MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

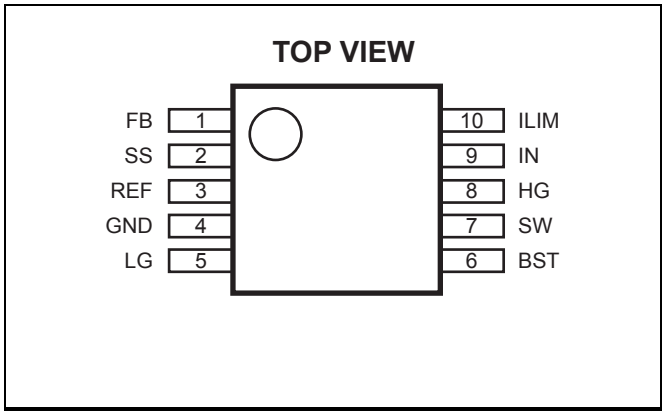
ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP2905EK	MSOP10	2905E	–40°C to +85°C

*For Tape & Reel, add suffix –Z (eg. MP2905EK–Z).

For RoHS compliant packaging, add suffix –LF (eg. MP2905EK–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN to GND ……... ….. ….....-0.3V to +30V
REF to GND …….....-0.3V to +6.5V
IN to REF ……..... ….....-0.3V to +25V
SS to GND ……..….. -0.3V to (REF + 0.3V)
LG to GND …….. -0.3V to (REF + 0.3V)
BST to GND…….. -0.3V to 36.5V
BST to SW……..……-0.3V to + 6.5V
SW to GND…….……-0.3V to +30V
HG to SW ……..….-0.3V to (BST + 0.3) V
FB to GND……..….-0.3V to +6.5V
ILIM to GND ..... ….....-0.3V to (IN + 0.3V)
ILIM to SW ……-0.6V to (IN + 0.3V)
HG and LG continuous current...±250mA RMS
Continuous Power Dissipation (TA = +25°C)(2)
…….0.77W
Junction Temperature.....+140°C
Storage Temperature Range
. …….....-65°C to +150°C
Lead Temperature (soldering, 10s)
…….....+300°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN}..... 3V to 28V
Operating Temperature .....–40°C to +85°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
MSOP10-EP	150	65	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature. T_J(MAX) the junction-to-ambient thermal resistance. θ_{JA} and the ambient temperature, T_A the maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=140°C(TYP) and disengages at T_J=120°C(TYP)
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, 4.7uF capacitor from REF, 0.01uf capacitor from SS to GND; V_{FB}=0.65V; V_{SW}=V_{GND}=0V; V_{ILIM}=11.5V; HG=unconnected; LG=unconnected; T_A=25°C, unless otherwise noted.

Parameter	Condition		Min	Typ	Max	Unit
IN Supply Voltage			3 (5)		28	V
REF output Voltage	I_{REF}=10mA		4.75	5.0	5.25	V
REF maximum output current			20			mA
BST output voltage	I_{BST}=10mA			5.0		V
BST maximum output current			20			mA
REF Undervoltage lockout (UVLO)	Rising		2.6	2.8	3	V
	Falling		2.25	2.45	2.65	V
	Hysteresis			350		mV
Supply Current	No switching, V_{FB}=0.65V	V_{IN}=12V		0.6	2	mA
		V_{IN}=V_{REF}=5V		0.7	2	
		V_{IN}=V_{REF}=3.3V		0.6	2	
Output regulation accuracy	V_{FB} peak		0.593	0.6	0.607	V
Output regulation hysteresis				22		mV
FB Propagation Delay	FB falling to LG falling			50		ns
	FB rising to HG falling			70		ns
Overvoltage-Protection(OVP) Threshold			0.7	0.75	0.8	V
High-Side Current – Sense Program Current	T_A=85°C			60		uA
	T_A=25°C		42.5	50	57.5	uA
Soft-Start internal Resistance			60	80	100	K
Fault Hiccup Internal SS Pulldown Current	V_{SW}<V_{ILIM} and V_{FB}<V_{SS}			230		nA
HG Driver Resistance	Sourcing Resistance			2.1		Ω
	Sinking Resistance			1.6		
LG Driver Resistance	Sourcing Resistance			2.2		Ω
	Sinking Resistance			1.1		
Dead time	HG low to LG high and LG low to HG high(adaptive)			40		ns
HG Minimum On-Time				100	200	ns
LG Minimum On-Time	Normal operation			100	200	ns
	Current fault			475		ns
Thermal Shutdown	Rising temperature, hysteresis=20(typ)			140(6)		°C

Notes:

5) If IN Supply Voltage is lower than 5V, circuit can keep work but the efficiency will be lower.

6) Guaranteed by design

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

PIN FUNCTIONS

Pin#	Name	Description
1	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback reference voltage is 0.59V. *See Setting the Output Voltage.*
2	SS	Soft-start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.01uF external capacitor sets the soft-start period to 4ms with an internal 84Kohm resistor. An internal 250nA current sink in hiccup mode gives approximately 10% duty cycle during fault conditions.
3	REF	Internal 5V LDO output. Bypass REF to GND with a 4.7uF or greater capacitor.
4	GND	Ground. Connect the exposed pad to pin 4
5	LG	Low-side Gate-Drive output. Drive the synchronous-rectifier MOSFET. Connect this pin to the gate of the synchronous MOSFET.
6	BST	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-channel MOSFET switching. Connect a 0.1uF or greater capacitor from SW to BST to power the high side switch. MP2905 contains an internal BST regulator, so external schottky from REF to BST is not necessary.
7	SW	Switch Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
8	HG	High-side gate-drive output. Drive the high-side MOSFET. Connect this pin to the gate of the high-side MOSFET
9	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 3V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Setting the Input Capacitor*.
10	ILIM	Current-limit threshold Set pin. A appropriate resistor should be connected between this pin and the drain of high-side MOSFET (IN). An internal 50uA current sink sets a voltage drop in the resistor. The voltage drop compares to high-side MOSFET voltage drop (Vds) to set the peak current-limit threshold.

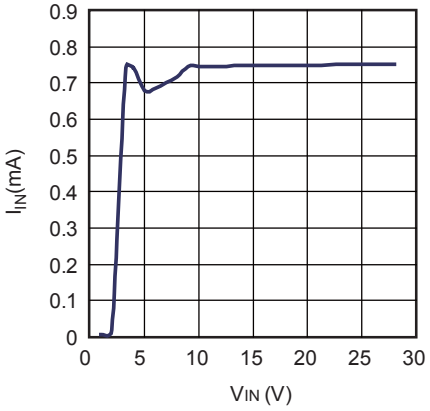
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

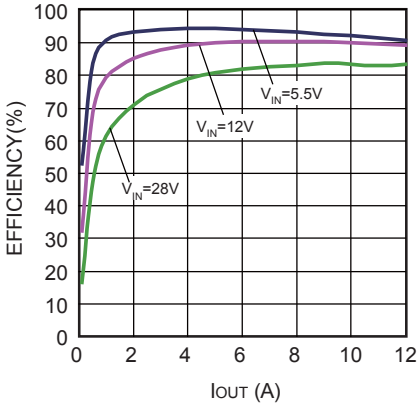
V_{IN}=12V, V_{OUT} =1.8V, I_{OUT}=12A, L1=1.5μH(DCR=3.41mΩ), C_{OUT}=100μF *2+330μF, T_A=+25°C, High Side MOS:SI7112DN-T1-E3, Low Side MOS:SI7336ADP-T1-E3 unless otherwise noted.

Supply Current (no switching) vs. Input Voltage

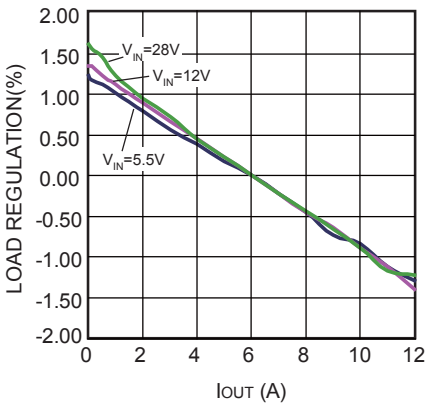
V_{FB}=0.65V



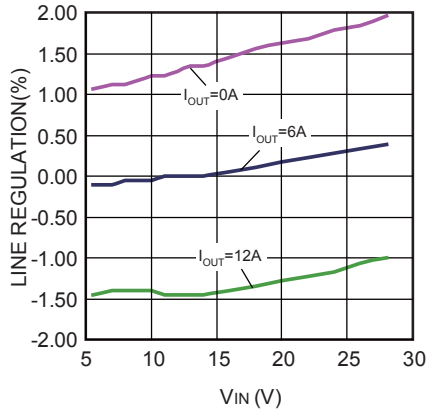
Efficiency



Load Regulation

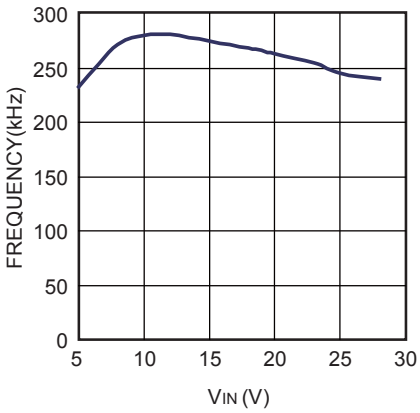


Line Regulation



Frequency vs. Input Voltage

no load, Feedforward Cap=22nF

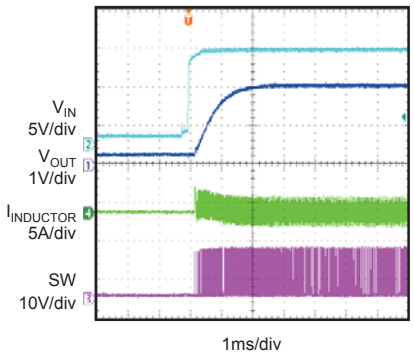


MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

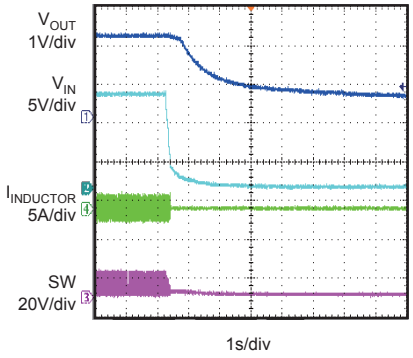
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.8V, I_{OUT}=12A, L1=1.5µH, C_{OUT}=100µF *2+330µF, T_A=+25°C, unless otherwise noted.

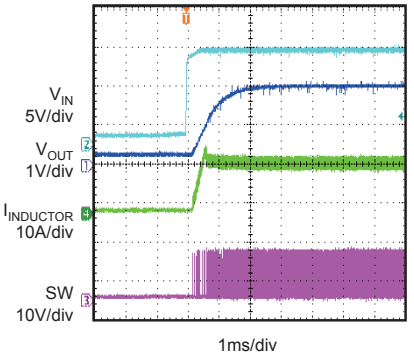
V_{IN} Power up
I_{OUT}=0A



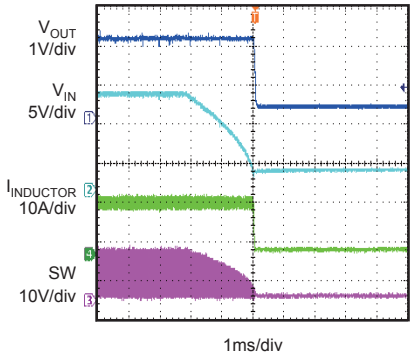
V_{IN} Power off
I_{OUT}=0A



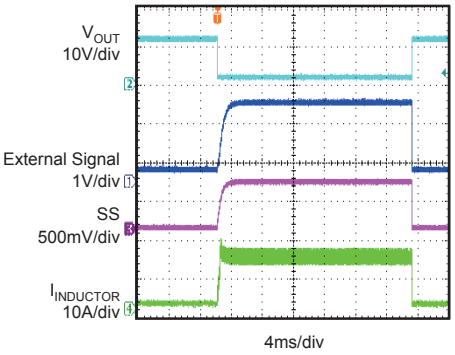
V_{IN} Power up
I_{OUT}=12A



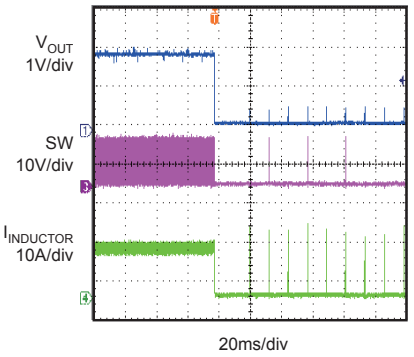
V_{IN} Power off
I_{OUT}=12A



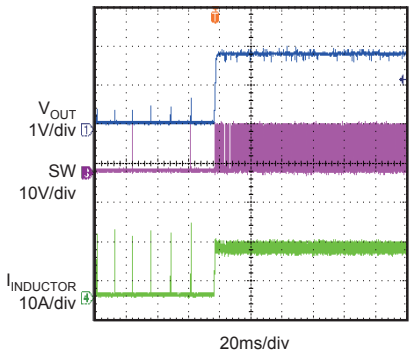
Start up and Shut down by Pull down and Release SS



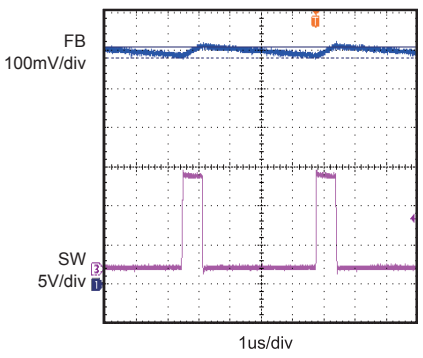
Short Entry



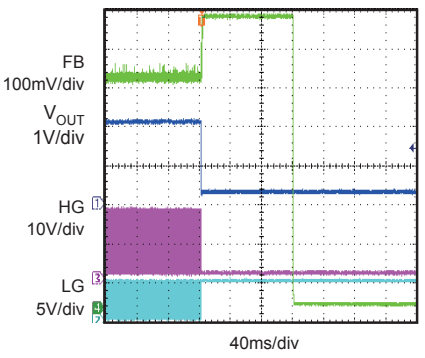
Short Recovery



FB Peak and Hysteresis



FB OVP



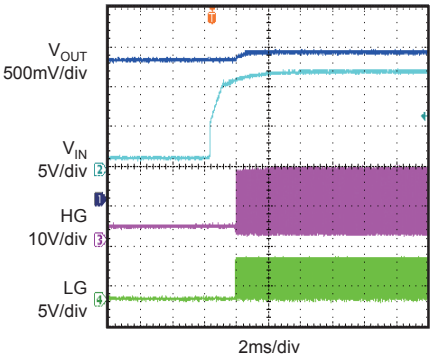
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.8V, I_{OUT}=12A, L1=1.5µH, C_{OUT}=100µF *2+330µF, T_A=+25°C, unless otherwise noted.

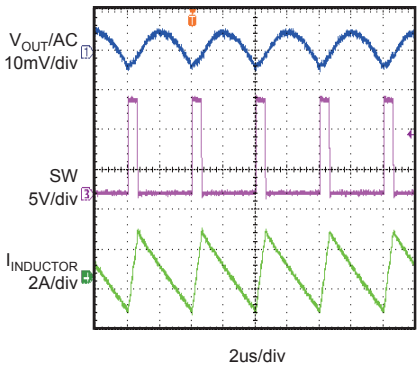
Pre-bias Test

Pre-bias Output Voltage=1.7V



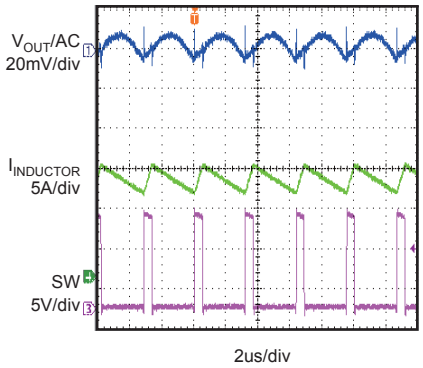
Output Ripple Voltage

I_{OUT}=0A, V_{OUT_RIPPLE}=18mV



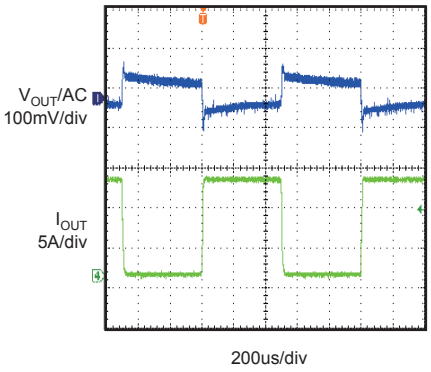
Output Ripple Voltage

I_{OUT}=12A, V_{OUT_RIPPLE}=17.6mV



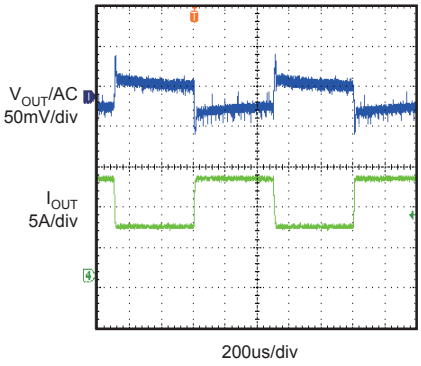
Load Transient Response

I_{OUT}=0A~12A@1A/us



Load Transient Response

I_{OUT}=6A~12A@1A/us



MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

FUNCTION DIAGRAM

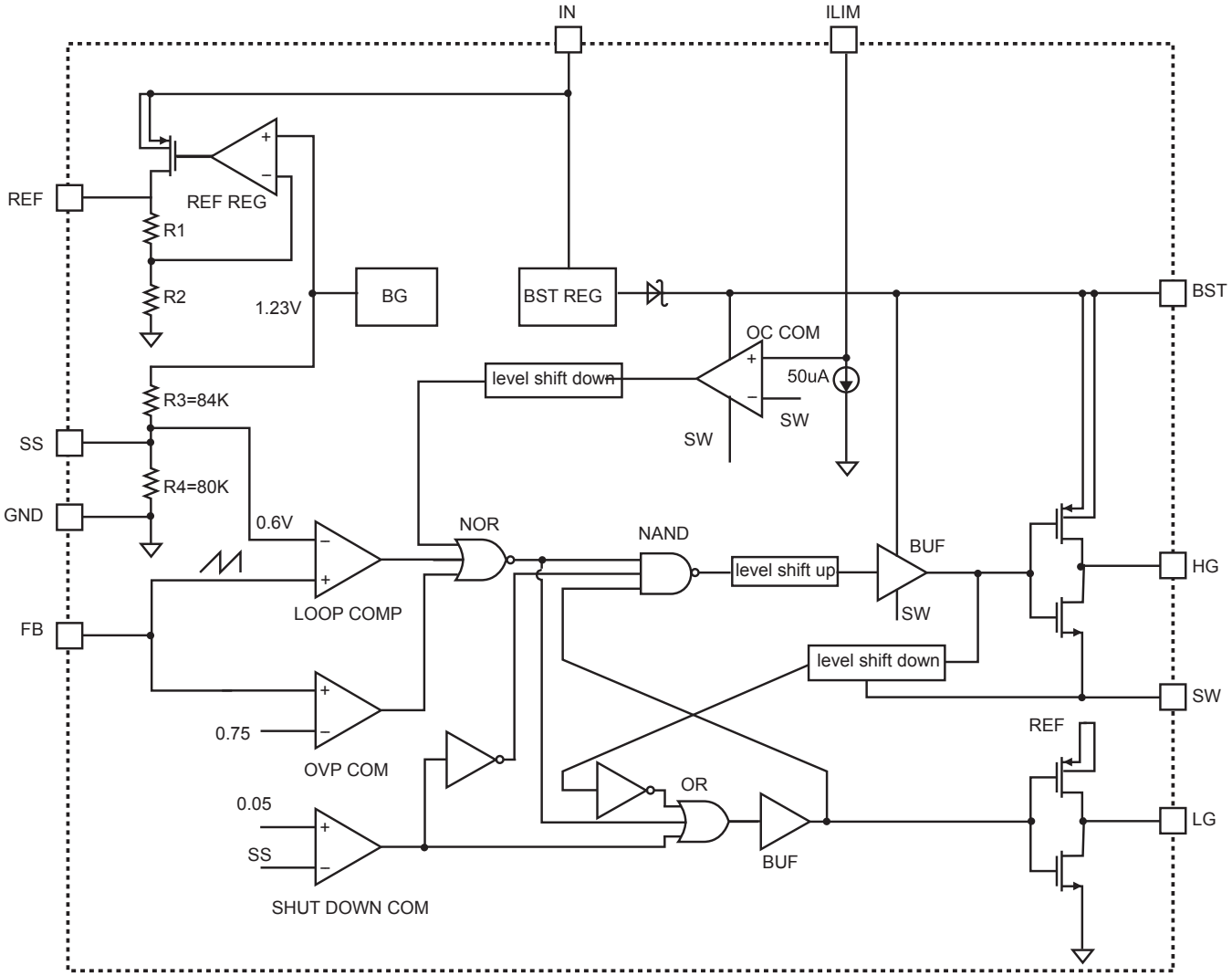


Figure 1—Functional Block Diagram

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

OPERATION

MP2905 uses a hysteretic control loop to regulate output voltage. It senses the voltage at FB pin, which is compared with SS voltage with 20mV hysteresis. When FB is lower than SS 20mV, high side switch turns on and FB voltage rises up. After FB voltage reaches SS voltage, high side switch turns off and low side switch turns on, which cause FB voltage drop until FB is lower than SS 20mV. So Vout is regulated at a stable voltage because FB voltage is regulated at the voltage (SS-10mV). See the setting output voltage for detailed information. Hysteretic voltage-mode control provides fast transient response without additional loop compensation.

Soft-start

An external cap is connected at SS pin to realize soft-start function. When SS pin pull down transistor turns off, internal reference begins to charge SS external cap through a resistor-divider. So FB rises slowly following SS voltage and inrush current is avoided. Soft-start time is determined by external cap and internal resistor-divider.

If SS has pre-bias voltage at startup, both HG and LG keep low, SS cap begins to discharge until lower than 50mV. Then SS will rise slowly and FB tracks SS.

Startup Sequence

In MP2905, at startup, if FB>SS, which means output has pre-bias voltage, HG and LG don't toggle until SS greater than FB.

Current Limit Function

A resistor is connected from the Drain of the high side MOSFET to ILIM pin to set current limit value. Internal 50uA current sink from ILIM to GND limits the maximum VDS cross high side switch drain and source. When VFB<300mV, if high side switch current hits the current limit, high side switch turns off immediately. If VFB>300mV, over current event occurs in four sequential cycles, high side switch turns off. Once high side MOSFET turns off, SS cap will be discharged by 250nA current. After SS voltage is lower than 50mV, SS cap is stopped discharging and high side switch tries to turn on again.

Output Over-voltage protection

Output over-voltage is monitored by FB voltage. If FB voltage higher than 750mV, HG is set low and LG is set high. This status will be latched until restart EN or VIN.

Enable

MP2905 turns off by pulling down SS pin to lower than 50mV. Releasing SS will start the run cycle.

High Side Gate Driver

MP2905 doesn't need Schottky, but still needs 0.1uF BST cap between BST pin and SW pin.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator (REF). This regulator takes V_{IN} input and operates in the full input range. When V_{IN} is greater than 5.0V, the output of the regulator is full regulation. When V_{IN} is lower than 5.0V, the output decreases. Bypass REF pin to GND with a 4.7uF or greater capacitor.

Under Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage.

The MP2905 UVLO comparator monitors the output voltage of the internal regulator (REF).

Thermal protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the part will be shut down and allow the chip to cool. When the IC is cool enough, the part will be turned on again. There is a built-in hysteresis.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page).

R1 is for approximately 50μA to 150μA bias current in the resistor-divider. A wide range of resistor R1 value is acceptable, choosing a typical value 6.04k, R3 is determined by:

$$R3 = R1 \times (\frac{Vout + 0.01V + (R_{DC} \times 0.5 \times I_{LOAD})}{V_{FB}} - 1)$$

where V_{FB} = 0.590V, R_{DC} is the DC resistance of the output inductor, I_{LOAD} is the full load current, 0.5*I_{LOAD} is half load condition, it's for Load regulation standard. The term 0.01V is to reflect 1/2 of the feedback threshold hysteresis. But R3 value also can't be too large, or circuit may work abnormally.

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will is favorable to less ripple current and the lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series DC resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L1 = \frac{V_{OUT}}{f_S \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

where I_{LOAD} is the full load current.

Setting Current Limit

MP2905 current limit can be set by an external resistor (R2) which is connected between ILIM pin and the drain of the high side MOSFET. An internal 50uA sink current sets a voltage drop on the resistor. The voltage drop compares to high-side MOSFET voltage drop (Vds) to set the peak current limit threshold. Below is the diagram of current limit function:

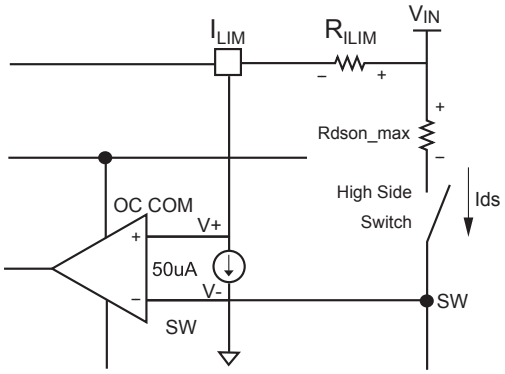


Figure 2—Current Limit Functional Diagram

The voltage drop on the high side MOSFET is:

$$V_{DS_ON}(max) = I_{DS}(max) \times R_{DS_ON}(max)$$

Where I_{DS}(max) equals the max peak inductor current I_{LP} (max).

Then, R_{ILIM} can be calculated using the V_{DS_ON}(MAX) with the following formula:

$$R_{ILIM} = \frac{V_{DS_ON}(max)}{50uA}(\Omega)$$

And R_{ILIM} should be kept in the range of 1kΩ~ 8kΩ.

Selecting Power MOSFETs

The MP2905 connects two external, logic-level, n-channel MOSFETs as the circuit switching elements. The MOSFETs are the key points for circuit efficiency. The major parameters we should concern are:

1) On-resistance, R_{DS_ON}: the lower, the better it will be.

2) Continuous Drain Current (@10sec), I_D: it should be higher than the peak current @ full load condition. And pay attention to I_D's variation with different temperature.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

3) Maximum drain-to-source voltage, V_{DS}(MAX): it should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.

4) Total gate charge Qg: the lower, the better it will be. For high-side MOSFET, the main power loss consists of conduction loss, switching loss, and drive loss. The high-side MOSFET conduction loss can be calculated by:

$$P_{high-side_conduction} = I_{LOAD}^2 \times R_{highside_DSON} \times D$$

Where D is the duct cycle, it's defined by:

$$D = \frac{V_{OUT}}{V_{IN}}$$

High-side MOSFET switching loss is calculated by:

$$P_{high-side_switching} = \frac{1}{2} V_{IN} \times I_{LOAD} \times (t_{ON} + t_{OFF}) \times f_S$$

Where t_{ON} is high-side MOSFET turn on time, t_{OFF} is high-side MOSFET turn off time, f_S is the switching frequency.

High-side MOSFET drive loss is calculated by:

$$P_{high-side_drive} = Q_{g_high-side} \times f_S \times V_{drive}$$

Where Vdrive is the high-side MOSFET driving voltage, typical value is 5V.

For low-side MOSFET, there isn't switching loss, conduction loss is the main loss, so we'd better choice a MOSFET with lower Rds-on than high side MOSFET. The recommended Rds-on of low side MOSFET is one-third of high-side MOSFET. The low-side MOSFET loss consists of conduction loss, drive loss and body diode conduction loss. The Low-side MOSFET conduction loss is calculated by:

$$P_{low-side_conduction} = I_{LOAD}^2 \times R_{low-side_DSON} \times (1 - D)$$

Low-side MOS drive loss is calculated by:

$$P_{low-side_drive} = Q_{g_low-side} \times f_S \times V_{drive}$$

Body diode conduction loss is calculated by:

$$P_{bodydiode} = 2 \times V_F \times I_{LOAD} \times t_{deadtime} \times f_S$$

Where V_F is body diode forward voltage drop, $t_{deadtime}$ is high-side MOSFET and low-side MOFETS transition time.

Except the losses above, there still is output cap loss in both high side MOSFET and low side MOSFET. Output cap loss is defined by:

$$P_{Cds} = \frac{1}{2} \times C_{DS} \times V_{DS}^2 \times f_S$$

where C_{DS} is the output cap of MOSFET.
For less switching noise, add drive resistors in series with the gate of MOSFET to slow down the transition between the high-side MOSFET and low-side MOSFET switching.

Selecting the Feed Forward Capacitor

The feed forward capacitor (C8 in front page typical application circuit) is a key factor to affect the frequency. It can be calculated by:

$$f_S == \frac{1}{R_{FB} \times C8} \times \frac{V_{FB}}{V_H + \frac{1}{C8}(90ns \times \frac{V_{IN}}{R_3} - 20ns \times \frac{V_{FB}}{R_{FB}})} \times (1 - \frac{V_O}{V_{IN}})$$

Where f_S is desired the frequency, V_{FB} is feedback reference voltage, typical is 590mV, V_H is output regulation hysteresis, typical value is 22mv, R_{FB} is the equivalent value of two voltage-divided resistors. For example, in 2905 typical application:

$$R_{FB} = \frac{R1 \times R3}{R1 + R3}$$

Select an X7R ceramic capacitor with the closest Capacitance to the value calculated as possible. Increase the Capacitance, the switching frequency decrease, and vice versa, decrease the Capacitance, the frequency increase.

And output capacitor, inductor and inductor DCR will affect the frequency, too, but those are limited.

The frequency calculated by the formula has a deviation within 30%.

Setting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

Since the input capacitor (Cin) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{Cin} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where

$$I_{Cin} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input terminal. The input voltage ripple can be estimated by capacitance:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C_{in}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Setting the Output capacitor

The output capacitor (Cout) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}})$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple is:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L1 \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple is:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the transient response and the stability of the regulation system. Higher voltage ripple will influence the voltage of the feed forward capacitor to make the system be unstable. So, at the condition which the tantalum or electrolytic capacitors with higher ESR is used or output current is higher, a RC filter is necessary from Vout to GND. Connect the resistor of filter between the Vout and feed forward capacitor, and connect the capacitor of filter from feed forward capacitor to GND. Follow the R7 and C12 connection in MP2905 typical application. 10Ω/1uF or 2Ω/4.4uF is recommended for good stability and better transient response.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

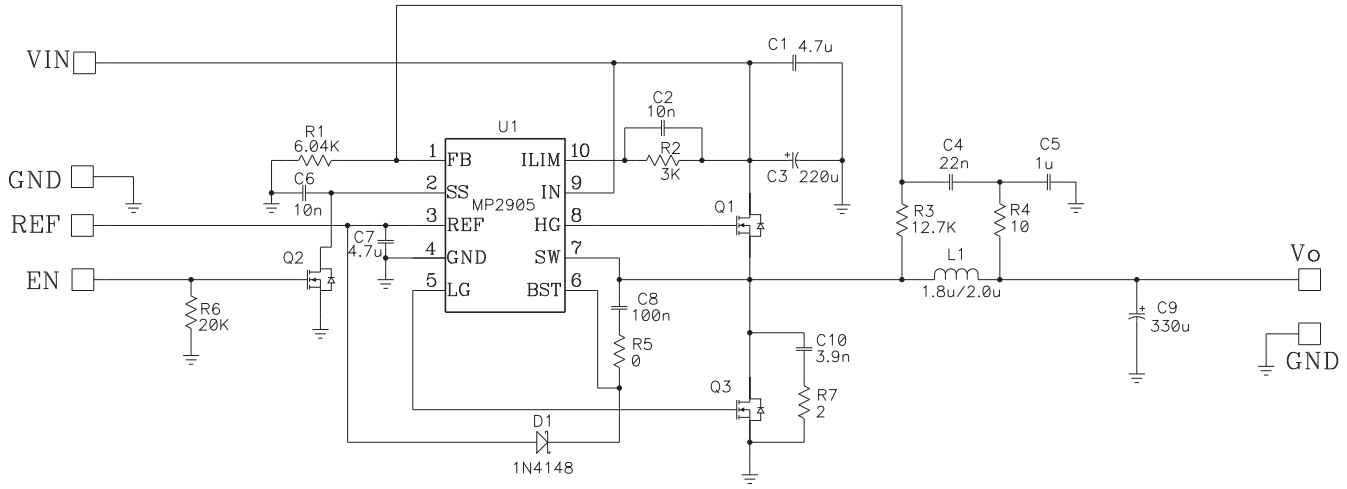


Figure 3—Typical Application Circuits for 12A Output

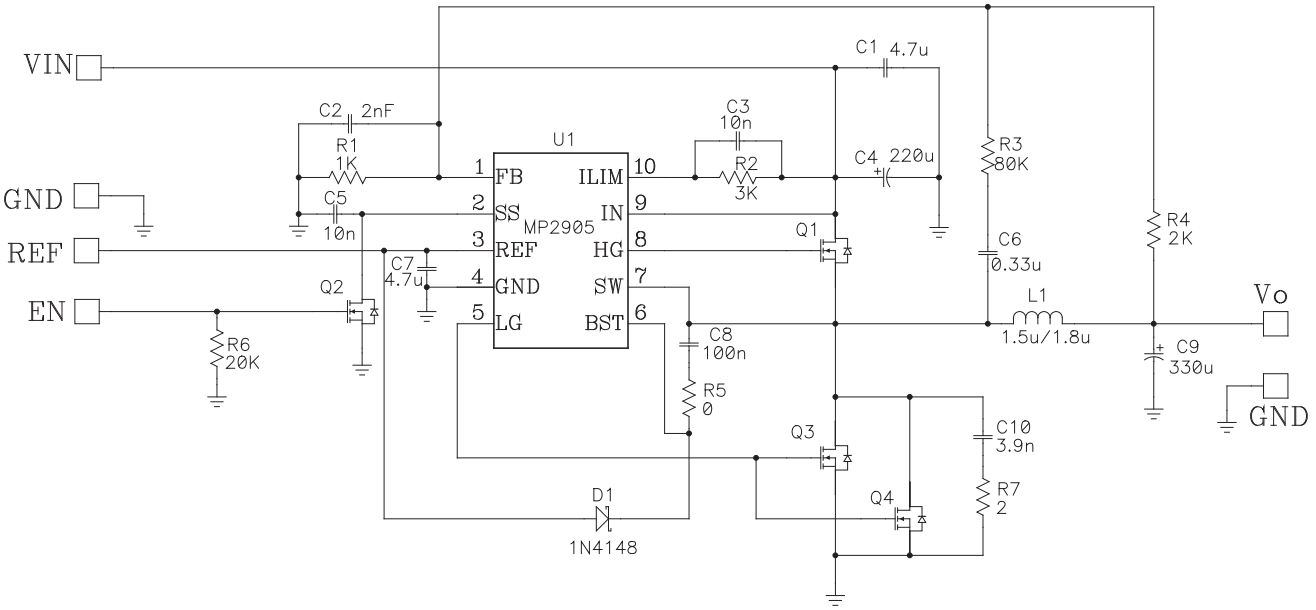


Figure 4—Typical Application Circuits for 25A Output without Droop(7)

Note:

7) For 25A application design, please refer to MPS special application note for 25A application.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines:

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET.
2) IC bypass ceramic capacitors are suggested to be put close to the IN Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to improve chip thermal performance and long term reliability.
6) It is suggested to add the snubber circuit across the high side MOSFET (IN pin and SW pin) so as to reduce the SW spike.
7) If output current is higher than 10A, recommend to use a four layers PCB, and pour ground in mid layer.

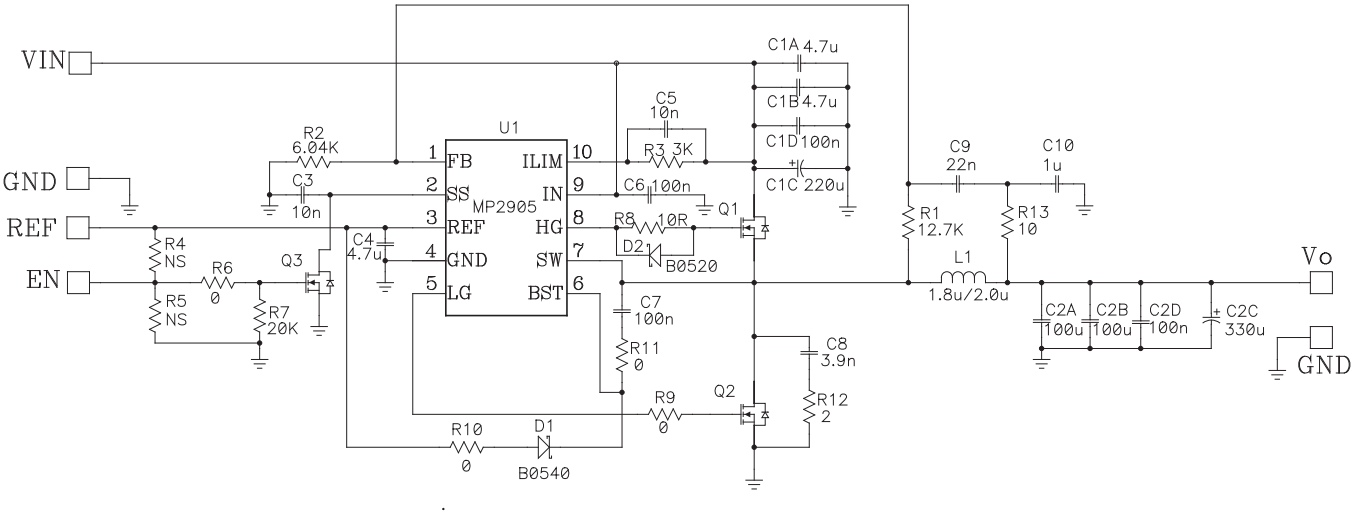
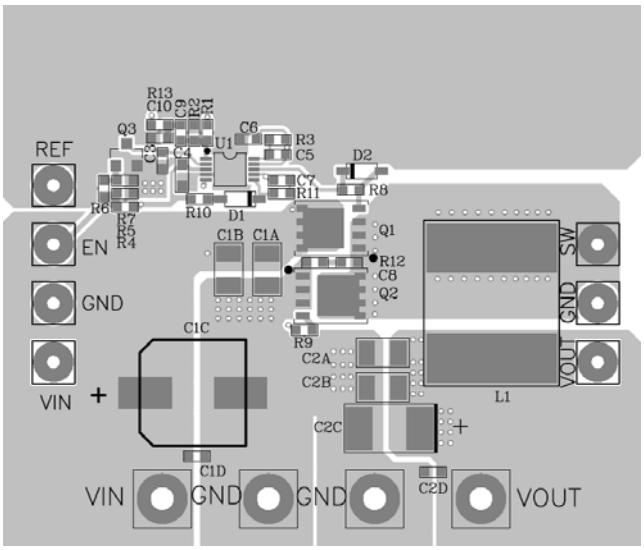
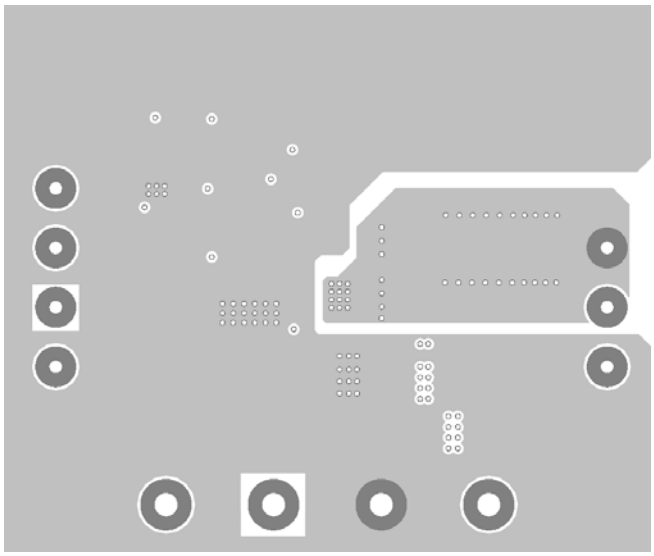


Figure 5—MP2905 Application Circuit

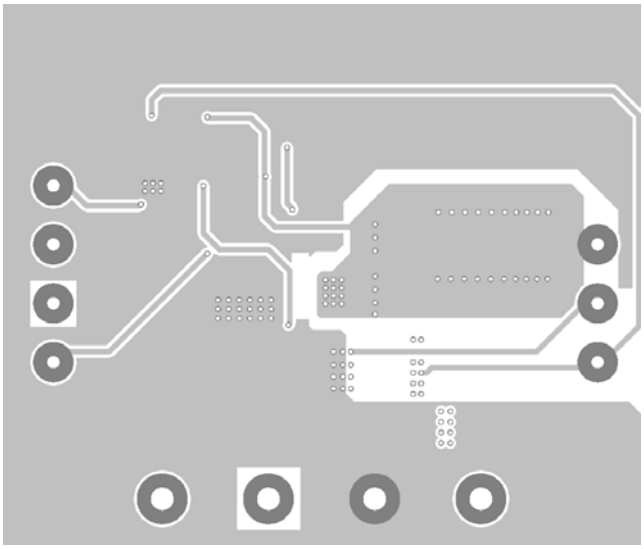
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.



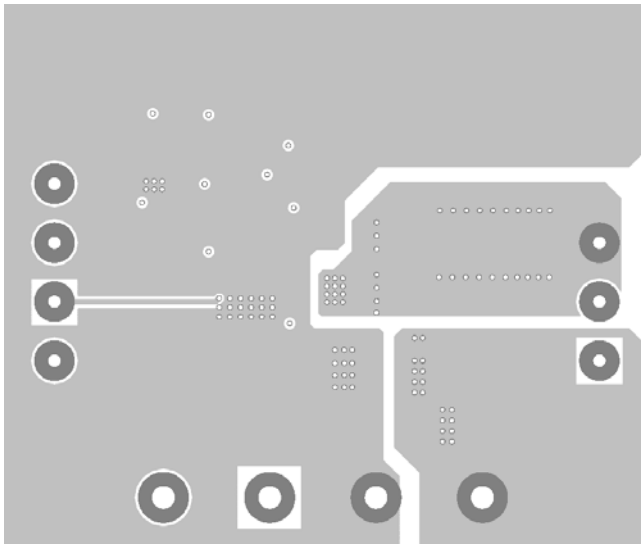
Top Layer



IN1



IN2



Bottom Layer

Figure 6—MP2905 Application Circuit and PCB Layout Guide

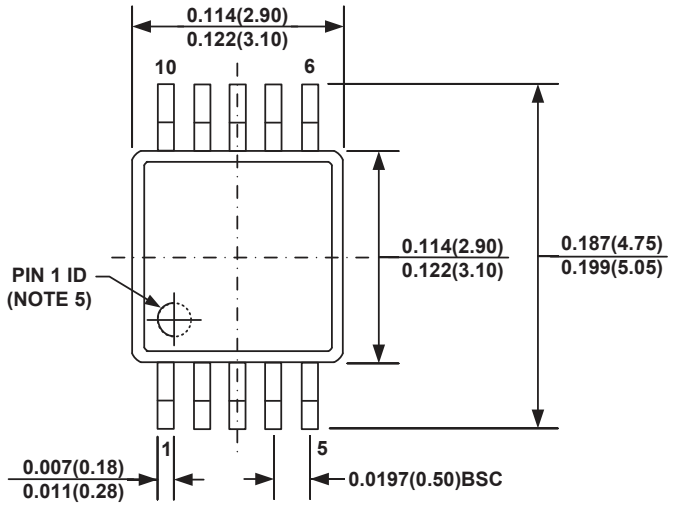
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.

PACKAGE INFORMATION

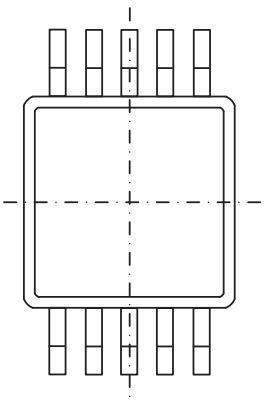
MSOP10

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

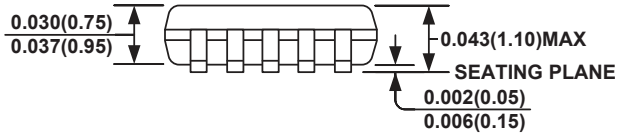
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2015. All Rights Reserved.



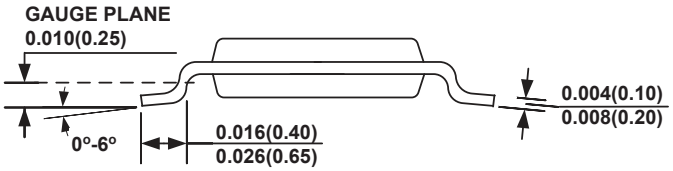
TOP VIEW



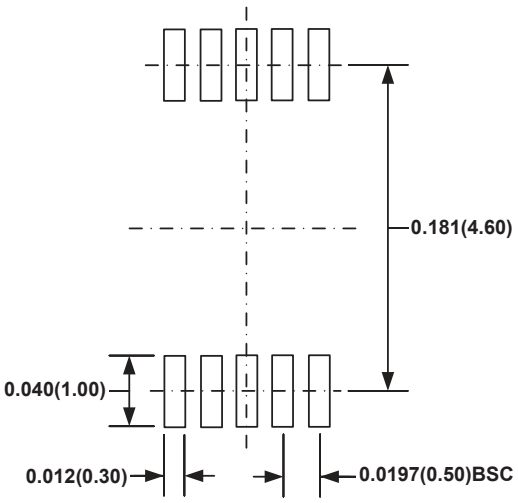
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.