MP28160

5.5V/0.5A High-Efficiency Integrated Buck-Boost Converter with 3.3V Fixed Output in 1.4x1.8mm CSP Package

DESCRIPTION

The MP28160 is an integrated buck-boost converter in a small CSP package. The buck-boost converter can operate from an input voltage above, equal to, or below the output voltage. It uses current mode control with a 1.8MHz fixed PWM frequency to optimize stability and transient response. In a light load condition, it enters auto PFM/PWM mode to get high light load efficiency. Integrated MOSFETs minimize the solution size while maintaining high efficiency.

Fault protection includes output hiccup current limiting, OVP, and thermal shutdown.

The MP28160 is available in a tiny CSP-12 (1.4mmx1.8mm) package.

FEATURES

- 2.5V to 5.5V Input Voltage Range
- 1.8MHz Switching Frequency for CCM
- 3.3V Fixed Output Voltage
- 500mA Continuous Output Current
- 1ms Soft-Start Time
- Auto PFM/PWM Mode
- Output Over-Voltage Protection
- Hiccup Over-Current Protection
- 1μA Shutdown Current
- Active Low System EN Pin
- Over-Temperature Shutdown
- Available in a Wafer Level Chip Scale Packaging: CSP-12(1.4mmx1.8mm)

APPLICATIONS

- USB-C Cable
- Thunderbolt
- Portable Devices

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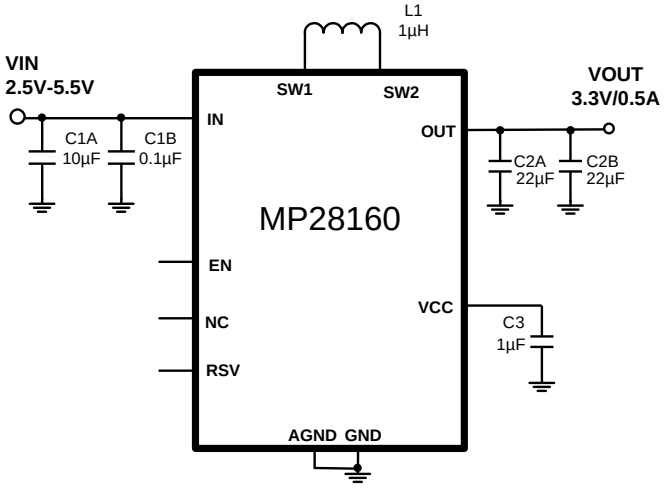
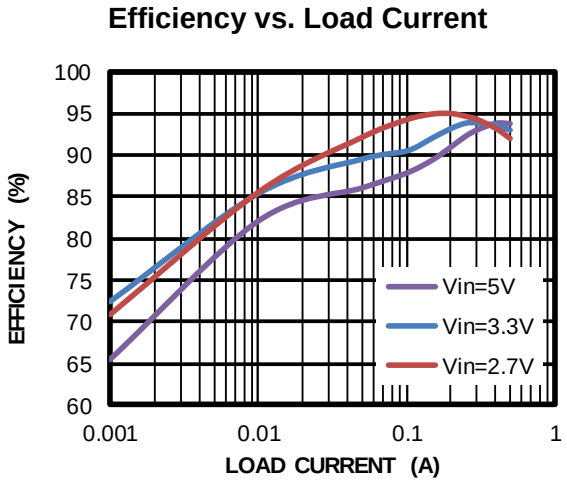
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP28160GC	CSP-12(1.4mmx1.8mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP28160GC–Z)

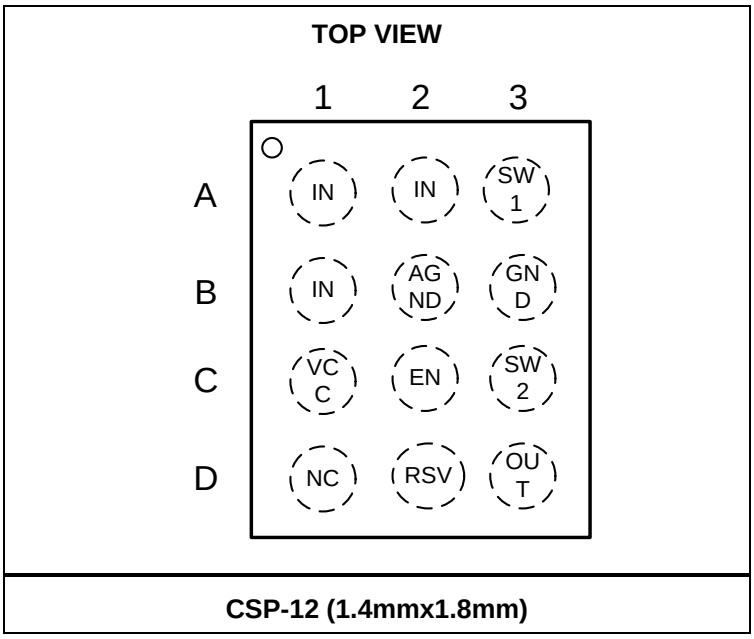
TOP MARKING

JLY

LLL

JL: Product code of MP28160GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



CSP-12 (1.4mmx1.8mm)

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PIN FUNCTIONS

CSP-12 Pin #	Name	Description
A1, B1, A2	IN	**The buck-boost input pin**. The MP28160 operates from a 2.5V to 5.5V VIN voltage. Place a 10µF or larger capacitor for decoupling.
A3	SW1	**Switch1.** The first half-bridge switch node is connected to SW1. Connect an inductor between SW1 and SW2.
B2	AGND	**Analog ground.** Connect it to GND.
B3	GND	**Power ground.** Reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect to GND with copper traces and vias.
C1	VCC	**Internal 5V LDO regulator output.** Decouple with a 1µF capacitor.
C2	EN	**On/off control for entire chip.** EN is active low. Drive EN high to turn off the chip; drive EN low, or float, to turn on the device. It has internal 600kΩ pull-down resistor to ground.
C3	SW2	**Switch2**. The internal second half-bridge switch node is connected to SW2. Connect an inductor between SW1 and SW2.
D1	NC	**No connection.**
D2	RSV	**Reserved pin.** RSV must be left floating or shorted to GND.
D3	OUT	**Output pin.**

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}).....-0.3V to +6V
V_{SW1}.....
–0.3V (-5V for <10ns) to V_{IN} + 0.3V (10V for <10ns)
V_{SW2}.....
–0.3V (-5V for <10ns) to V_{OUT} + 0.3V (10V for <10ns)
V_{EN} .....-0.3V to +5.5V
All Other Pins.....–0.3V to +6V
Continuous Power Dissipation (TA = +25°C) (2)
CSP-12 (1.4mmx1.8mm) 1.14W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Operation Input Voltage VIN.....2.5V to 5.5V
Output Current 500mA
Operating Junction Temp. (TJ). -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
CSP-12 (1.4mmx1.8mm)	110	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application

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ELECTRICAL CHARACTERISTICS

V_{IN} =5.0V, V_{EN} = 0V, T_J = -40°C to +125°C(5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN}=5V, VIN=5V, T_J=25°C		1	10	μA
Supply current (quiescent)	I_Q	V_{EN}=0V, VIN=5V, No switching, T_J=25°C		220	280	μA
EN logic high input	V_{EN_H}	Disable Part	1.2			V
EN logic low input	V_{EN_L}	Enable Part			0.4	V
EN to ground resistance	R_{EN}			600		kΩ
Thermal shutdown(6)	T_{STD}			150		°C
Thermal hysteresis(6)	T_{HYS}			20		°C
VCC regulator	V_{CC}	VIN=5.5V	4.5	5	5.5	V
VCC load regulation	V_{CC_RG}	I_{CC}=0-5mA		3	5	%
Buck-Boost						
Input under-voltage lockout rising threshold	V_{IN_R}		2.05	2.25	2.45	V
Input under-voltage lockout hysteresis voltage	V_{IN_F}			150		mV
Output voltage	V_{OUT}		-1.5%	3.3	+1.5%	V
Output over-voltage protection	$V_{OUT_OVP_R}$		110%	115%	120%	V_{OUT}
Output OVP recovery	$V_{OUT_OVP_F}$			105%		V_{OUT}
OVP discharge resistance	R_{DIS}			1		kΩ
Oscillator frequency	Fs		1.45	1.8	2.15	MHz
Peak current limit	I_{LIM}	V_{OUT}=0V	1.65	2.5	3.35	A
SWD valley current limit(7)				-1.5		A
PMOS on resistance	$R_{DS(on)-P}$	SWA, SWD, 3.3Vin, 3.3Vout		90		mΩ
NMOS on resistance	$R_{DS(on)-N}$	SWB, SWC, 3.3Vin, 3.3Vout		80		mΩ
Soft-start time	Is	0-100%Vout		1		ms

5) All min/max parameters are tested at T_J=25ºC. Limits over temperature are guaranteed by design, characterization, and correlation.
6) Guaranteed by design.
7) Guaranteed by engineering sample characterization.

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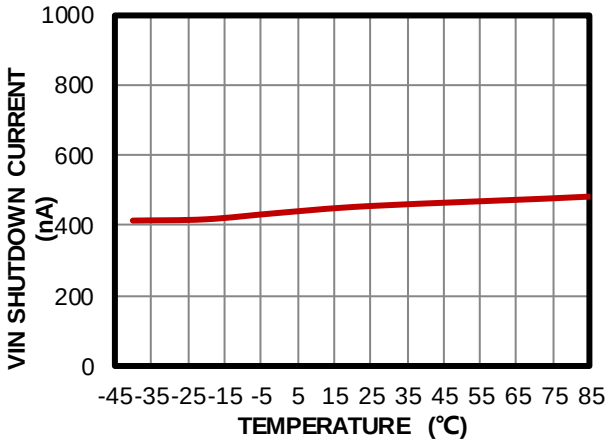
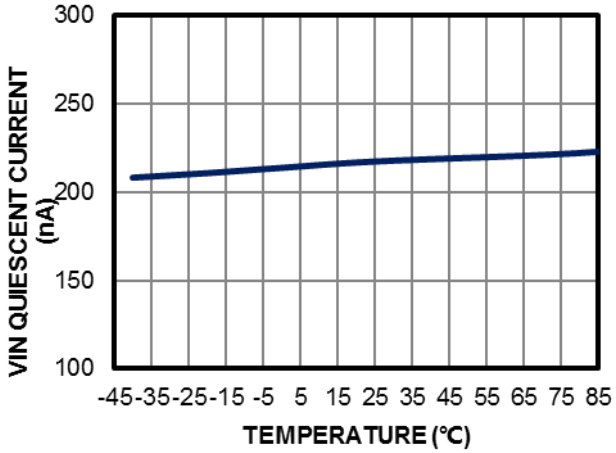
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

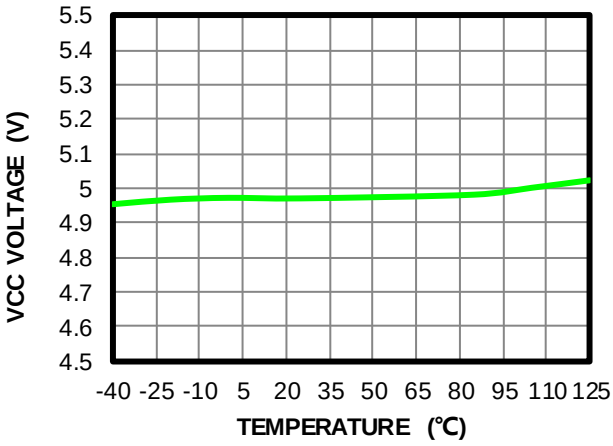
VIN Shutdown Current vs. Temperature, V_{IN} = 5V



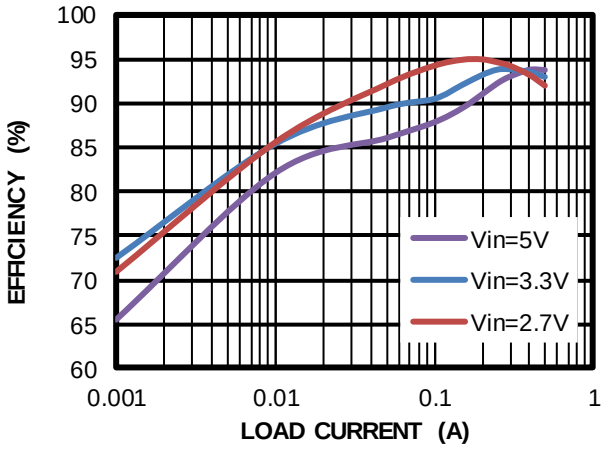
VIN Quiescent Current vs. Temperature, V_{IN} = 5V



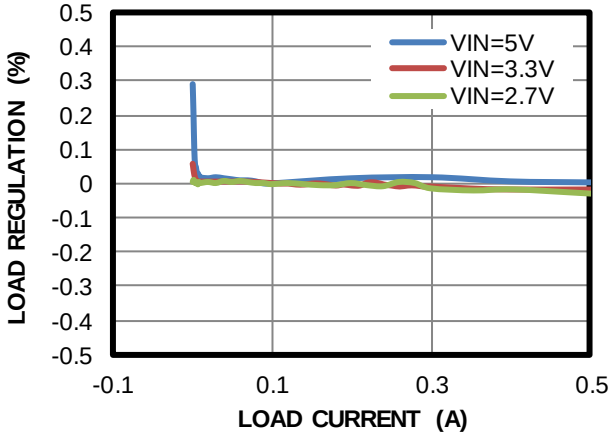
VCC Voltage vs. Temperature



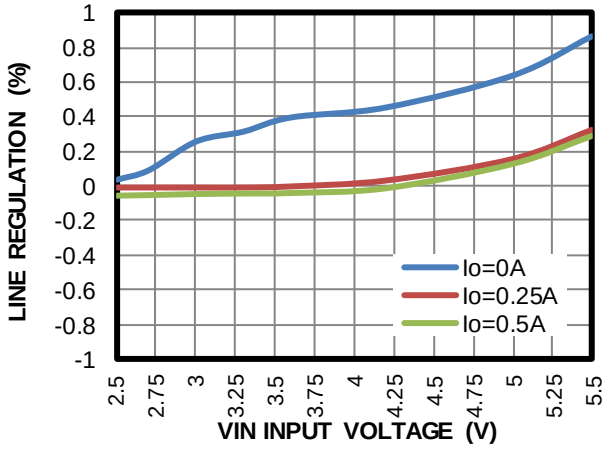
Efficiency vs. Load Current



Load Regulation



Line Regulation



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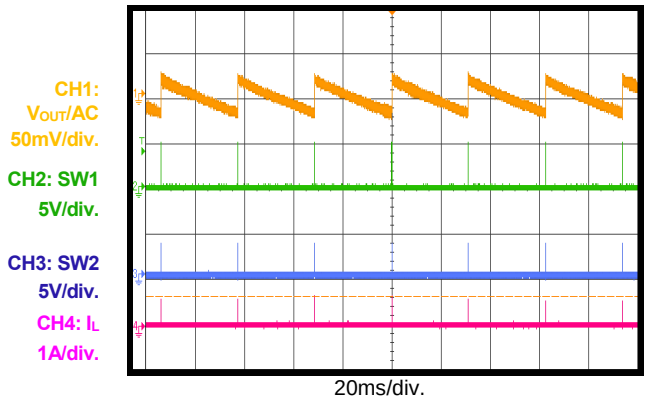
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

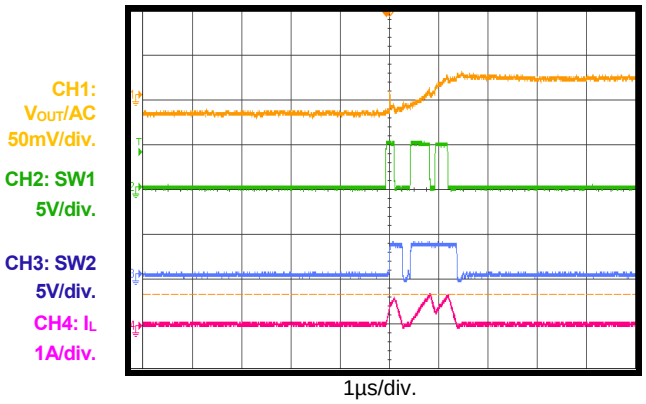
Output Ripple

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



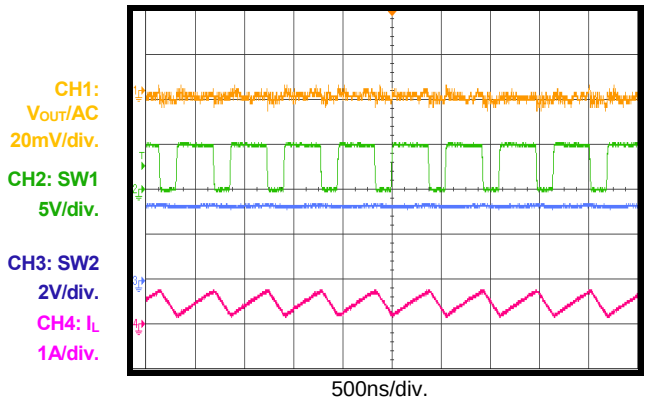
Output Ripple

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



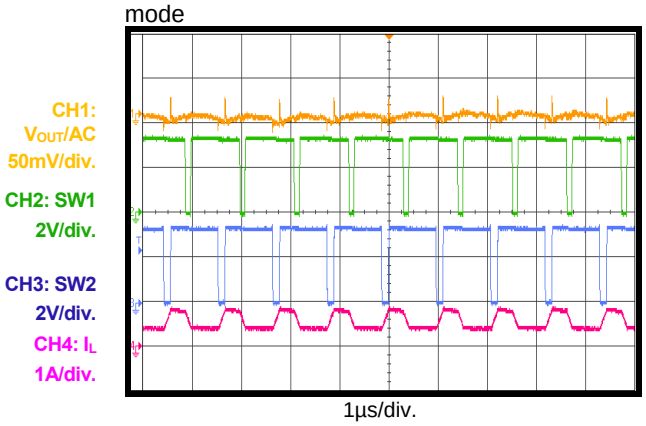
Output Ripple

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.5A



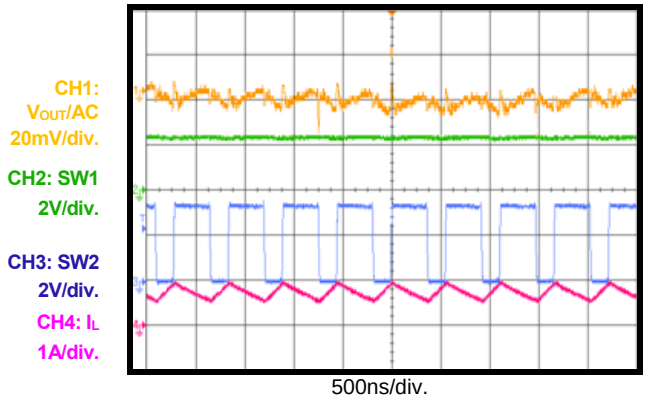
Output Ripple

V_{IN}=3.3V,V_{OUT}=3.3V, I_{OUT}=0.5A,Buck-boost mode



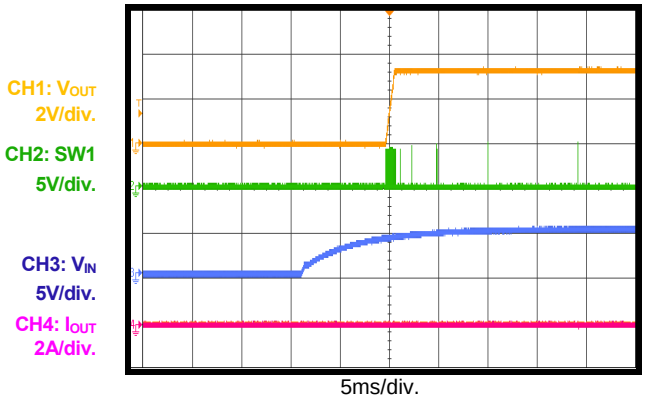
Output Ripple

V_{IN}=2.5V , V_{OUT}=3.3V, I_{OUT}=0.5A, Boost mode



Power Start-Up

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



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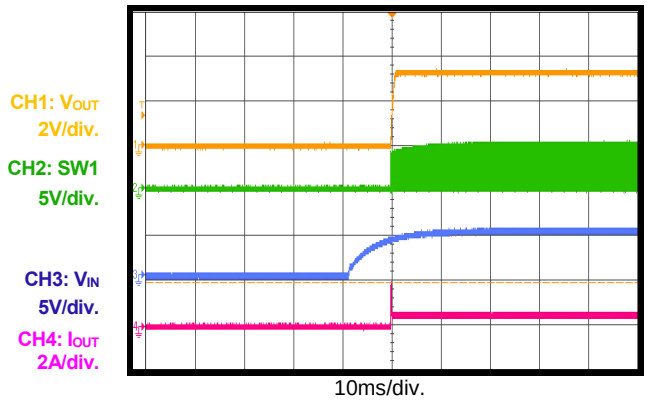
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}= 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

Power Start-Up

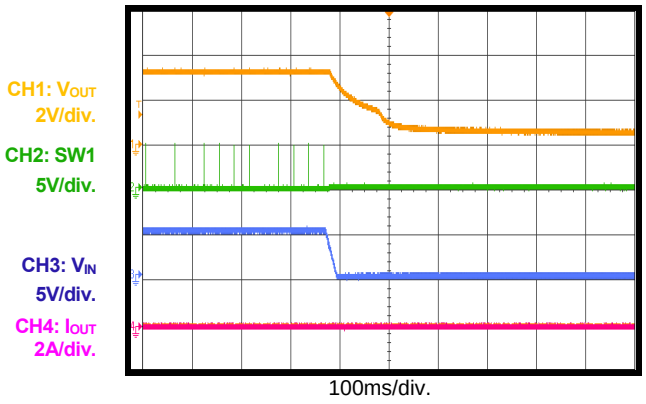
V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.5A



10ms/div.

Power Shutdown

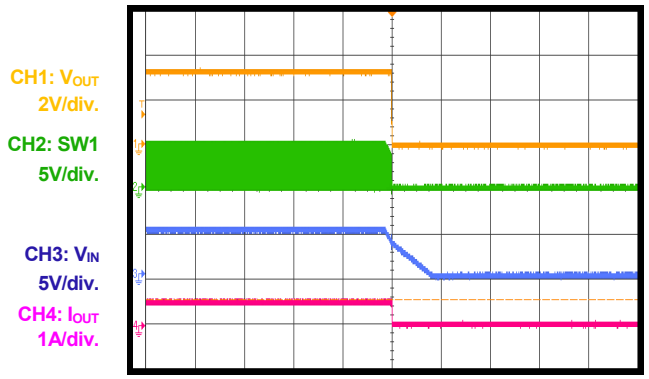
V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



100ms/div.

Power Shutdown

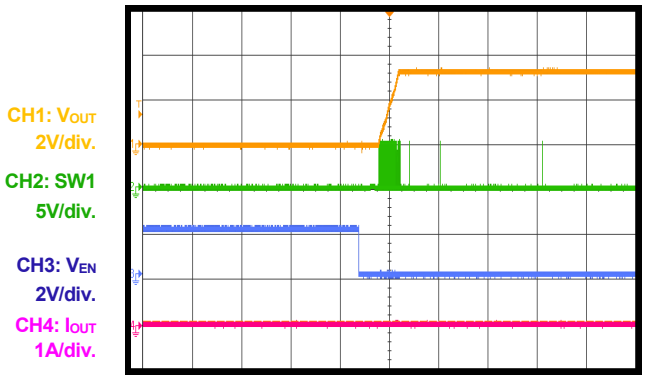
V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.5A



20ms/div.

EN Start-Up

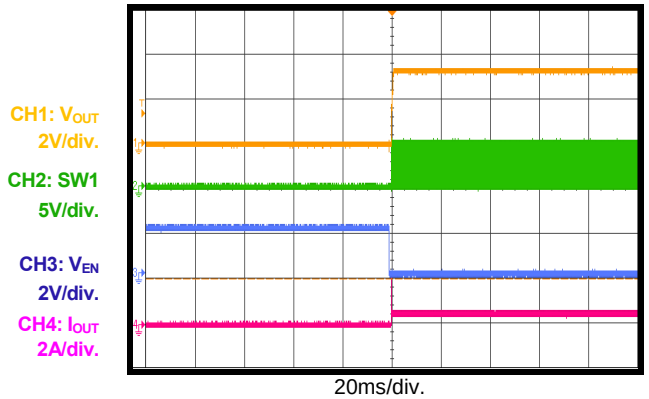
V_{IN}=5V,V_{OUT}=3.3V, I_{OUT}=0A



2ms/div.

EN Start-Up

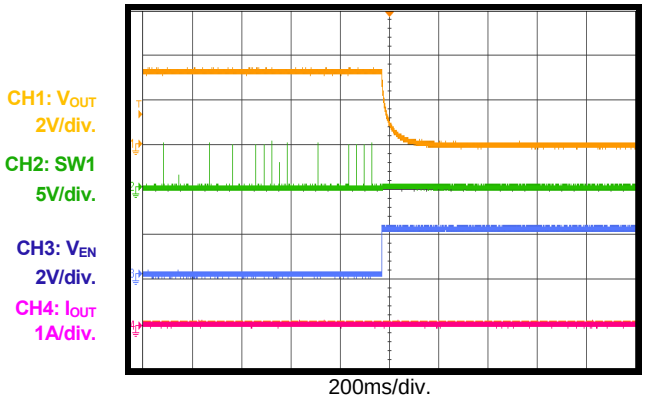
V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.5A



20ms/div.

EN Shutdown

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



200ms/div.

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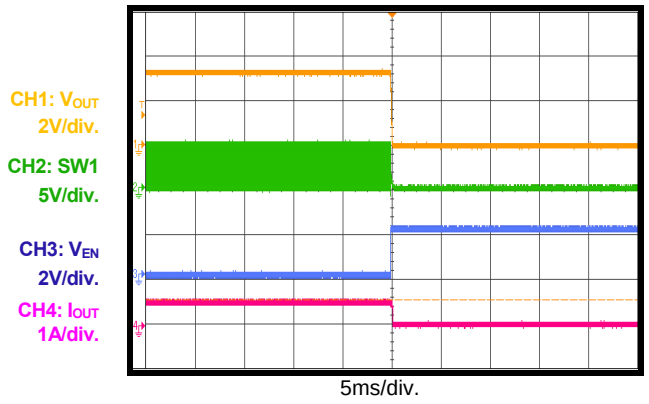
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

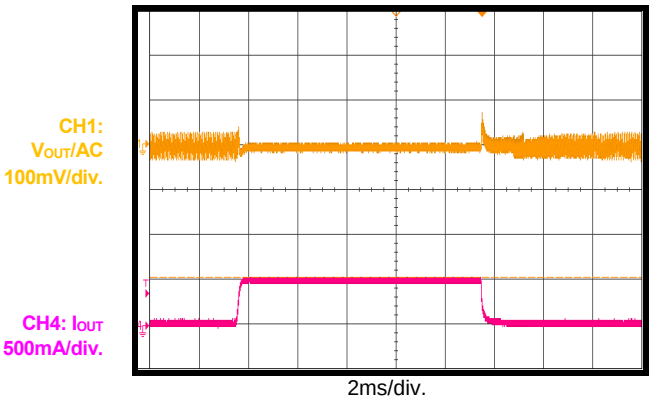
EN Shutdown

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.5A



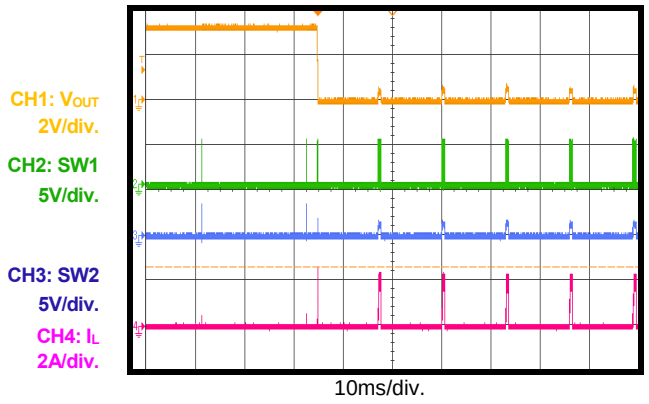
Load Transient

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A-0.5A, 200mA/µs



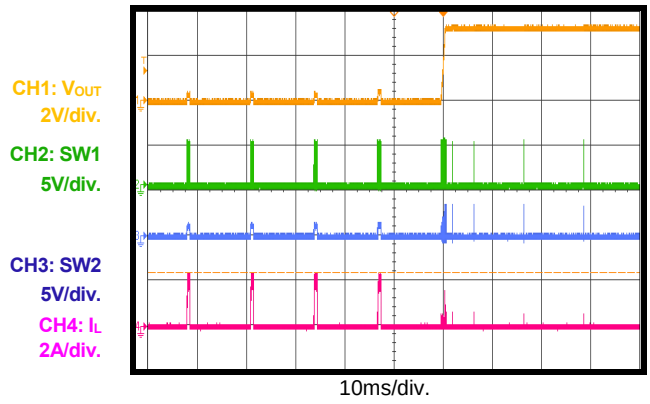
SCP Entry

V_{IN}=5V, V_{OUT}=3.3V, short output to GND.



SCP Recovery

V_{IN}=5V, V_{OUT}=3.3V, short output to GND



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BLOCK DIAGRAM

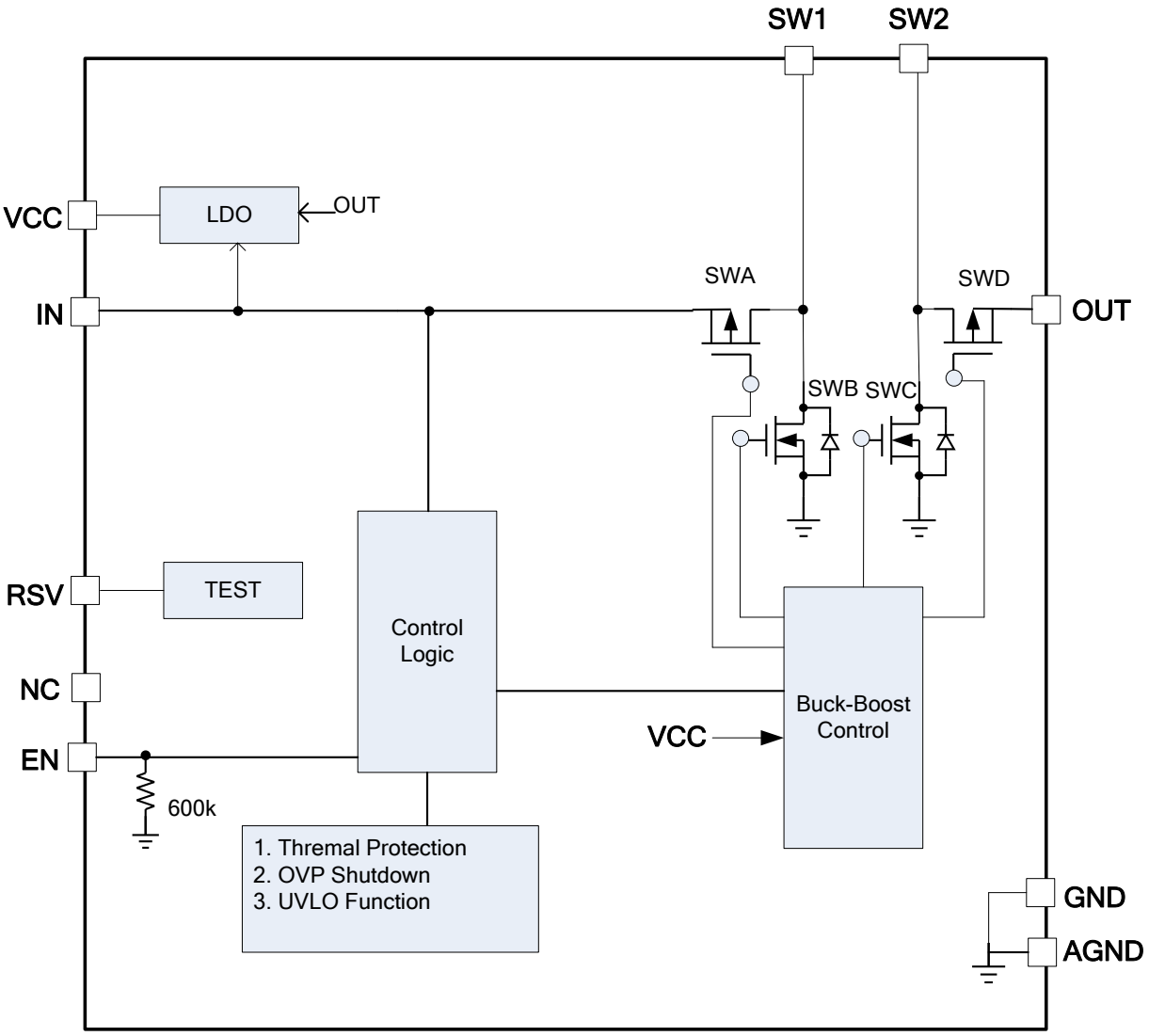

Figure 1: Functional Block Diagram

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OPERATION

The MP28160 is a high efficiency, buck-boost converter that provides regulated output voltage above, equal to, or below the input voltage.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is used to protect the device from operating at an insufficient supply voltage. The MP28160's UVLO circuit monitors the IN voltage. During start-up, IN must rise higher than $V_{IN-UVLO}$ to enable the IC.

EN

EN is the system on/off control input. It's an active low input. EN has an internal weak pull-down resistor. Pull EN low or float to enable the MP28160. Pull EN high to disable the MP28160.

VCC Power Supply

When EN is active, IN charges the VCC. All internal circuits of the MP28160 are supplied by VCC, and VCC only needs to be decoupled with a ceramic capacitor less than 1μF. VCC can be biased by VOUT. After the system starts up, VCC is powered by the higher value of IN or VOUT internally.

Buck-Boost Operation

The output voltage is sensed via an internal resistor divider from the output to ground. The voltage difference between the V_{OUT} feedback voltage and the internal reference is amplified by the error amplifier to generate a control signal (V_{C-Buck}). By comparing V_{C-Buck} with the internal current ramp signal (the sensed SWA's current with slope compensation) through the buck comparator, a pulse-width modulation (PWM) control signal for the buck leg (SWA, SWB) is generated.

Another control signal ($V_{C-Boost}$) is derived from V_{C-Buck} through the level shift. Similarly, $V_{C-Boost}$ is compared with the same ramp signal through the boost comparator and generates a PWM control signal for the boost leg (SWC, SWD). The switch topology for the buck-boost converter is shown in Figure 2.

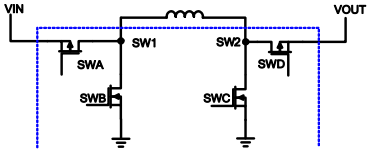

Figure 2: Buck-Boost Switch Topology

Buck Region (VIN > VOUT)

When the input voltage is significantly higher than the output voltage, the converter can deliver energy to the load within SWA's maximum duty cycle by switching SWA and SWB. The converter operates in buck mode. In this condition, SWD remains on and SWC remains off. V_{C-Buck} compares with the current ramp signal normally and generates a PWM output. Therefore, SWA/SWB is pulse-width modulated to produce the required duty cycle and eventually support the output voltage.

Buck-Boost Region (VIN ≈ VOUT)

When VIN is close to VOUT, the converter is unable to provide enough energy to the load due to SWA's maximum duty cycle, so the current ramp signal cannot trigger V_{C-Buck} in the first period, and SWA remains on with 100% duty cycle. If SWB is not turned on in the first period, boost begins working in the secondary period (SWC switches in the secondary period), and an offset voltage is added to the current ramp signal to allow it to reach V_{C-Buck}. SWC turns off when the current ramp signal intersects with $V_{C-Boost}$ in the secondary period, and SWD conducts the inductor current when SWC is off. This is called boost operation.

SWA turns off when the current ramp signal intersects with V_{C-Buck} in the secondary period, and SWB turns on to conduct the inductor current after SWA turns off. This is called buck operation.

If SWB turns on in the secondary period, the boost operation (SWC on) is disabled in the following cycle. If SWA continues to conduct with 100% duty in the secondary cycle, the boost operation is also enabled in the following duty cycle. SWA/SWB and SWC/SWD switch during this condition simultaneously. This is called buck-boost mode.

Boost Region (VIN < VOUT)

When the input voltage is significantly lower than the output voltage, the control voltage (V_{C-Buck}) is always higher than the current ramp signal. The offset voltage is added to the current signal, so SWB cannot turn on in all cycles. The boost operation (SWC on) is enabled in every cycle based on the logic, so only SWC and SWD switch. This is called boost mode. In this condition, SWC/SWD is pulse-width modulated to

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produce the required duty cycle and eventually support the output regulation voltage.

Internal Soft Start (SS)

When EN is active and VIN is above the UVLO rising threshold, the MP28160 buck-boost starts up with a soft-start function. The internal soft-start (SS) signal ramps up and controls the feedback reference voltage.

OCP/SCP

The MP28160 employs peak current limits through switch A current sensing. The current limit is 2.5A typical.

In an overload or short-circuit condition, VOUT drops due to the steady state switching current limit. If VOUT drops below 60% of its normal output, the MP28160 stops switching and recovers after ~12ms with hiccup mode protection. After the switching stops in hiccup protection, the internal soft-start signal is clamped to V_{FB} + 0.3V, where V_{FB} is the divided voltage from the residual VOUT. This smooths the soft start-up when the MP28160 recovers from hiccup protection.

During the soft-start time, the MP28160 blanks during hiccup protection. After the soft-start time is finished, if VOUT is still lower than 60% of the normal voltage, the MP28160 resumes hiccup mode. If VOUT rises above 60% of the normal value, the MP28160 enters normal operation.

OVP

The MP28160 employs output over-voltage protection. A fast comparator will sense the output voltage condition. Once it is triggered, the MP28160 will stop switching, and a 1k internal resistor will be switched on to discharge the output.

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APPLICATION INFORMATION

Component Selection

Selecting the Inductor

As a buck-boost topology circuit, the inductor must support buck application with the maximum input voltage and boost application with the minimum input voltage. Two critical inductance values can be calculated according to the buck and boost mode current ripple. See equation (1) and (2).

$$L_{MIN-BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times F_{REQ} \times \Delta I_L} \quad (1)$$

$$L_{MIN-BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times F_{REQ} \times \Delta I_L} \quad (2)$$

Where:

F_{REQ} is the switching frequency

ΔI_L is the peak-to-peak inductor current ripple. As a rule of thumb, the peak-to-peak ripple can be set at 0.2A to 1A to achieve a better balance between the BOM cost, output ripple, and efficiency. The minimum inductor value for the application is the higher value between Equation 1 and Equation 2.

In addition to the inductance value, the inductor must support peak current based on equation (3) and equation (4) to avoid saturation.

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times F_{REQ} \times L} \quad (3)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times F_{REQ} \times L} \quad (4)$$

Where η is the estimated efficiency of the MP28160.

Choose a proper inductor to make sure the inductor current won't trigger the peak current and valley current limit.

Input and Output Capacitor Selection

Use ceramic capacitors with low ESR as input and output capacitors in order to filter any disturbance present in the input line and achieve stable operation.

Minimum values of 10μF for the input capacitor and 2×22μF for the output capacitors are needed to achieve optimum performance.

The input and output capacitors must be placed as close to the device as possible.

PCB Board Layout (8)

Efficient PCB layout is critical for standard operation and thermal dissipation. Refer to Figure 3 and the PCB layout guidelines below to ensure an effective layout design:

1) Place the VIN capacitor and VOUT capacitor as close to VIN and OUT as possible.

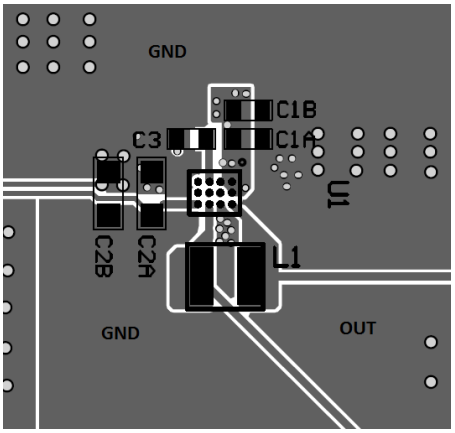
2) Use a large ground plane directly connected to GND. Add lots of GND vias to connect Cout's GND node and VIN capacitor's GND.

3) Connect AGND to the VCC capacitor's GND node by a Kelvin sense trace.

4) Place the VCC decoupling capacitor as close as possible to VCC.

Notes:

(8) The recommended layout is based on the typical application circuit on the next page (see Figure 4).



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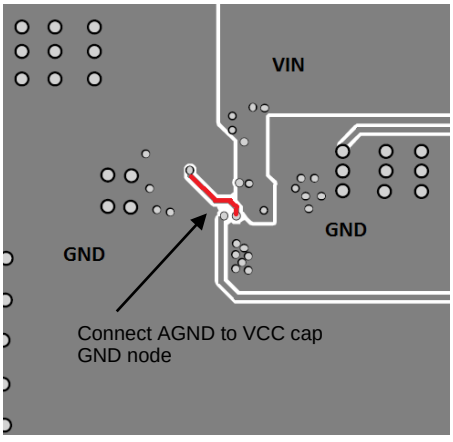

Bottom layer

Figure 3: PC Board Layout

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TYPICAL APPLICATION CIRCUITS

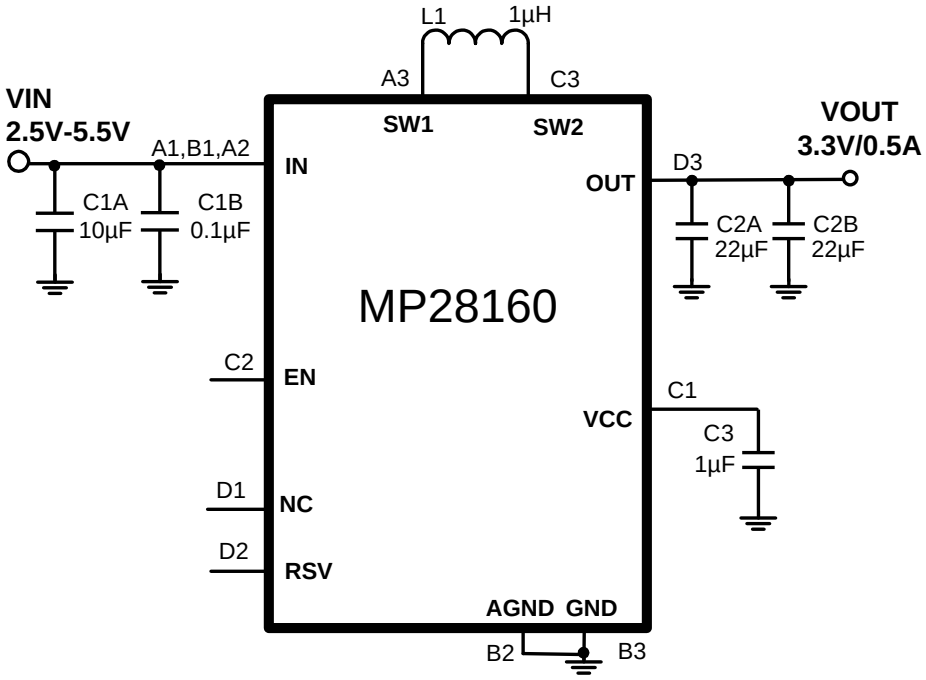

Figure 4: Typical application circuit with fixed 3.3V output voltage

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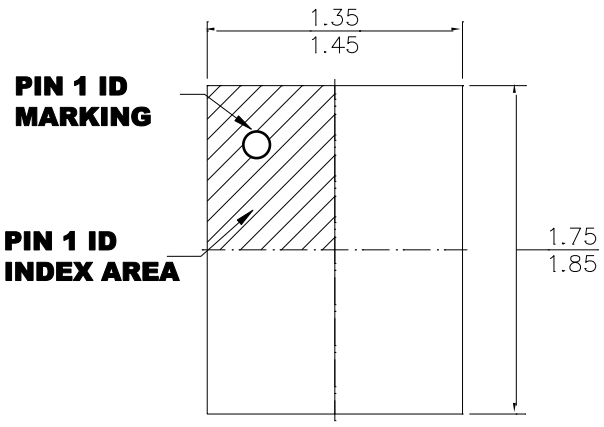
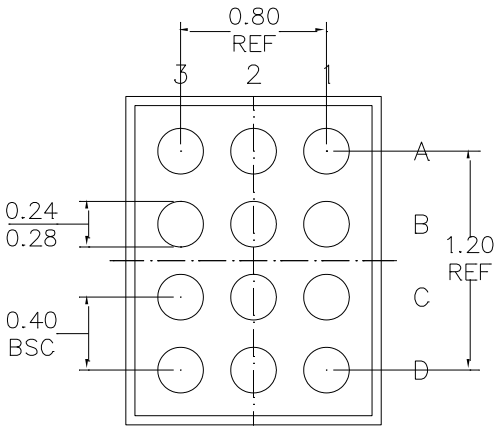
PACKAGE INFORMATION

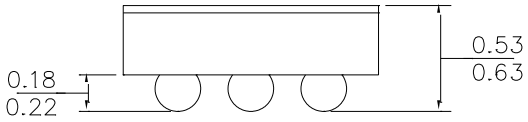
CSP-12 (1.4mmx1.8mm)



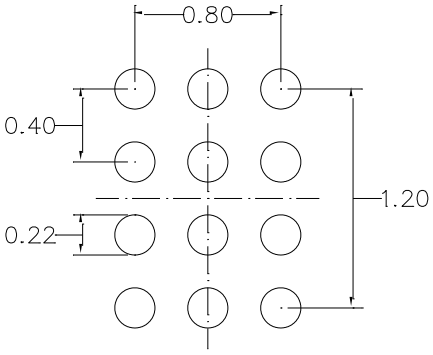
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

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