MP2661

4.65V System, 500mA,I²C-Controlled Battery Charger with Power Path Management for Single-Cell Li-Ion Battery

The Future of Analog IC Technology

DESCRIPTION

The MP2661 is a highly integrated, single-cell, Li-Ion/Li-Polymer battery charger with system power path management for space-limited, portable applications. The MP2661 uses input power from either an AC adapter or a USB port to supply the system load and charge the battery independently. The charger features trickle charge, constant current (CC) and constant voltage (CV) regulation, charge termination, and charge status.

The power path management function ensures continuous power to the system by automatically selecting the input, the battery, or both to power the system. This power stage features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2661 provides system short-circuit protection (SCP) by limiting the current from the input to the system and the battery to the system. This feature is especially critical to prevent the Li-Ion battery from being damaged by excessively high currents. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below the programmable battery UVLO threshold, which prevents the Li-Ion battery from being over-discharged. An integrated I²C control interface allows the MP2661 to program the charging parameters, such as input current limit, input voltage regulation limit, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2661 is available in a 9-pin 1.55mmx1.55mm WCSP package.

FEATURES

- Fully Autonomous Charger for Single-Cell Li-Ion/Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I²C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- PCB Over-Temperature Protection (PCB_OTP)
- System Reset Function
- Built-In Battery Disconnection Function
- Thermal Limiting Regulation On-Chip
- Available in a WCSP-9 (1.55mmx1.55mm) Package

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smart Watches

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

TYPICAL APPLICATION

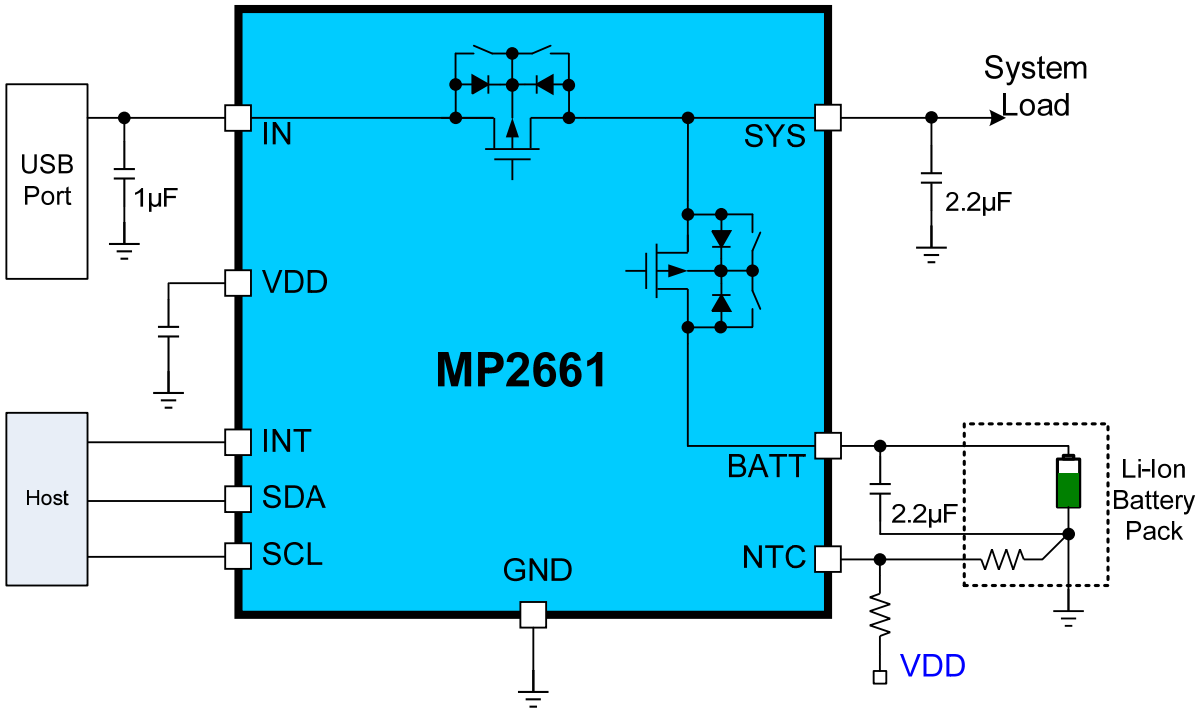


Table 1: Operation Mode Table

Items	I²C Control			INT Pin	
	HZ=1	CEB=1	FET_DIS=1*	H to L for 16s	H to L for 4s
LDO FET	Off	x	X	x	x
Battery FET (charging)	x	Off	Off	Off for 4s, then on	On
Battery FET (discharging)	x	x	Off	Off for 4s, then on	On

x = no effect

* -- FET_DIS goes back to 0 battery FET is off.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number**	Package	Top Marking
MP2661GC-xxxx***	WLCSP-9(1.55mmx1.55mm)	*See Below*
EVKT-2661	Evaluation Kit	

** For Tape & Reel, add suffix –Z (e.g. MP2661GC-xxxx–Z)
***"xxxx"is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain a "xxxx" value.

TOP MARKING

EZY
LLL

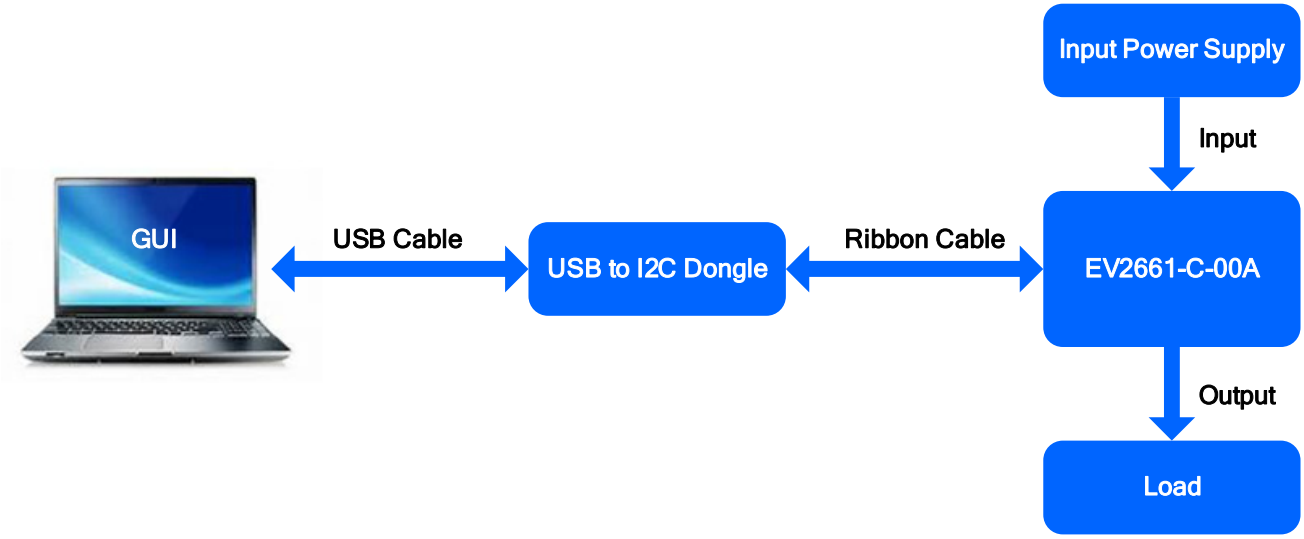
EZ: Product code of MP2661GC
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-2661

EVKT-2661 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EV2661-C-00A	MP2661 Evaluation Board	1
2	EVKT-USBI2C-02-BAG	Include one USB to I²C dongle, one USB cable, one ribbon cable,	1
3	Tdrive-2661	USB Flash drive that stores the GUI installation file and supplemental documents.	1

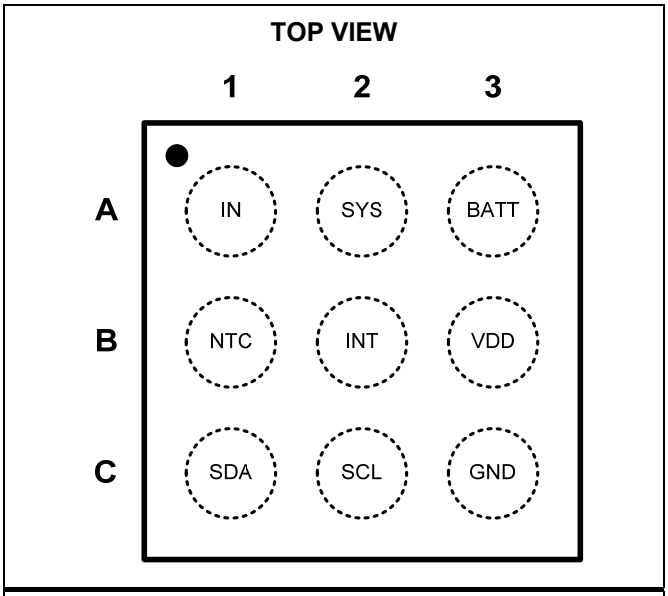
Order direct from MonolithicPower.com or our distributors.



EVKT-2661 Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

PACKAGE REFERENCE



WCSP-9 (1.55mmx1.55mm)

PIN FUNCTIONS

Package Pin #	Name	I/O	Description
A1	IN	Power	**Input power.** Place a ceramic capacitor (≥1μF) from IN to GND as close to the IC as possible.
A2	SYS	Power	**System power supply.** Place a ceramic capacitor (≥2.2μF) from SYS to GND as close to the IC as possible.
A3	BATT	Power	**Battery.** Place a ceramic capacitor (≥2.2μF) from BATT to GND as close to the IC as possible.
B1	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VDD to NTC to GND. The charge is suspended when NTC is out of range.
B2	INT	O	**Open drain interrupt output.** INT can send the charging status and fault interruption to the host. INT is also used to disconnect the system from the battery. Pull INT from high to low for >16s.The battery MOSFET is off and turns on automatically after >4s, regardless of the INT state. The external pull up resistor at INT should be **not smaller than 300kΩ**.
B3	VDD	I	**Internal control power supply.** Connect a ceramic capacitor(0.1μF)from VDD to GND. No external load is allowed.
C1	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
C2	SCL	I/O	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
C3	GND	Power	**Ground.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +13V
All other pins to GND ..... -0.3V to +6.0V
Continuous power dissipation(T_A=+25°C)(2)
..... 0.88W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (VIN) ..... 4.35V to 5.5V (USB Input)
I_{IN} ..... Up to 455mA
I_{SYS} ..... Up to 3A(5)
I_{CHG} ..... Up to 455mA
V_{BATT} ..... Up to 4.545V
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
WLCSP-9 (1.55mmx1.55m)	114 ..	12 ...	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Guaranteed by design

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT}=3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input voltage range	V_{IN}				13	V
Input operation voltage	V_{IN}		4.35	5	5.5	V
BATT input voltage(5)	V_{BATT}				4.5	V
Input over-voltage protection (OVP) threshold	V_{IN_OVP}	Input rising threshold	5.85	6	6.15	V
Input OVP hysteresis				350		mV
Input under-voltage threshold	V_{UV_IN}	Input rising threshold	3.8	3.9	4.0	V
Input under-voltage threshold hysteresis				170		mV
Input vs. battery threshold	V_{IN_BATT}	Input rising vs. battery	100	130	160	mV
Input vs. battery threshold hysteresis				85		mV
BATT under-voltage threshold	V_{UV_BATT}	BATT voltage falling, programmable, Reg01[2:0]=100 –2.8V	2.6	2.8	3.0	V
Battery UVLO Range		Programmable using I²C	2.4		3.1	V
BATT under-voltage threshold hysteresis				210		mV
Battery over-voltage protection	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		130		mV
		Falling, higher than V_{BATT_REG}		70		
Power Path Management						
Regulated system output voltage	V_{SYS_REG}	V_{IN} =5.5V, I_{SYS}=10mA, I_{CHG}=0A	4.55	4.65	4.75	V
Input current limit	I_{IN_LMT}	Reg00[2:0]=000 –85mA	65	75	85	mA
		Reg00[2:0]=001 –130mA	102	116	130	
		Reg00[2:0]=100 –265mA	230	247	265	
		Reg00[2:0]=111 –455mA	400	428	455	
Input voltage regulation threshold	V_{IN_REG}	I²C programmable range	3.88		5.08	V
		I²C setting V_{IN_REG} =4.20V	4.10	4.20	4.30	
SYS output voltage	V_{SYS}	Charging mode, V_{IN}=5.5V, V_{BATT}=3.7V	4.55	4.65	4.75	V
		Supplement mode, V_{BATT}=3.7V,I_{BATT}=100mA	3.6			
		V_{IN}<V_{UV_IN} and V_{BATT}<V_{UV_BATT}		0		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT}=3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN to SYS switch on resistance	R_{ON_SYS}	V_{IN}=5V, I_{SYS}=100mA		300	400	mΩ
Supply current at input	I_{IN}	V_{IN}=5.5V, CE=L, enable, I_{CHG} = 0A, I_{SYS} = 0A		600		μA
		V_{IN}=5.5V,CE=H, charge disabled		480		
Supply current at BATT input	I_{BATT}	V_{IN}=5V, CE=L, I_{SYS}=0A, V_{BATT}=4.3V		32		μA
		V_{IN}=0V, CE=H, I_{SYS} = 0A, V_{BATT}=4.35V, disable PCB_OTP function, do not include the current from external NTC resistor		11	13	
		V_{IN}=0V, CE=H, I_{SYS} = 0A, V_{BATT}=4.35V, enable PCB_OTP function, do not include the current from external NTC resistor		20	24	
		V_{BATT}=4.5V, V_{IN}=V_{SYS}=GND, FET_DIS=1, disconnect mode		4	5.5	
BATT input to SYS switch on resistance	R_{ON_BATT}	V_{IN}< 2V, V_{BATT}=3.5V, I_{SYS}=100mA		100	150	mΩ
BATT to SYS current limit	I_{BATT_MAX}	Program Range	400		3200(5)	mA
BATT to SYS switch leakage		V_{BATT}=4.5V, V_{IN}=V_{SYS}=GND, disconnect mode			1	μA
SYS reverse to BATT switch leakage		V_{SYS}=6V, V_{IN}=4.5V, V_{BATT}=GND, CE=H			1	μA
Battery discharge function controlled by INT (5)	t_{INT}	INT pull-low lasting time to turn off the battery discharge function		16		s
		Battery MOSFET lasts for the off time duration before auto-on		4		
Battery Charger						
Battery voltage regulation range	V_{BATT_REG}	Programmable using I²C	3.600		4.545	V
Battery voltage regulation (V_{BATT_REG}=4.2V)	V_{BATT}	T = +25°C, I_{BATT} = 15mA	4.179	4.20	4.221	V
Battery charge full voltage(I²C]	V_{BATT_REG}	V_{BATT_REG} = 4.2V, Reg04[7:2] = 101000	4.179	4.20	4.221	V
		V_{BATT_REG} = 4.35V, Reg04[7:2] = 110010	4.328	4.35	4.372	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT}=3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Constant current regulation for charging	I_{CHG}	V_{IN} = 5V, V_{BATT} = 3.8V, programmable range	8		535(5)	mA
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CHG_SETTING}$ = 93mA	88	93	98	
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CHG_SETTING}$ = 246mA	232	248	263	
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CHG_SETTING}$ = 399mA	376	401	426	
Charging current thermal foldback threshold(5)		Junction Temperature Regulation Reg06[1:0]=11–120°C		120		°C
Trickle current	I_{TC}	Program range	6		27	mA
		$I_{TC_setting}$=6mA, Reg03h[1:0]=00	2.5	4.7		
		$I_{TC_setting}$=20mA, Reg03h[1:0]=10	14	18	22	
End of charge (EOC) current threshold	I_{BF}	$I_{CHG_SETTING}$≤263mA, (Reg02 bit[4] = 0), $I_{TC_SETTING}$= 6mA	5	7	9	mA
		$I_{CHG_SETTING}$≤263mA, (Reg02 bit[4] = 0), $I_{TC_SETTING}$=13mA	10	13.5	17	
		$I_{CHG_SETTING}$≤263mA, (Reg02 bit[4] = 0), $I_{TC_SETTING}$=20mA	16	20	24	
		$I_{CHG_SETTING}$≤263mA, (Reg02 bit[4] = 0), $I_{TC_SETTING}$=27mA	22	27	32	
		$I_{CHG_SETTING}$≥280mA, (Reg02 bit[4] = 1), $I_{TC_SETTING}$= 6mA	10	13.5	17	
		$I_{CHG_SETTING}$≥280mA, (Reg02 bit[4] = 1), $I_{TC_SETTING}$=13mA	22	27	32	
		$I_{CHG_SETTING}$≥280mA, (Reg02 bit[4] = 1), $I_{TC_SETTING}$=20mA	34	42	49	
		$I_{CHG_SETTING}$≥280mA, (Reg02 bit[4] = 1), $I_{TC_SETTING}$=27mA	46	55	64	
End of charge current threshold hysteresis	I_{BF_HYS}	$I_{CHG_SETTING}$≤263mA, (Reg02 bit[4] = 0), $I_{TC_SETTING}$= 20mA	7.5	11	15	mA
		$I_{CHG_SETTING}$ ⩾ 280mA, (Reg02 bit[4] = 0), $I_{TC_SETTING}$ = 20mA	19	24	29	
Trickle charge threshold voltage	V_{BATT_LOW}	V_{BATT}rising, set V_{BATT_LOW}=3.0V	2.8	3.0	3.1	V
Trickle voltage hysteresis				90		mV
Recharge threshold below V_{BATT_REG}	V_{RECHG}	Reg04[0] = 0	120	160	200	mV
		Reg04[0] = 1	260	300	350	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown rising threshold(5)				150		°C
Thermal shutdown hysteresis(5)				20		°C
NTC output current	I_{NTC}	CE = L, NTC = 3V	-100	0	100	nA
NTC cold temp rising threshold	V_{COLD}	As a percentage of V_{DD}	63	65	67	%
NTC cold temp rising threshold hysteresis				30		mV
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{DD}	31	33	35	%
NTC hot temp falling threshold hysteresis				70		mV
NTC hot temp falling threshold for PCB_OTP	V_{HOT_PCB}	As a percentage of V_{DD}	30	32	34	%
NTC hot temp falling threshold hysteresis for PCB_OTP				85		mV
Logic I/O Pin Characteristics						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
I²C Interface(SDA, SCL)						
Input high threshold level		V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.4	V
I²C clock frequency	F_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Digital clock2	F_{DIG2}			32		kHz
Watchdog timer	t_{WDT}	Programmable (Reg05h [5:4] = 11)		160		s

NOTE:

5) Guaranteed by design.

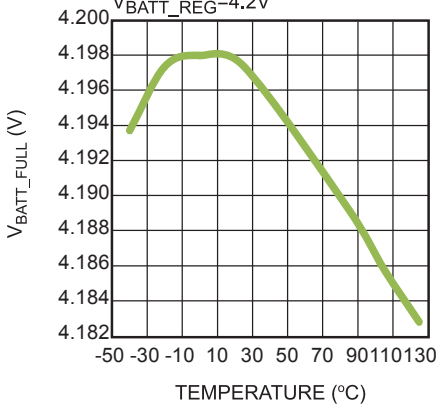
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LMT}=455mA, I_{CHG}=246mA, V_{IN_REG}=4.76V, unless otherwise noted.

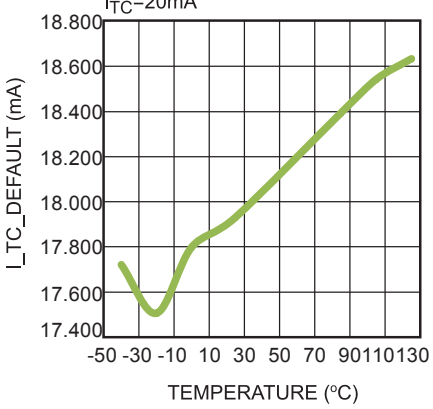
VBATT Full Voltage vs. Temperature

V_{BATT_REG}=4.2V



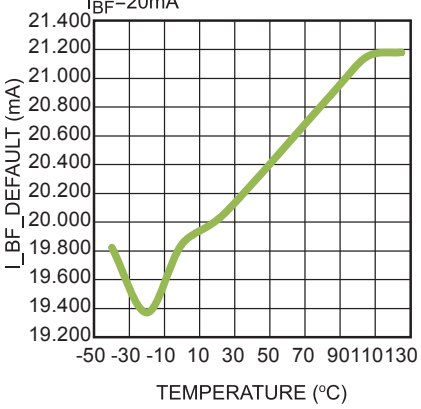
Trickle Charge Current vs. Temperature

I_{TC}=20mA



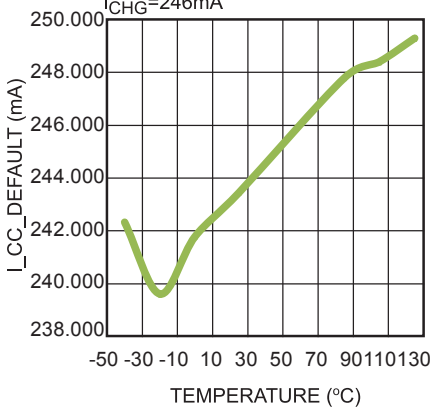
Battery Full Termination Current vs. Temperature

I_{BF}=20mA



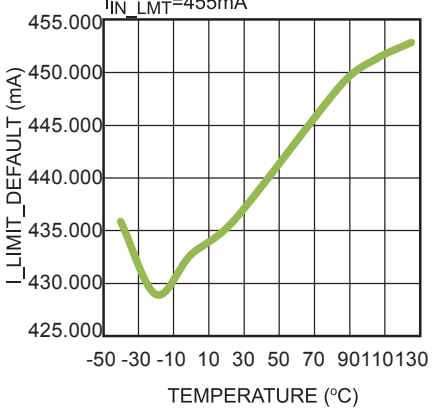
Charge Current vs. Temperature

I_{CHG}=246mA

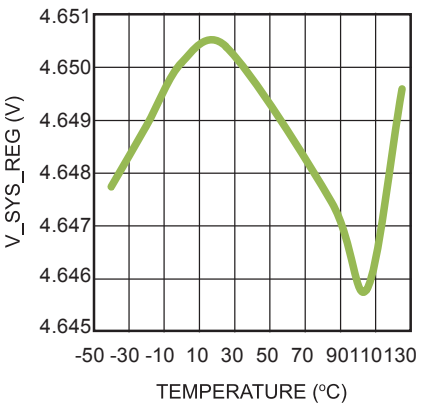


Input Current Limit vs. Temperature

I_{IN_LMT}=455mA

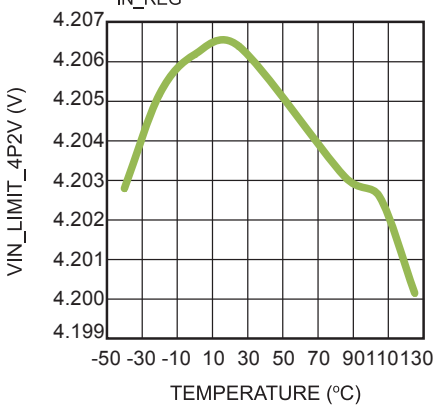


System Regulation Voltage vs. Temperature



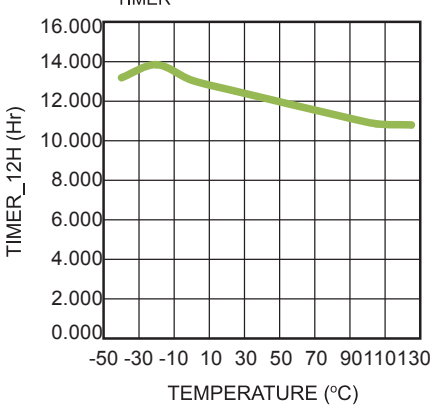
Input Voltage Regulation vs. Temperature

V_{IN_REG}=4.2V

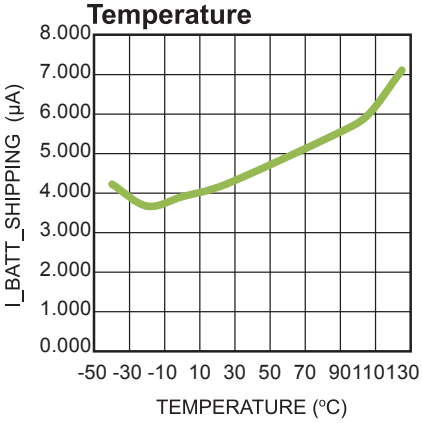


Timer Period vs. Temperature

T_{TIMER}=12 Hours



Battery Leakage Current Under Shipping vs. Temperature

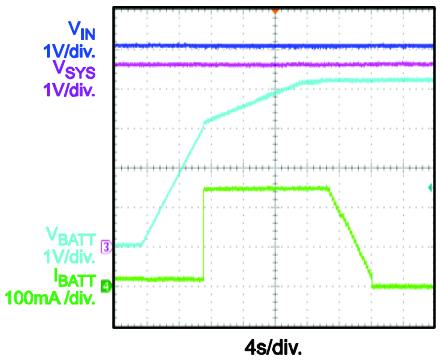


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

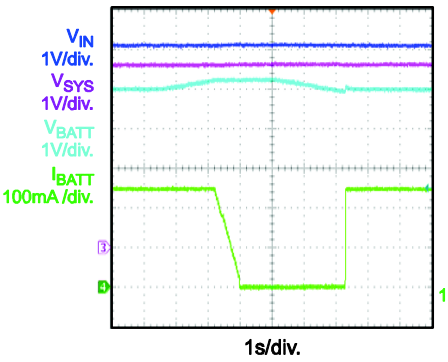
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LMT}=455mA, I_{CHG}=246mA, V_{IN_REG}=4.76V, unless otherwise noted.

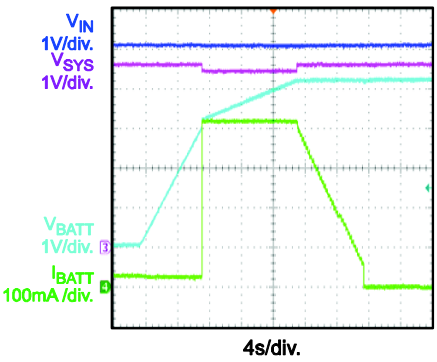
Battery Charge Curve
I_{SYS}=0A



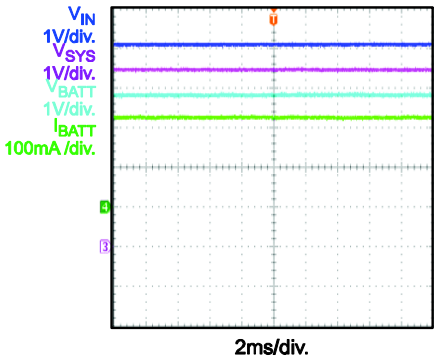
Auto-Recharge
I_{SYS}=0A



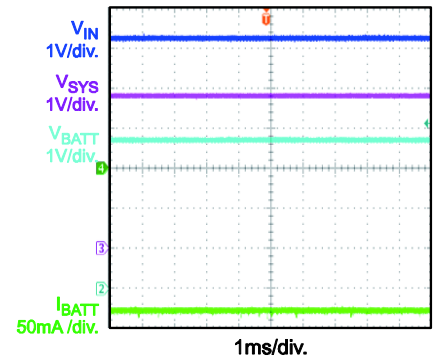
Battery Charge Curve
I_{CHG}=399mA



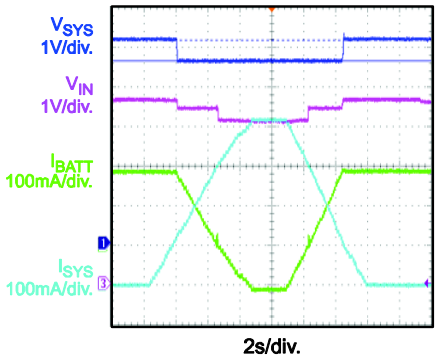
CC Charge Steady State
V_{BATT}=3.7V, I_{SYS}=200mA



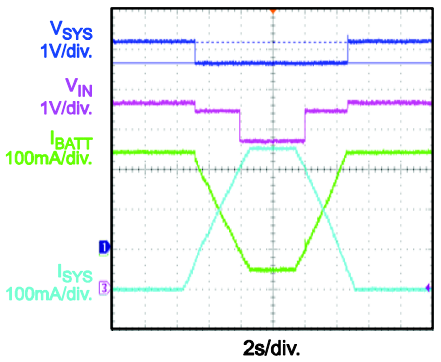
Supplement Mode Steady State
V_{BATT}=3.7V, I_{SYS}=600mA



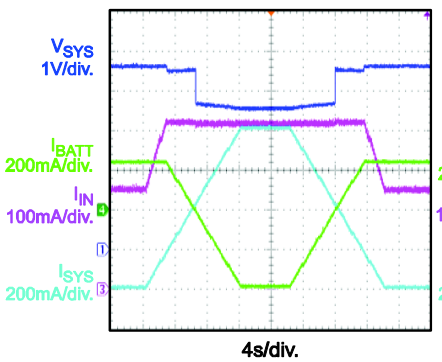
Input Voltage Regulation based PPM
V_{IN}=5V/150mA, V_{BATT}=4.2V, V_{IN_REG}=4.84V



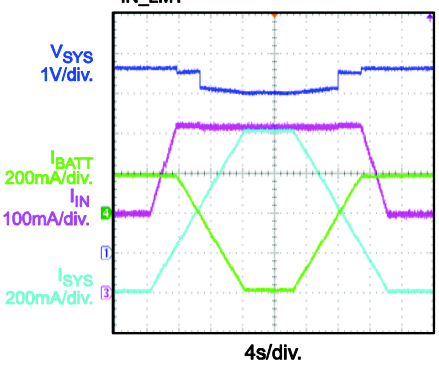
Input Voltage Regulation based PPM
V_{IN}=5V/300mA, V_{BATT}=3.7V



Input Current Limit based PPM
V_{BATT}=3.7V



Input Current Limit based PPM
V_{BATT}=4.2V, I_{BATT}=100mA, I_{IN_LMT}=200mA

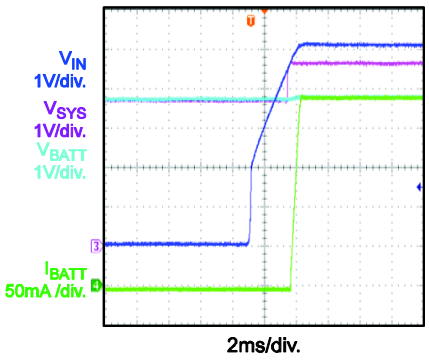


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

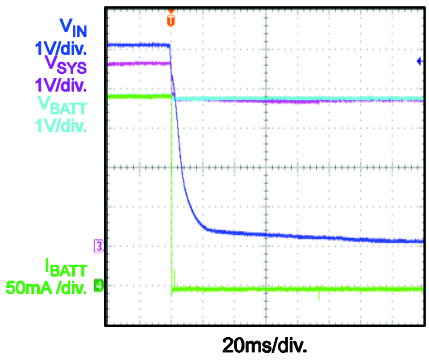
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LMT}=455mA, I_{CHG}=246mA, V_{IN_REG}=4.76V, unless otherwise noted.

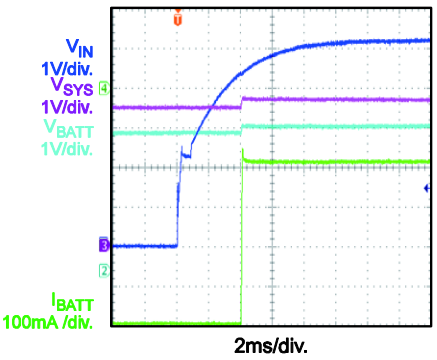
Power On
V_{BATT}=3.7V, I_{SYS}=0A



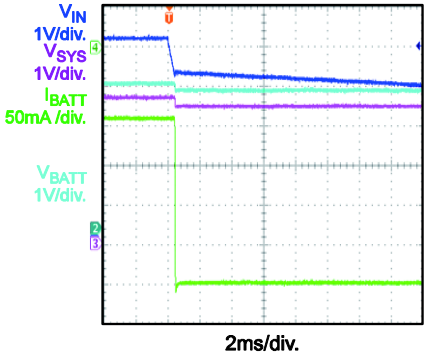
Power Off
V_{BATT}=3.7V, I_{SYS}=0A



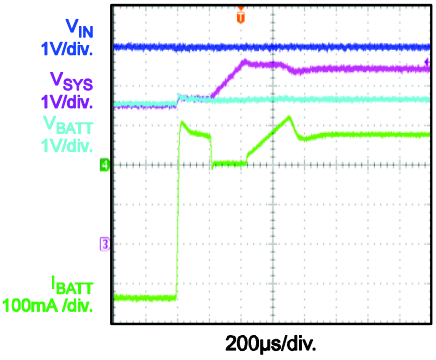
Power On @ Supplement Mode
V_{BATT}=3.7V, I_{SYS}=600mA



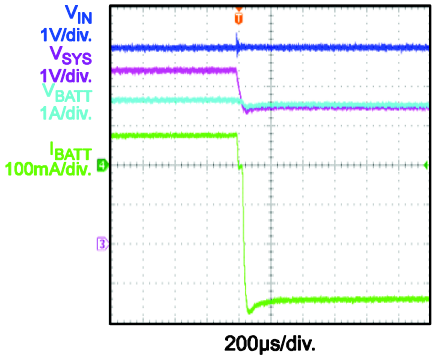
Power Off @ Supplement Mode
V_{BATT}=3.7V, I_{SYS}=600mA



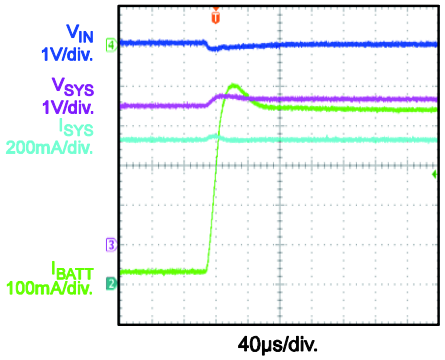
EN On @ Input Current Limit Based PPM
V_{BATT}=3.7V, I_{SYS}=350mA



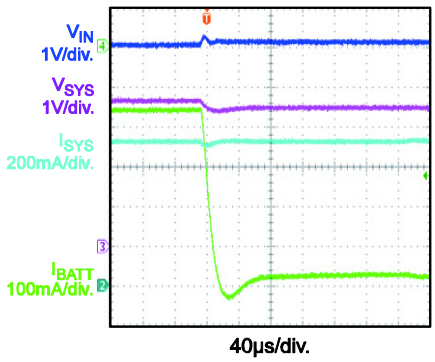
EN Off @ Input Current Limit Based PPM
V_{BATT}=3.7V, I_{SYS}=350mA



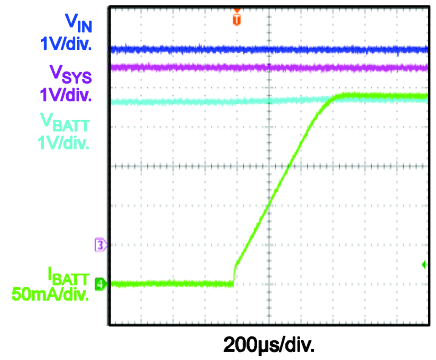
EN On @ Supplement Mode
V_{BATT}=3.7V, I_{SYS}=600mA



EN Off @ Supplement Mode
V_{BATT}=3.7V, I_{SYS}=600mA



Charge On
V_{BATT}=3.7V, I_{SYS}=0A

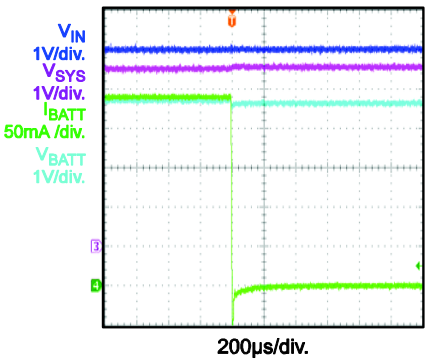


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

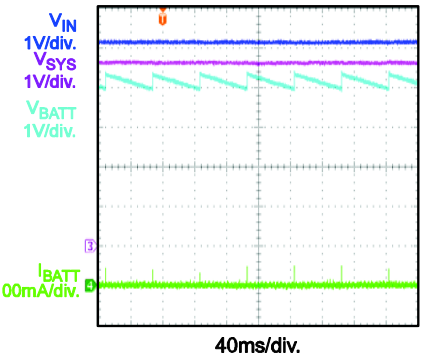
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LMT}=455mA, I_{CHG}=246mA, V_{IN_REG}=4.76V, unless otherwise noted.

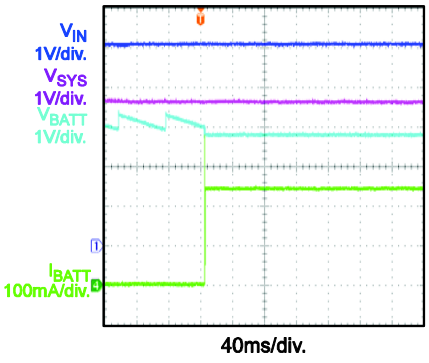
Charge Off
V_{BATT}=3.7V, I_{SYS}=0A



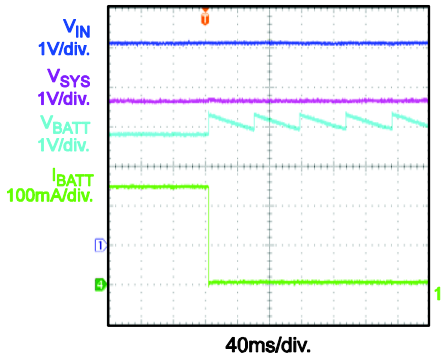
BATT Float Operation
I_{SYS}=0A



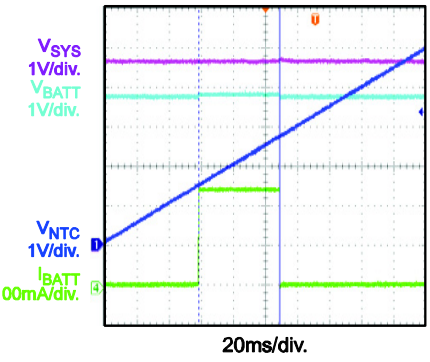
BATT Insertion
V_{BATT}=3.7V, I_{SYS}=0A



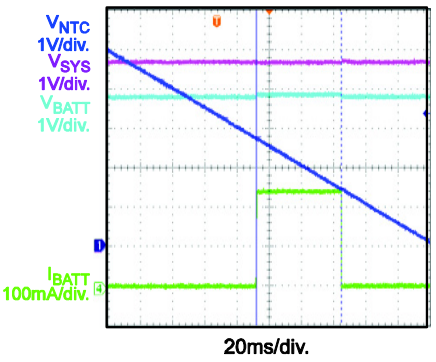
BATT Removal
V_{BATT}=3.7V, I_{SYS}=0A



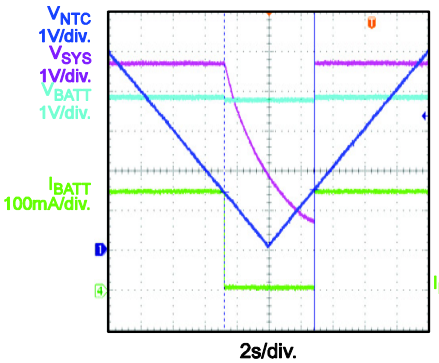
NTC On/Off
V_{BATT}=3.7V, I_{SYS}=0A



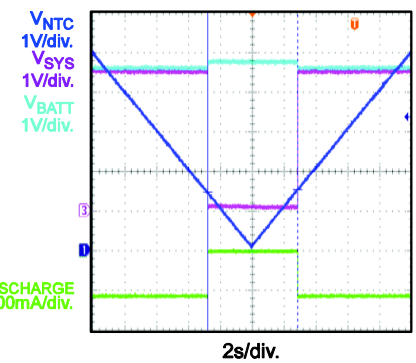
NTC On/Off
V_{BATT}=3.7V, I_{SYS}=0A



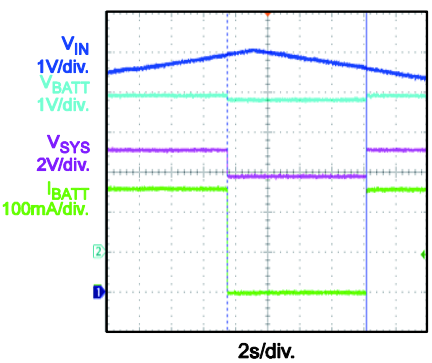
PCB OTP @ Charge Mode
V_{BATT}=3.7V, I_{SYS}=0A



PCB OTP @ Discharge Mode
V_{IN}=0V, V_{BATT}=3.7V, I_{SYS}=1A



V_{IN} OVP Operation
V_{BATT}=3.7V, I_{SYS}=0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

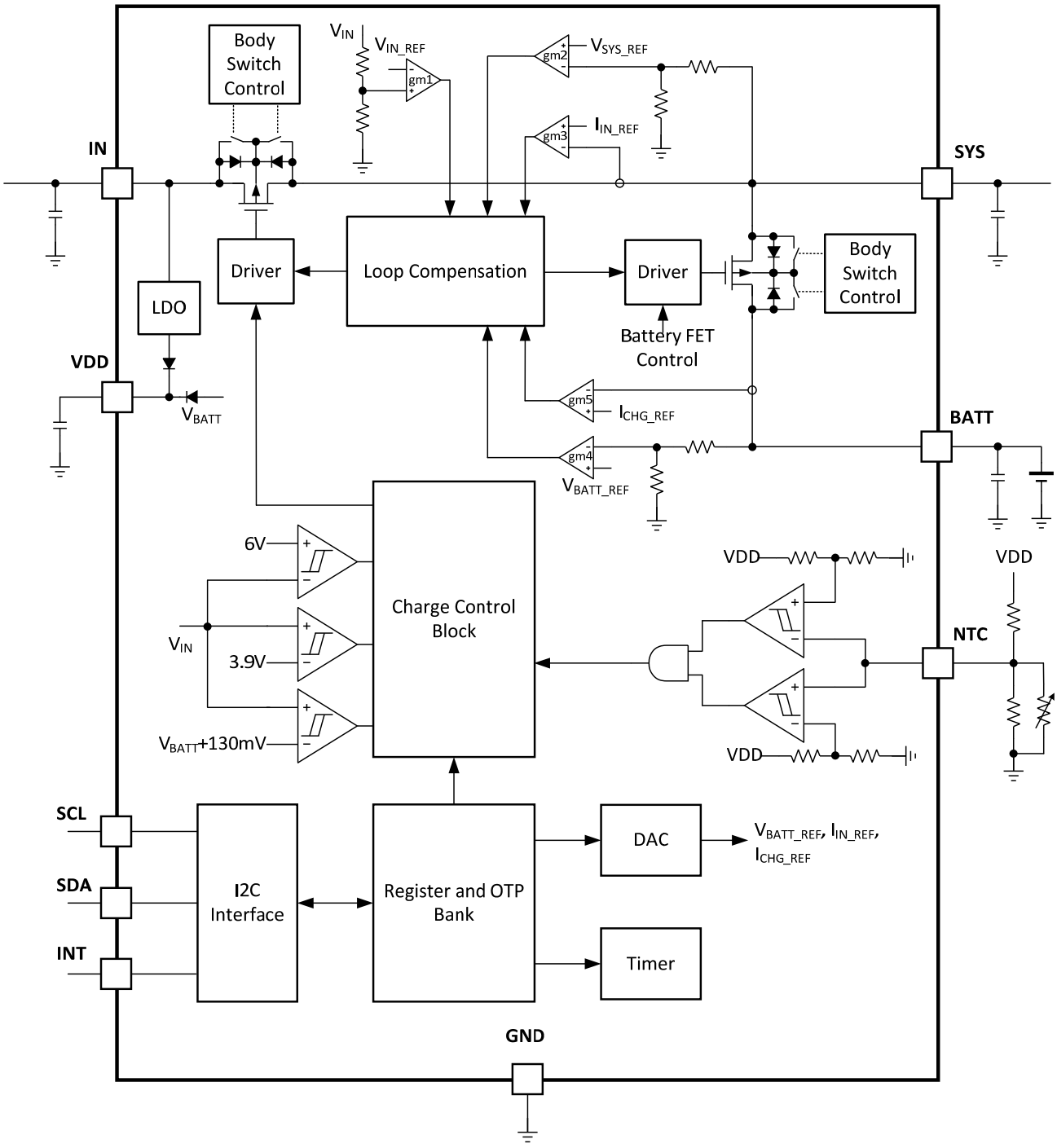


Figure 1: Function Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

OPERATION

Introduction

The MP2661 is an I²C-controlled, single-cell, Li-Ion or Li-Polymer battery charger with complete power path management. The full charge function features trickle charge (TC), constant current (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. If there is conflict in meeting both the system load and battery charging current, the IC reduces the charging current automatically or uses the battery as a supplemental power to satisfy the system load.

The IC integrates a 300mΩ LDO MOSFET between IN and SYS, and a 100mΩ battery MOSFET between SYS and BATT.

In charging mode, the on-chip 100mΩ battery MOSFET works as a full-featured linear charger with trickle charging, constant current and constant voltage charging, charge termination, auto-recharging, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I²C interface. The IC limits the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the 100mΩ battery MOSFET is fully turned on to connect the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 100mΩ battery MOSFET is also fully turned on, allowing the battery to power up the system.

When the system load is satisfied, the remaining current is used to charge the smart power path management battery. The IC reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 2 shows the power path management structure of theMP2661.

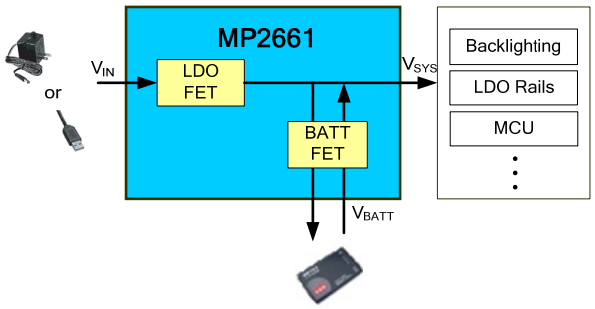


Figure 2: Power Path Management Structure

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN or BATT. When IN or BATT rises above the respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and the battery MOSFET driver are active. The I²C interface is ready for communication and all registers are reset to the default value. The host can access all registers.

Input OVP and UVLO

The MP2661 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the input voltage exits the normal input voltage range, the Q1 MOSFET is turned off immediately.

When the input voltage is identified as a good source, a 200μs immunity timer is active. If the input power is still sufficient until the 200μs timer expires, the system starts up. Otherwise, Q1 remains off.

Figure 3 depicts the operation profile.

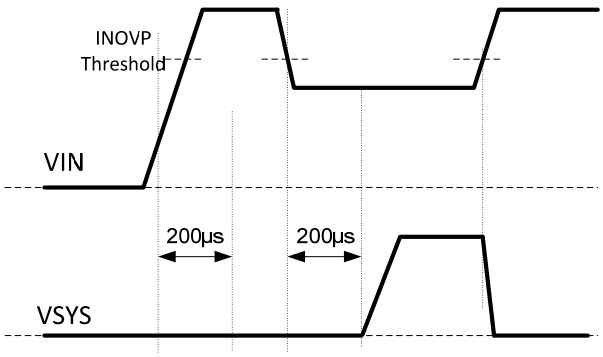


Figure 3: Input Power Detection Operation Profile

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

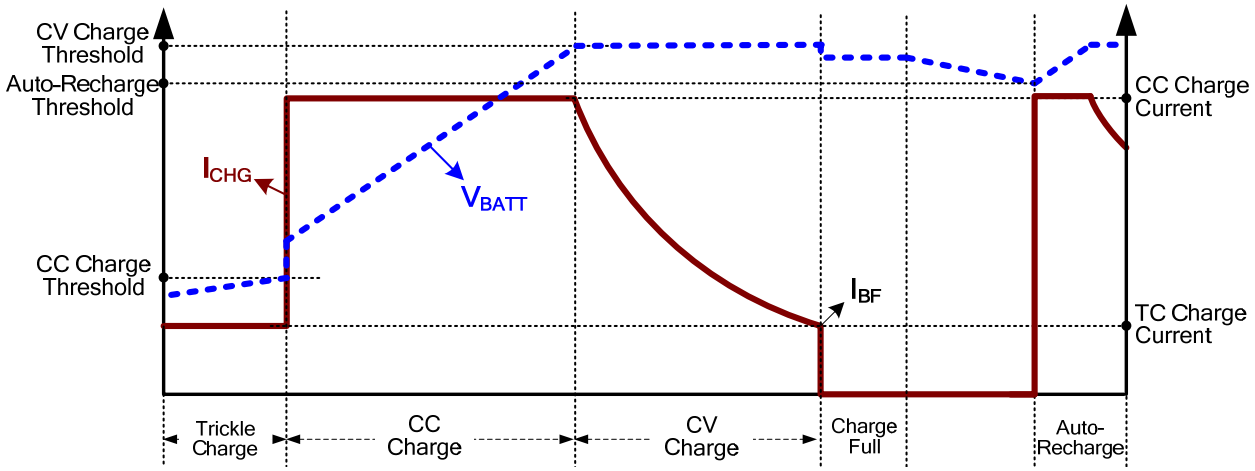


Figure 4: Battery Charge Profile

Power Path Management

The IC employs a direct power path structure with the battery MOSFET decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missed battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO MOSFET.

As shown in Figure 1, the direct power structure is composed of a frond-end LDO MOSFET between IN and SYS and a battery FET between SYS and BATT.

The input LDO (using an LDO MOSFET) provides power to the system, which drives the system load directly and charges the battery through the battery FET.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO MOSFET is fully on with the input current limit.

Battery Charge Profile

The IC provides three main charging phases: trickle charge, constant current charge, and constant voltage charge (see Figure 4).

1. *Phase 1 (trickle current charge):* The IC is able to safely trickle charge the deeply depleted battery until the battery voltage reaches the trickle charge to the fast charge threshold (V_{BATT_LOW}). The trickle charge current is programmable via Reg03 bit [1:0]. If V_{BATT_LOW} is not reached before the pre-charge timer (1hr) expires, the charge cycle is ceased, and a corresponding timeout fault signal is asserted.
2. *Phase 2 (constant current charge):* When the battery voltage exceeds V_{BATT_LOW}, the IC enters a constant-current charge (fast charge) phase. The fast charge current can be programmable via Reg02 bit [4:0].
3. *Phase 3 (constant voltage charge):* When the battery voltage rises to the pre-programmable charge full voltage (V_{BATT_REG}) set via Reg04 bit [7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

Assuming the termination function (EN_BF)is set via Reg05[6] = 1, the charge cycle is considered complete when the following conditions are valid:

- The charge current(I_{BATT}) reaches the end of charge (EOC) current threshold(I_{BF}), and the 2.5ms delay timer is initiated.
- During the 2.5ms delay period, I_{BATT} is always smaller than $I_{BF}+I_{BF_HYSTERESIS}$.

The charge status is marked as complete once the 2.5ms delay timer expires.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

The charge current is terminated at the same time if TERM_TMR is set via Reg05[0] = 0; otherwise, the charge current keeps tapering off.

If EN_BF = 0, the termination function is disabled, the above actions will not occur. During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. If the input current or the input voltage reach their limits during the CV charge, the charge full termination is not influenced when the charge current is not so close to the EOC current specification.

A new charge cycle starts when the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by the I²C
- Auto-recharge kicks in

Under the following conditions:

- No thermistor fault at NTC
- No safety timer fault
- No battery over-voltage
- BATFET is not forced to turn off

Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold, and V_{IN} is still in the operation range, the IC begins another new charging cycle automatically without the requirement of restarting a charging cycle manually.

The auto-recharge function is valid only when EN_BF =1 and TERM_TMR=0.

Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 130mV higher than V_{BATT_REG}. When the battery over-voltage event occurs, the IC suspends the charging immediately and asserts a fault.

Input Current and Input Voltage Based Power Management

To meet the input source (usually USB) maximum current limit specification, the IC uses input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the I²C to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, back-up input voltage-based power management also works to prevent the input source from being overloaded. If either the input current limit or the input voltage limit is reached, the Q1 MOSFET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to the minimum value of 4.56V or V_{IN}-160mV, the charge current is reduced to prevent the system voltage from dropping further.

Voltage-based DPM regulates the input voltage to V_{IN_REG} when the load is over the input power capacity. V_{IN_REG} set via the I²C should be at least 400mV higher than V_{BATT_REG} to ensure the stable operation of the regulator.

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero, and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the IC enters battery supplement mode. When the system voltage is 30mV below the battery voltage, the ideal diode mode is enabled. The battery MOSFET is regulated to maintain V_{BATT}-V_{SYS} at 22.5mV. If the supplement current I_{DSG}*R_{ON_BATT} is higher than 22.5mV, the battery MOSFET is fully turned on to keep the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BATT}+20mV, ideal diode mode is disabled.

Figure 5 shows the dynamic power management and battery supplement mode operation profile.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

When V_{IN} is not available, the IC operates in discharge mode, and the battery MOSFET is always fully on to reduce loss.

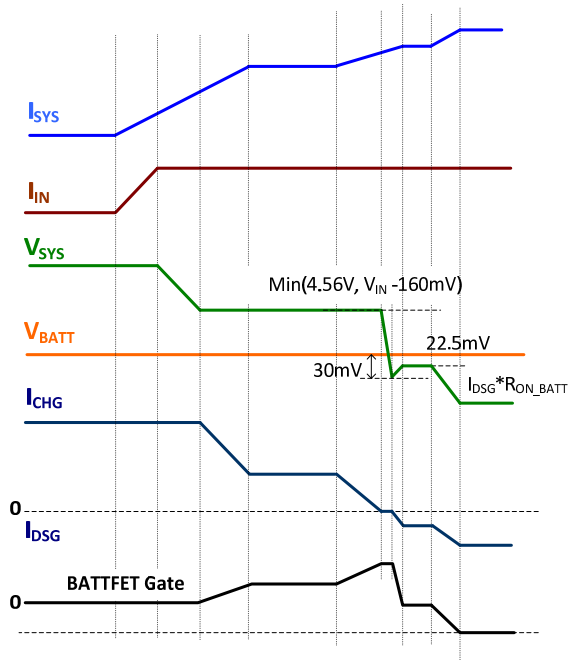


Figure 5: Dynamic Power Management and Battery Supplement Operation Profile

Battery Charge Full Voltage

The battery voltage for the constant voltage regulation phase is V_{BATT_REG}. When V_{BATT_REG} is 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C. When the battery is removed, the BATT voltage is between V_{BATT_REG}-V_{RECHG} and V_{BATT_REG}.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating. When the internal junction temperature reaches the pre-set limit of T_{REG} (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via Reg06 bit [1:0].

When the junction temperature reaches 150°C, both Q1 and Q2 are turned off.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment for the chip. A resistor with an appropriate value should be connected from VDD to NTC, and the thermistor should be connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the temperature. The IC sets a pre-determined upper and lower bound of the divide ratio internally for NTC cold and NTC hot. In the MP2661, the I²C default setting is the PCB_OTP. The function can be changed through the I²C (see Table 2).

Table 2: NTC Function Selection Table

I²C Control		Function
EN_NTC	ENB_PCB_OTP	
0	x	Disable
1	1	NTC
1	0	PCB_OTP

When PCB_OTP is selected, if the NTC voltage is lower than the NTC hot threshold, both the LDO MOSFET and battery MOSFET are off. The PCB_OTP fault sets the NTC_FAULT status (Reg08 bit [1]) to 1 to indicate the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function only works in charge mode. Once the NTC voltage falls out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

Safety Timer

The IC provides both a pre-charge and a fast-charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer is one hour when the battery voltage is below V_{BATT_LOW}. The fast charge safety timer begins when the battery enters fast charging. The fast charge safety timer can be programmed through the I²C. The safety timer feature can be disabled via the I²C.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

The following actions restart the safety timer:

- A new charge cycle is kicked in
- Reg01 bit [3] is written from 0 to 1 (charge enable)
- Reg05 bit [3] is written from 0 to 1 (safety timer enable)
- Reg01 bit [7] is written from 0 to 1 (software reset)

Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, the IC starts in the watchdog timer expiration state or default mode. All registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are programmable. If the watchdog timer (Reg05 bit [5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the Reg01 bit [6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is no V_{IN}, the watchdog timer is suspended. (Figure 10)

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no V_{IN}
- Register reset Reg01 bit [7] is reset

Battery Discharge Function

If battery is connected and the input source is missing, the battery MOSFET is fully on when V_{BATT} is above the V_{UV_BATT} threshold. The 100mΩ battery MOSFET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once I_{BATT} exceeds the programmable discharge current limit (default 2A), the battery MOSFET is turned off after a 60μs delay, and the MP2661enters hiccup mode in over-current protection. The discharge current can be programmed high to 3.2A through the I²C.Ifthe discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery MOSFET is turned off and starts hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable V_{UV_BATT} threshold (default 2.8V), the battery MOSFET is turned off to prevent over-discharge.

System Short-Circuit Protection (SCP)

The MP2661 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BATT to SYS path.

The system voltage is continuously monitored. If V_{SYS} is lower than 1.5V, the system (SCP) for the IN to SYS path and the BATT to SYS path are active. I_{BATTOC} is decreased to half of the original value.

1) *IN to SYS path:* Once I_{IN} is over the protection threshold, both the LDO MOSFET and the BATT MOSFET are turned off immediately, and the IC enters hiccup mode. Otherwise, the max current limit and the setting input current limit are not reached, and I_{IN} is regulated at I_{INLMT}. Hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800μs.
2) *BATT to SYS path:* Once I_{BATT} is over the 3.7A protection threshold, both the LDO MOSFET and the BATT MOSFET are turned off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The interval of the hiccup mode is 800μs.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation. (Figure 13)

Interrupt to Host (INT)

The IC has an alert mechanism which can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of the below events can trigger the INT output:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

- Good input source detected
- UVLO or input OVP charge completed
- Charging status change
- Any fault in Reg08 (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in Reg08. After the IC exits the fault state, the fault bit could be released to 0 after the host reads Reg08. The NTC fault is not latched and always reports the current thermistor conditions.

Note that the INT needs the external pull up resistor for its open-drain connection. Suggest the resistance not lower than 300kΩ.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system:
Case A: to prevent excessive capacity discharge during the device is in shipping or storage.
Case B: allow the system power reset
The MP2661 provides both shipping mode (see figure 14) and system reset mode for different application requirements.

1). Shipping Mode:

Entering the Shipping mode: The register bit (FET_DIS), Reg06 Bit[5], controls the IC to enter the shipping mode.

During the normal operation, the battery MOSFET is turned on and this bit is 0. If this bit is set to 1 through I²C, the battery MOSFET is turned off, and the MP2661 enters shipping mode. The FET_DIS bit is reset to 0 automatically after the battery MOSFET is turned off (see Figure 6).

Exiting shipping mode: The IC can exit the shipping mode by pulling INT down.

1.1) When the IC is in the shipping mode and only the Battery is present, pulling INT down by pushing PB (see the "TYPICAL APPLICATION CIRCUIT") could wake the MP2661 up from shipping mode. (refer to table3)

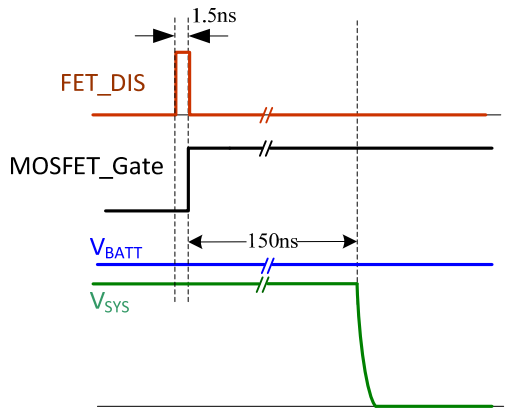


Figure 6: the time delay from FET_DIS is written (1) to the battery FET off

Table3: Exit the Shipping mode with BATT present only

	INT signal	IC exits the shipping mode
Case1	INT= low twice with the rising edge >600ns	at once
Case2	INT= low once with the rising edge >600ns	after 4s
Case3	INT= low for 4s	Once after the 4s
Case4	INT = low with the rising edge in ms level	at once

1.2) When the IC is in the shipping mode and a valid Vin powers on, the MP2661 could be woken up too. After Vin is preset, the MP2661 pulls INT low to indicate the event "Good input source detected" if the Vin is in the operation range. then, the MP2661 could be woken up from the shipping mode by the INT signal. (see Figure 7).

Table4: Exit the Shipping mode with Vin Powers on

	INT signal	IC exits the shipping mode
Case1	INT= low twice with the rising edge >600ns	at once
Case2	INT= low once with the rising edge >600ns	after 4s
Case3	INT = low with the rising edge in ms level	at once

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

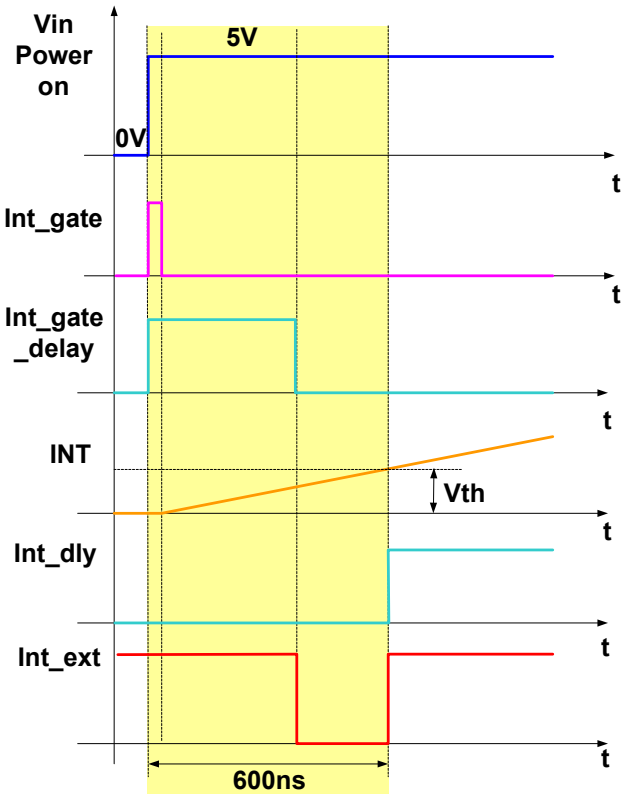


Figure 7: INT signal during Vin powers on

If FET_DIS is set to 1 during the shipping mode, the IC could still wake up after INT keeping low for 4s. But in this case, the FET_DIS bit cannot be reset to 0 automatically, it has to be reset to 0 manually through I²C.

2). Reset Mode

The IC can use INT to cut off the path from the battery to the system when system reset is needed.

Once the logic at INT is set to low for more than 16s, the battery is disconnected from the system by turning off the battery MOSFET.

The off state lasts for 4s, then the battery MOSFET is turned on automatically, and the system is powered by the battery again. During the 4s off period, INT pin voltage level could be high or low. The IC can reset the system by controlling INT (see Figure 8).

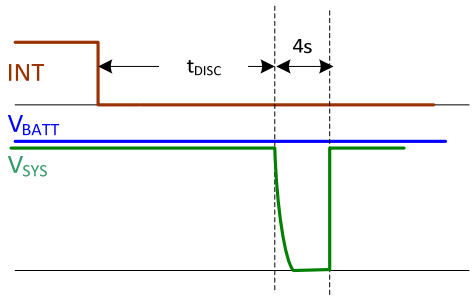


Figure 8: System Reset Function Operation Profile

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

I²C REGISTER MAP

IC Address: 09H (reserved some trim options)

Input Source Control Register/Address: 00H (Default: 01001111)

Bit	Symbol	Description	Read/Write	Default
Bit 7	EN_HIZ(6)	0: disable 1: enable	Read/write	Disable (0)
Input Voltage Regulation				
Bit 6	V_{IN_REG} [3]	640mV	Read/write	Offset: 3.88V Range: 3.88V -5.08V Default: 4.60V (1001)
Bit 5	V_{IN_REG} [2]	320mV		
Bit 4	V_{IN_REG} [1]	160mV		
Bit 3	V_{IN_REG} [0]	80mV		
Input Current Limit				
Bit 2	I_{IN_LIM} [2]	000: 85mA 001: 130mA 010: 175mA 011: 220mA 100: 265mA 101: 310mA 110: 355mA 111: 455mA	Read/write	455mA (111)
Bit 1	I_{IN_LIM} [1]			
Bit 0	I_{IN_LIM} [0]			

NOTE:

6) This bit only controls the on and off of the LDO MOSFET.

Power-On Configuration Register/Address: 01H (Default: 0000 0100)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Register reset	0: keep current setting 1: reset	Read/write	Keep current setting (0)
Bit 6	I²C watchdog timer reset	0: normal 1: reset	Read/write	Normal(0)
Bit 5	Reserved			
Bit 4	Reserved			
Charger Configuration				
Bit 3	CEB	0: charge enabled 1: charge disabled	Read/write	Charge enabled (0)
Battery UVLO Threshold				
Bit 2	V_{UV_BATT} [2]	0.4V	Read/write	Offset: 2.4V Range: 2.4V-3.1V Default: 2.8V (100)
Bit 1	V_{UV_BATT} [1]	0.2V		
Bit 0	V_{UV_BATT} [0]	0.1V		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

I²C REGISTER MAP*(continued)*

Charge Current Control Register/Address: 02H (Default: 000 01110)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Bit 6	Reserved			
Bit 5	Reserved			
Charge Current Setting				
Bit 4	I_{CHG} [4]	272mA	Read/write	Offset: 8mA Range: 8mA -535mA Default: 246mA (01110)
Bit 3	I_{CHG} [3]	136mA		
Bit 2	I_{CHG} [2]	68mA		
Bit 1	I_{CHG} [1]	34mA		
Bit 0	I_{CHG} [0]	17mA		

Pre-Charge/Termination Current/Address: 03H (Default: 01001 010)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
BATT to SYS Discharge Current Limit				
Bit 6	I_{DCH}[3]	1600mA	Read/write	Offset: 200mA Range: 400mA-3.2A Valid range: 0001 - 1111 Default:2000mA(1001)
Bit 5	I_{DCH} [2]	800mA		
Bit 4	I_{DCH} [1]	400mA		
Bit 3	I_{DCH} [0]	200mA		
PCB_OTP Enable				
Bit 2	ENB_PCB_OTP	0: enable 1: disable	Read/write	Enable(0)
Trickle Current				
Bit 1	I_{TC} [1]	14mA	Read/write	Offset: 6mA Range: 6mA-27mA Default: 20mA (10)
Bit 0	I_{TC} [0]	7mA		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

I²C REGISTER MAP*(continued)*

Charge Voltage Control Register/Address: 04H (Default: 1010 0011)

Bit	Symbol	Description	Read/Write	Default
Battery Regulation Voltage				
Bit 7	V_{BATT_REG} [5]	480mV	Read/write	Offset: 3.60V Range: 3.60V - 4.545V Default: 4.2V (101000)
Bit 6	V_{BATT_REG} [4]	240mV		
Bit 5	V_{BATT_REG} [3]	120mV		
Bit 4	V_{BATT_REG} [2]	60mV		
Bit 3	V_{BATT_REG} [1]	30mV		
Bit 2	V_{BATT_REG} [0]	15mV		
Trickle Charge Threshold				
Bit 1	V_{BATT_LOW}	0: 2.8V 1: 3.0V	Read/write	3.0V (1)
Battery Recharge Threshold (below V_{BATT_REG})				
Bit 0	V_{RECHG}	0: 150mV 1: 300mV	Read/write	300mV (1)

Charge Termination/Timer Control Register/Address: 05H (Default: 0100 1010)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Termination Setting (the termination is allowed or not)				
Bit 6	EN_BF	0: disable 1: enable	Read/write	Enabled(1)
I²C Watchdog Timer Limit				
Bit 5	WATCHDOG [1]	00: disable timer 01: 40s 10: 80s 11: 160s	Read/write	Disable timer(00)
Bit 4	WATCHDOG [0]			
Safety Timer Setting				
Bit 3	EN_TIMER	0: disable 1: enable	Read/write	Enable timer (1)
Constant Current Charge Timer				
Bit 2	CHG_TMR [1]	00: 3hrs 01: 5hrs 10: 8hrs 11: 12hrs	Read/write	5hrs (01)
Bit 1	CHG_TMR [0]			
Termination Timer Control (when TERM_TMR is enabled, the IC will not suspend the charge current after charge termination)				
Bit 0	TERM_TMR	0: disable 1: enable	Read/write	(0)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

I²C REGISTER MAP*(continued)*

Miscellaneous Operation Control Register/Address: 06H (Default: 0100 1011)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Bit 6	TMR2X_EN	0: disable 2X extended safety timer during PPM 1: enable 2X extended safety timer during PPM	Read/write	Enable (1)
Bit 5	FET_DIS(7)	0: enable 1: turn off	Read/write	Enabled(0)
Bit 4	Reserved			
Bit 3	EN_NTC	0: disable 1: enable	Read/write	Enabled(1)
Bit 2	Reserved			
Thermal Regulation Threshold				
Bit 1	T_{REG} [1]	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Read/write	120°C (11)
Bit 0	T_{REG} [0]			

NOTE:

7) This bit controls the on and off of the battery MOSFET, including the charging and discharging.

System Status Register/Address: 07H (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Revision				
Bit 6	Rev [1]	Revision number	Read only	(00)
Bit 5	Rev [0]			
Bit 4	CHG_STAT [1]	00: not charging 01: trickle charge 10: charge 11: charge done	Read only	Not charging (00)
Bit 3	CHG_STAT [0]			
Bit 2	PPM_STAT	0: no PPM 1: in PPM	Read only	No PPM (0) (no power-path management happens)
Bit 1	PG_STAT	0: power fail 1: power good	Read only	Not power good (0)
Bit 0	THERM_STAT	0: no thermal regulation 1: in thermal regulation	Read only	Normal (0)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

I²C REGISTER MAP*(continued)*

Fault Register/Address: 08H (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Bit 6	WATCHDOG_FAULT	0: normal 1: watchdog timer expiration	Read only	Normal (0)
Bit 5	VIN_FAULT	0: normal 1: input fault (OVP or bad source)	Read only	Normal (00)
Bit 4	THEM_SD	0: normal 1: thermal shutdown	Read only	
Bit 3	BAT_FAULT	0: normal 1: battery OVP	Read only	Normal (0)
Bit 2	STMR_FAULT	0: normal 1: safety timer expiration	Read only	Normal (0)
Bit 1	NTC_FAULT [1]	0: normal 1: NTC hot	Read only	Normal (00)
Bit 0	NTC_FAULT [0]	0: normal 1: NTC cold		

OTP(8) MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	N/A			I_{CHG}: **8mA-535mA / 17mA** step				
0x03	N/A					PCB_OTP	I_{TC}: **6mA-27mA/7mA step**	
0x04	V_{BATT_REG}: **3.6V-4.545V / 15mV** step						N/A	
0x05	N/A		WATCHDOG	N/A				

OTP(8) DEFAULT

OTP(8) Items	Default
I_{CHG}	246mA
PCB_OTP	Enable
I_{TC}	20mA
V_{BATT_REG}	4.2V
WATCHDOG	Disable

NOTE:
8) OTP is One Time Program.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

STATE CONVERSION CHART

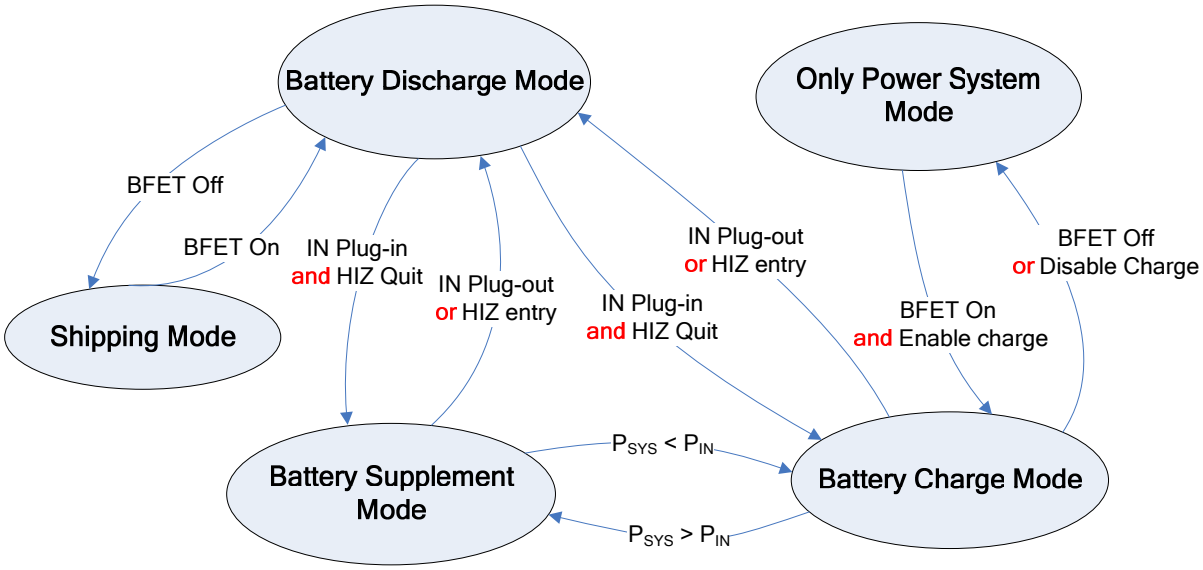


Figure 9: State Machine Conversion

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

CONTROL FLOW CHART

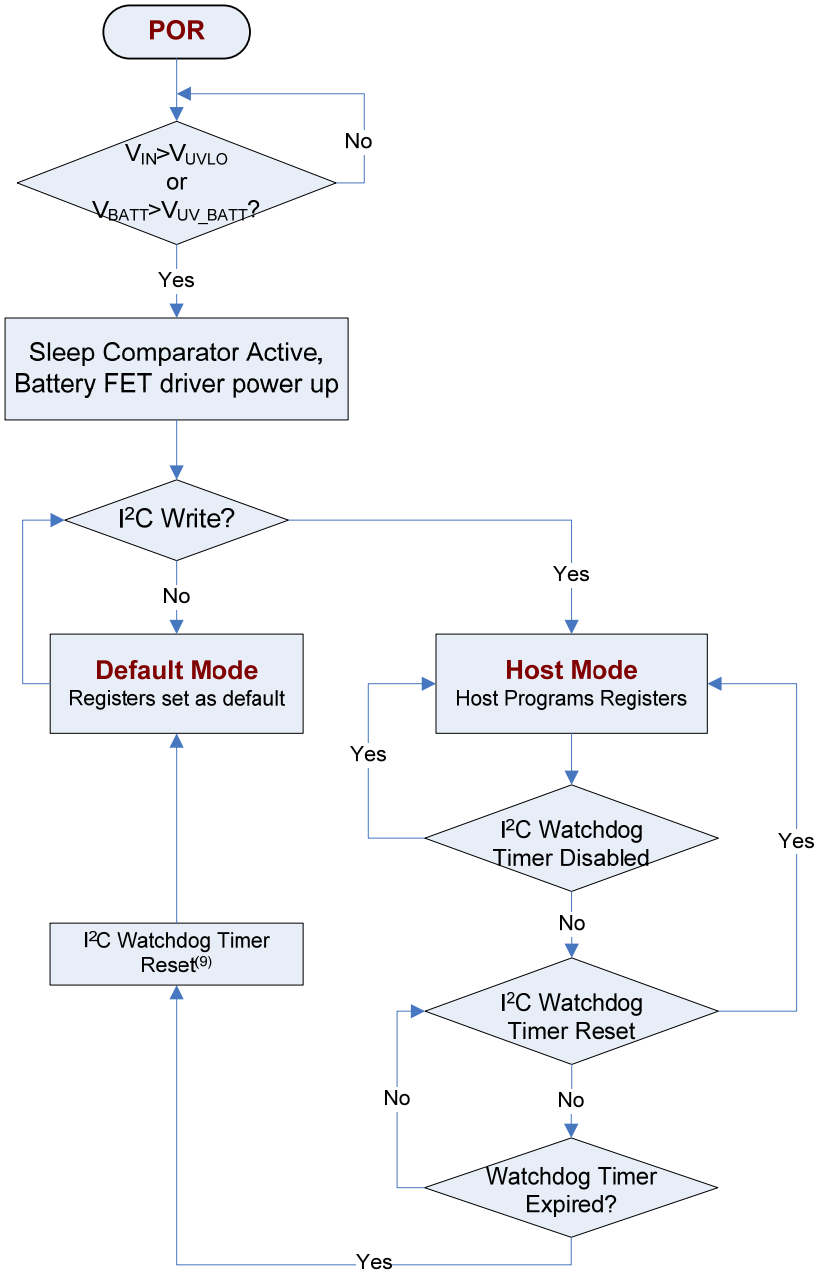


Figure 10: Default Mode and Host Mode Selection(10)

NOTES:

9) Once the watchdog timer expires, the I²C watchdog timer must be reset, or the watchdog timer is not valid in the next cycle.

10) The watchdog timer is held when V_{IN} is not present.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

CONTROL FLOW CHART*(continued)*

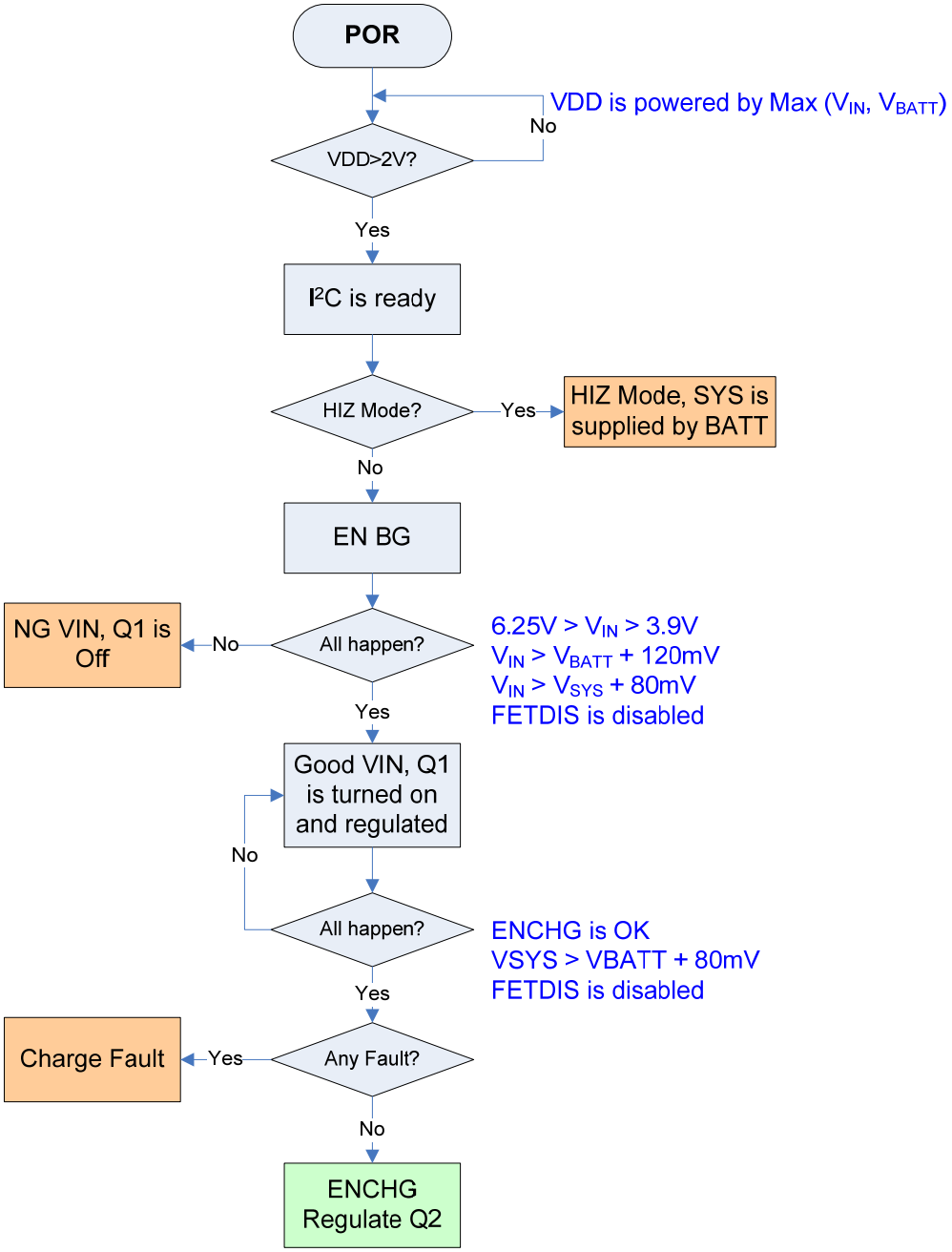


Figure 11: Input Power Start-Up Flow Chart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

CONTROL FLOW CHART*(continued)*

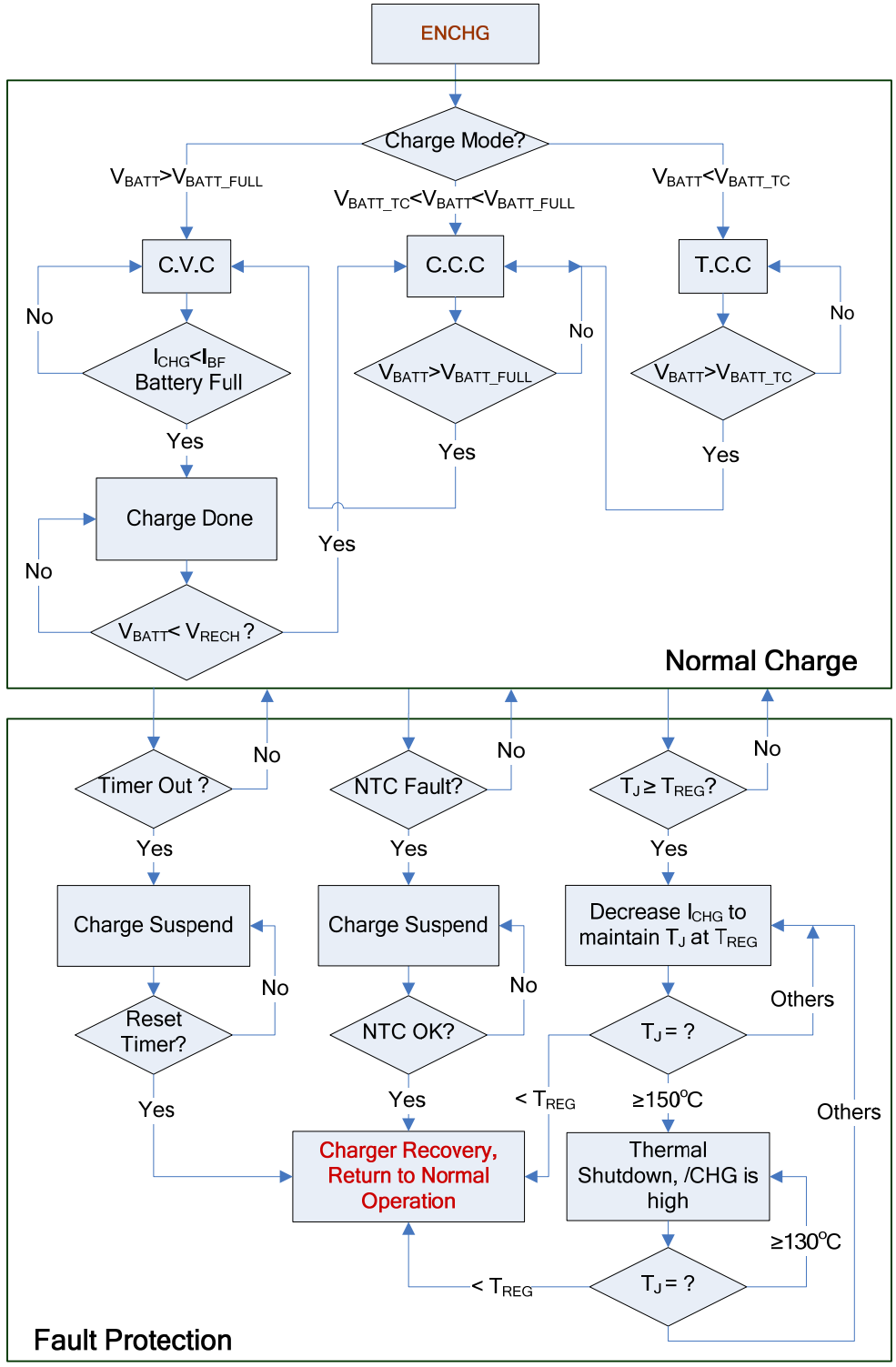


Figure 12: Charging Process

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

CONTROL FLOW CHART*(continued)*

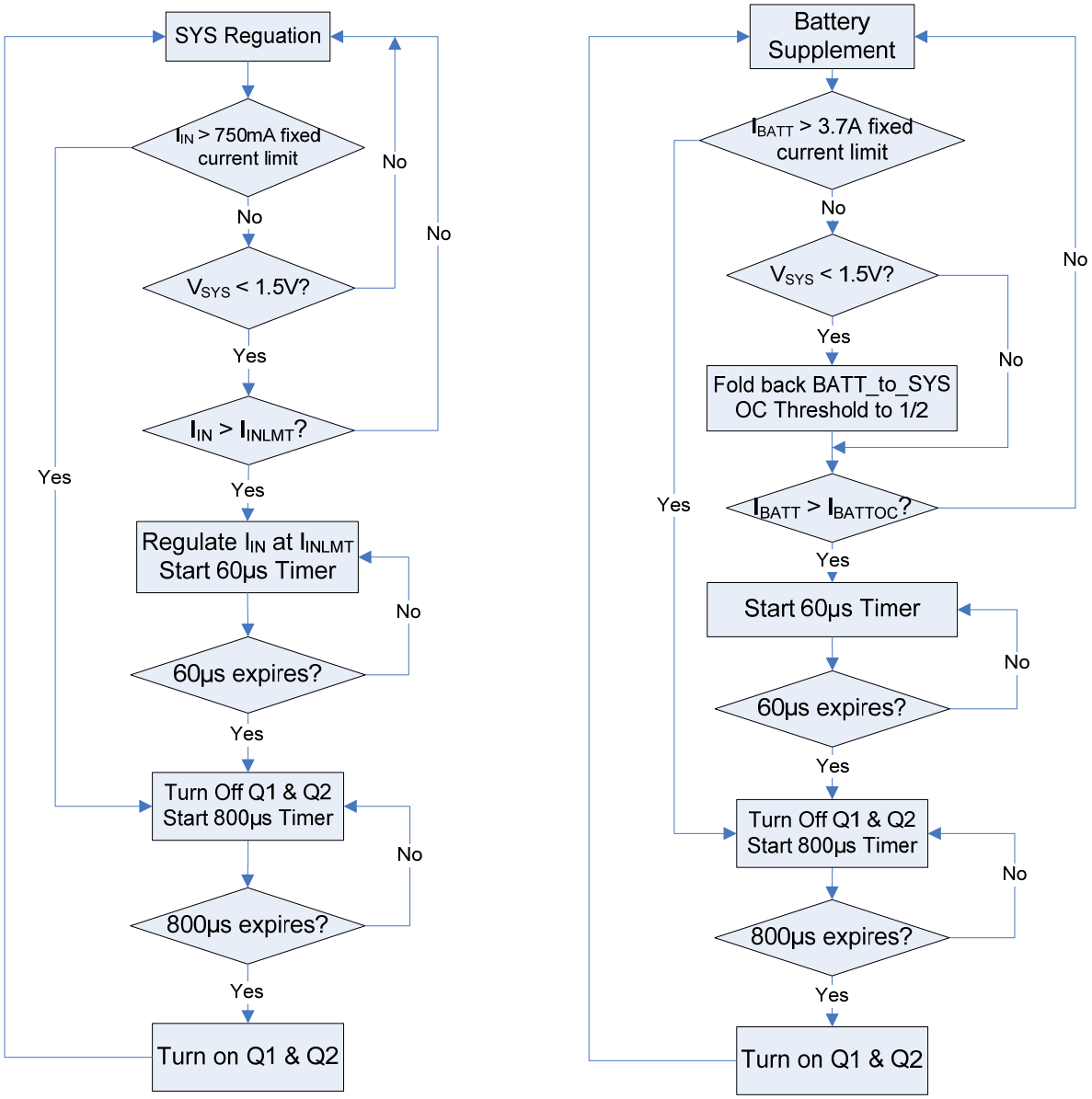


Figure 13: System Short-Circuit Protection

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

CONTROL FLOW CHART*(continued)*

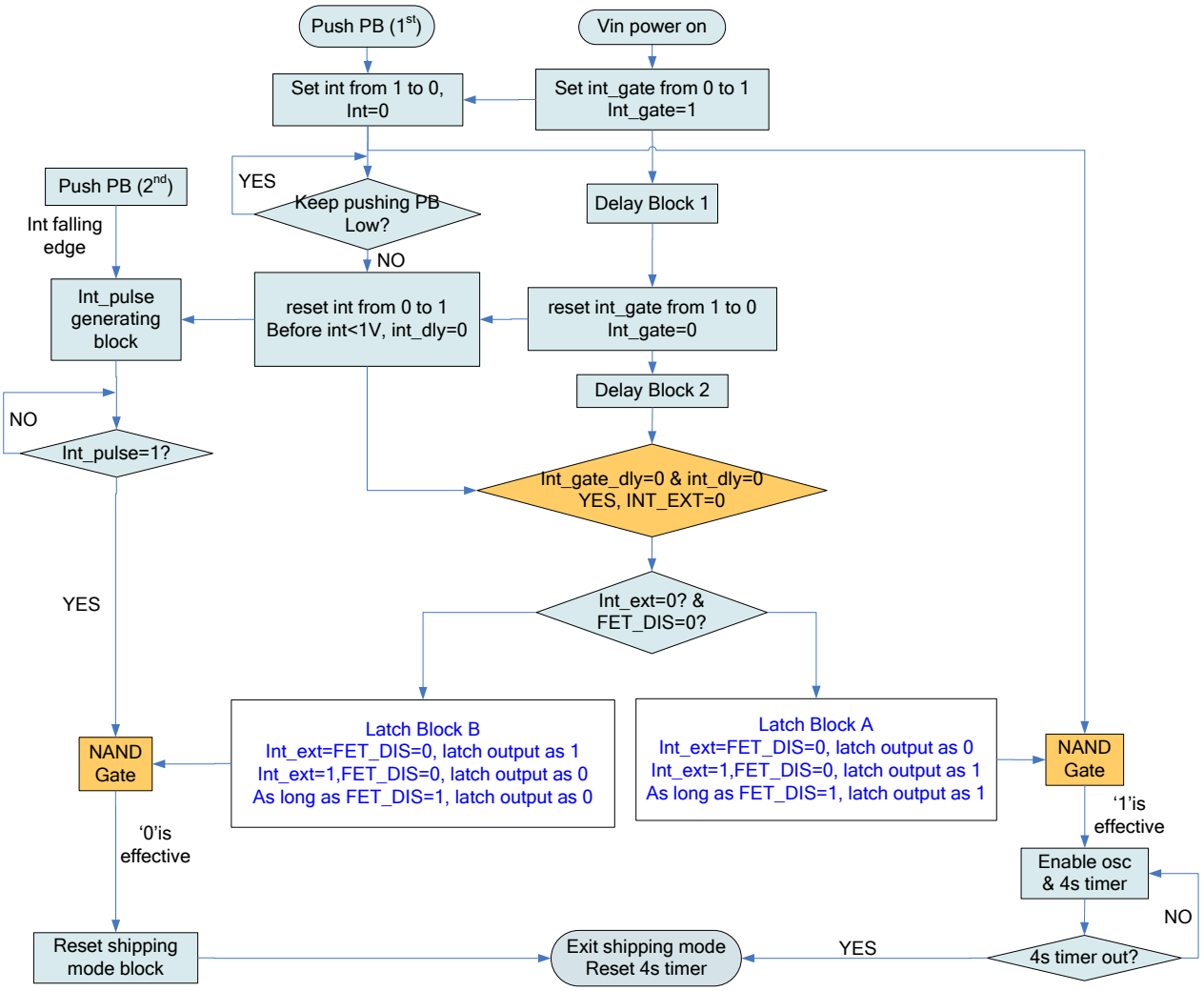


Figure 14: MP2661 Exits the Shipping Mode

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting a Resistor for the NTC Sensor

NTC uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors ($R_{T1}$and R_{T2})allow the high temperature limit and low temperature limit to be programmed independently. In other words, the IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors. $R_{T1}$and R_{T2}depend on the type of the NTC resistor and can be calculated with Equation (1) and Equation (2):

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the value of the NTC resistor at a high temperature of the required temperature operation range, and R_{NTCL} is the value of the NTC resistor at a low temperature.

Selecting the External Capacitor

Like most low-dropout regulators, the MP2661 requires external capacitors for regulator stability and voltage spike immunity. The device is specifically designed for portable applications requiring minimum board space and small components. These capacitors must be correctly selected for optimal performance.

An input capacitor is required for stability. A capacitor at least 1μF must be connected between IN and GND for stable operation over the entire load current range. There can be more output capacitance than input as long as the input is at least 1μF.

The IC is designed specifically to work with a very small ceramic output capacitor(typically 2.2μF). A ceramic capacitor with X5R or X7R type dielectrics at least 2.2μF is suitable in the MP2661 application circuit. For the MP2661, the output capacitor should be connected between SYS and GND with thick traces and a small loop area.

A capacitor from BATT to GND is also necessary for the MP2661, and the typical capacitance value is 2.2μF. A ceramic capacitor with X5R or X7R type dielectrics at least 2.2μF is suitable for the application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place the external capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2. Place the PCB trace connecting the capacitor between VDD and GND very close to the IC.
3. Keep the AGND for the I²C wire clean and away from PGND.
4. Place the I²C wire in parallel.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

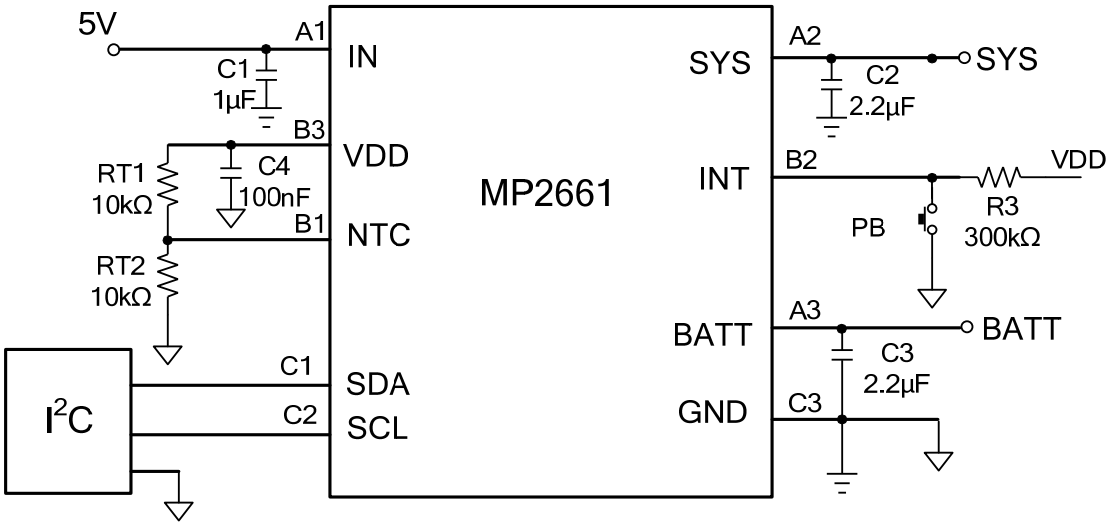


Figure15: MP2661 Typical Application Circuit with 5V Input

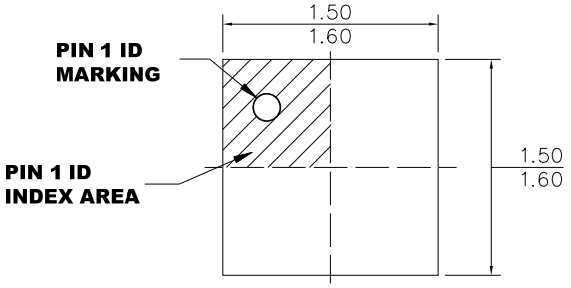
Table 5: The Key BOM of Figure 15

Qty	Ref	Value	Description	Package	Manufacture
1	C1	1µF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C2, C3	2.2µF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C4	100nF	Ceramic Capacitor;16V; X5R or X7R	0603	Any

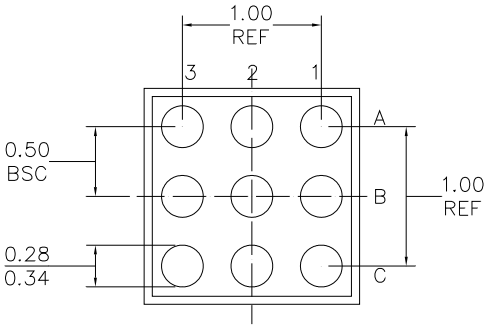
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018MPS. All Rights Reserved.

PACKAGE INFORMATION

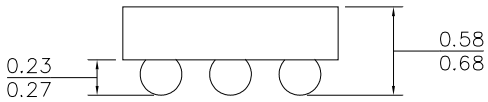
WLCSP-9 (1.55mmx1.55mm)



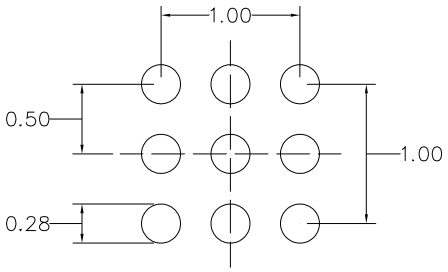
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.