MP24971

1.5A, 50V, 100kHz, 5V Fixed Output Step-Down Converter with Programmable Current Limit and Output Line-Drop Compensation

The Future of Analog IC Technology

DESCRIPTION

The MP24971 is a monolithic, step-down, switch-mode converter with a programmable output-current limit. It has a fixed 5V/1.5A continuous output over a wide input supply range, and has excellent load and line regulation. It has an internal 2ms-to-4ms soft-start that prevents inrush current at start-up, and compensates for output line drop.

MP24971 achieves a low EMI signature with well-controlled switching edges.

It has fault-condition protections including hiccup-mode current limit protection, short-circuit protection, output over-voltage protection, and thermal shutdown.

The MP24971 requires a minimal number of readily-available standard external components, and is available in SOIC8 and SOIC8E packages.

FEATURES

- Wide 8V-to-50V Operating Input Range
- Output Over-Voltage Protection
- 5V Fixed Output
- 0.4Ω Internal Power MOSFET
- Internal 4ms Soft-Start
- Stable with Low-ESR Ceramic Output Capacitors
- Fixed 100kHz Frequency
- Low EMI Signature
- Thermal Shutdown
- Output Line-Drop Compensation
- Hiccup Circuit Limit and Short Circuit Protection
- Available in SOIC8 and SOIC8E Package

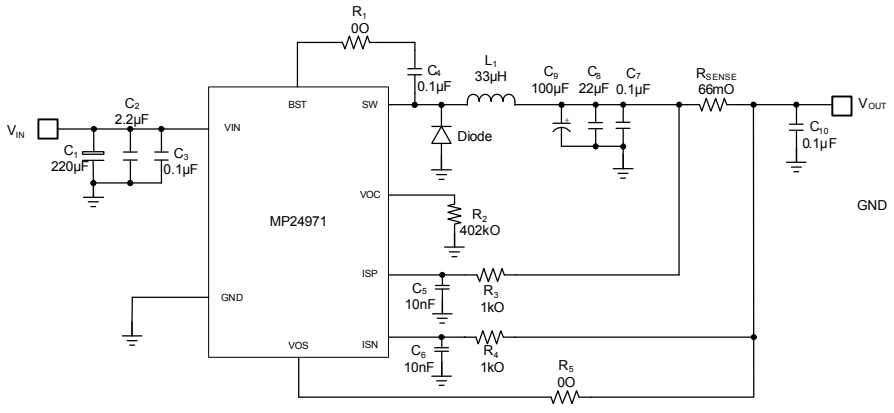
APPLICATIONS

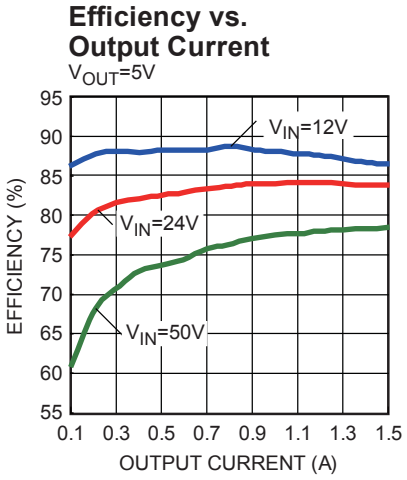
- USB Power Supplies
- Automotive Power Adapters
- Power Supplies for Linear Chargers

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TYPICAL APPLICATION





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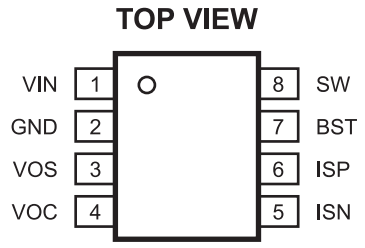
ORDERING INFORMATION

Part Number	Package	Top Marking	Operating Temperature (T_J)
MP24971DS*	SOIC8	MP24971	-40°C to +125°C
MP24971DN**	SOIC8E	MP24971	-40°C to +125°C

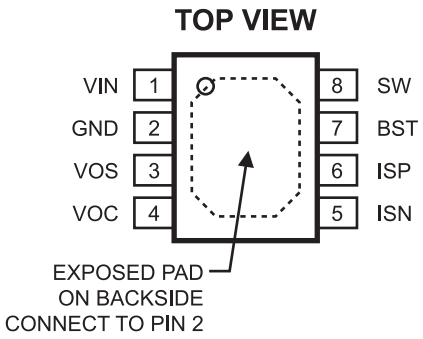
* For Tape & Reel, add suffix –Z (eg. MP24971DS–Z);
For RoHS, compliant packaging, add suffix –LF (eg. MP24971DS–LF–Z).

** For Tape & Reel, add suffix –Z (eg. MP24971DN–Z);
For RoHS, compliant packaging, add suffix –LF (eg. MP24971DN–LF–Z).

PACKAGE REFERENCE



SOIC8



SOIC8E

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} 60V
V_{ISN}, V_{ISP}, V_{VOS} ..... 0V to 8V
$|V_{ISN} - V_{ISP}|$ ..... 0V to 0.4V
V_{SW} ..... -0.3V to (V_{IN} + 0.3V)
V_{BST} ..... V_{SW} + 6.5V
All Other Pins ..... -0.3V to +6.5V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C
Continuous Power Dissipation (T_A = 25°C) (2)
SOIC8 ..... 1.38W
SOIC8E 2.5W

ESD Susceptibility

HBM (Human Body Mode) 2kV

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 8V to 50V
Maximum Junction Temp. (T_J) ..... 125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8	90	45	°C/W
SOIC8E	50	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Output Voltage	V_{OUT}	8V ≤ V_{IN} ≤ 50V, R_{SENSE}=0Ω	4.85	5	5.15	V
Output Over-Voltage Protection	V_{OVP}		5.69	6	6.2	V
Switch-On Resistance	$R_{DS(ON)}$			0.4	0.5	Ω
Switch Leakage		V_{ISN} = 6.5V, V_{SW} = 0V		0.1	1(5)	μA
Current Limit			3.5	4.4	5.2	A
Oscillator Frequency	f_{SW}		70	100	140	kHz
Bootstrap Voltage	V_{BST} - V_{SW}			4		V
Minimum On Time	t_{ON}		50	100	250	ns
SW Rising Edge	t_{RISE}			50	100	ns
SW Falling Edge	t_{FALL}			85	150	ns
Under-Voltage Lockout Threshold Rising			2.8	3.5	4.2	V
Under-Voltage Lockout Threshold Hysteresis			200			mV
Load-Line Compensation Gain	V_{VOC}	V_{ISP}-V_{ISN}=50mV	200	330	450	mV
		V_{ISP}-V_{ISN}=100mV	500	620	700	
Current Sense Voltage	V_{ISP}-V_{ISN}	V_{ISN}=5V	90	100	110	mV
Input Bias Current (ISN, ISP)	$I_{BIAS\ (ISN,ISP)}$	V_{ISP}=V_{ISN}=5V	-1	-0.5	+1	μA
Supply Current (Quiescent)		V_{ISN} = V_{VOS} = 5.5V		1.2	1.5	mA
Thermal Shutdown				150		°C

Note:

5) Guaranteed by design.

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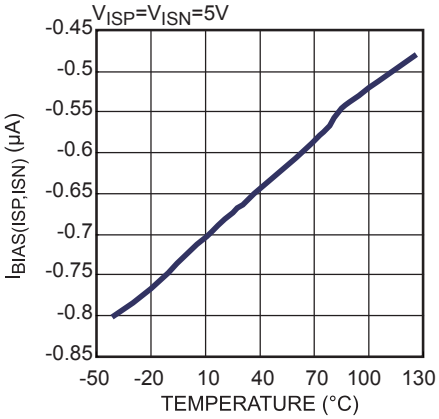
PIN FUNCTIONS

Package Pin #	Name	Description
1	VIN	Supply Voltage. Operates from an unregulated 8V-to-50V input. Requires decoupling capacitor(s)—C_{IN}—to limit voltage spikes. Drain of the internal power MOSFET; supplies power to the whole chip.
2	GND Exposed Pad	Ground. Voltage reference of the regulated output voltage. GND node should be placed outside of the diode-to-C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part. Connect exposed pad to GND plane for optimal thermal performance.
3	VOS	Output Voltage Sense. Connect directly to the output.
4	VOC	Output Line Drop Compensator. Connect to GND through a resistor to compensate for the output voltage drop.
5	ISN	Negative Current Sense Input. Used for limiting load current and for over-voltage protection. Native 6V over-voltage protection threshold.
6	ISP	Positive Current Sense Input. Used for load current limiting.
7	BST	Bootstrap. Requires a capacitor to drive the power MOSFET gate above the supply voltage. Connected capacitor between SW and BST pins to form a floating supply across the power MOSFET driver. An on-chip regulator charges the external bootstrap capacitor. If the on-chip regulator is not powerful enough, add a diode from V_{IN} or V_{OUT} to charge the external boot-strap capacitor.
8	SW	Switch Output. Output power supply.

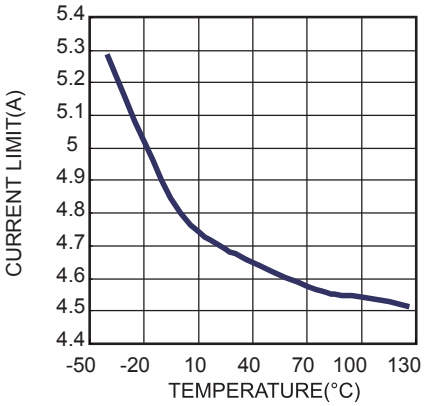
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TYPICAL CHARACTERISTICS

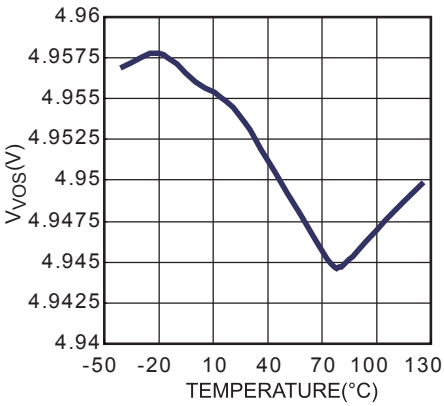
$I_{BIAS(ISP,ISN)}$ vs. Temperature



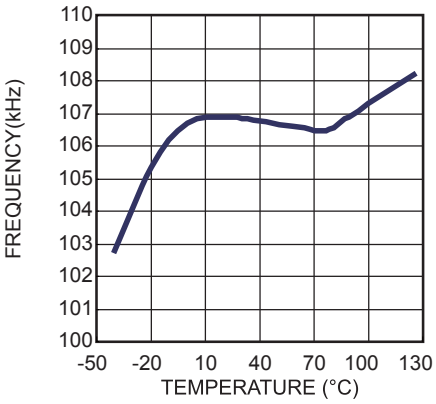
Current Limit vs. Temperature



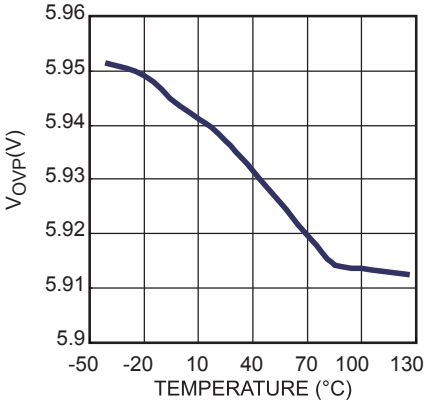
V_{VOS} vs. Temperature



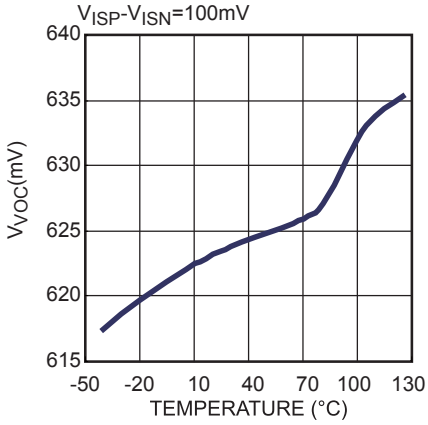
Frequency vs. Temperature



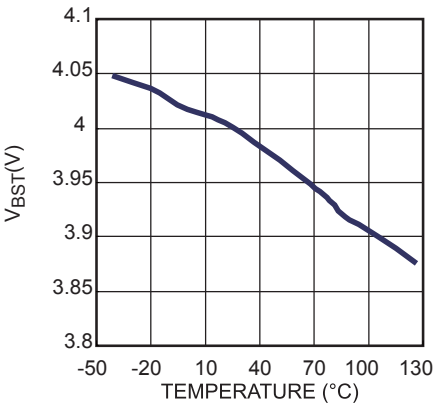
V_{OVP} vs. Temperature



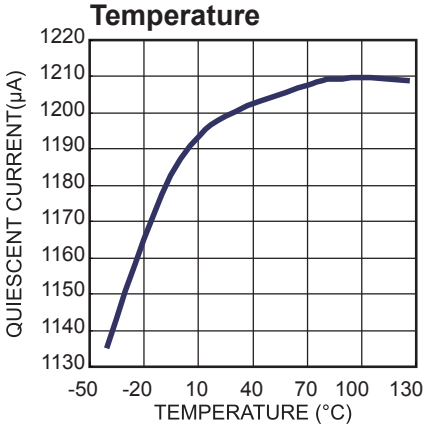
V_{VOC} vs. Temperature



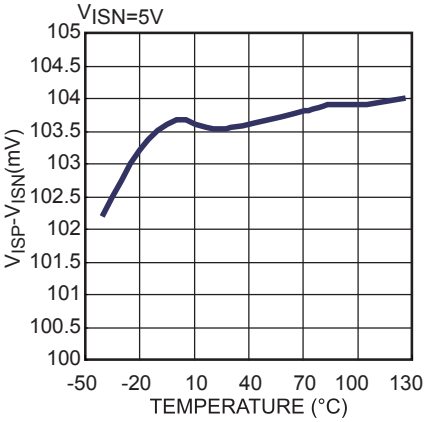
V_{BST} vs. Temperature



Quiescent Current vs. Temperature



V_{ISP}-V_{ISN} vs. Temperature



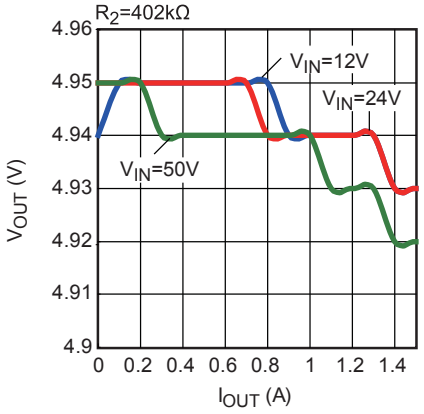
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TYPICAL PERFORMANCE CHARACTERISTICS

C1=220µF, C2=2.2µF, C8=22µF, C9=100µF, L=33µH, R_{SENSE}=66mΩ, T_A=25°C, unless otherwise noted.

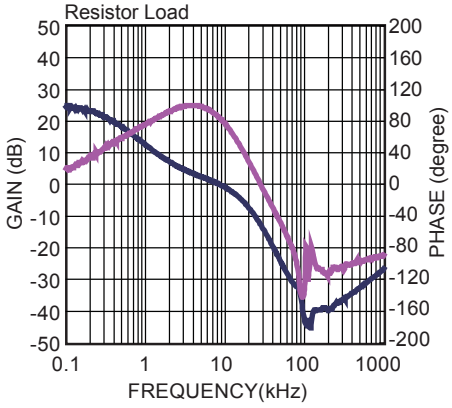
Output Line Drop Compensation

R_{SENSE}=50mΩ, R_{TRACE}=225mΩ
R_2=402kΩ



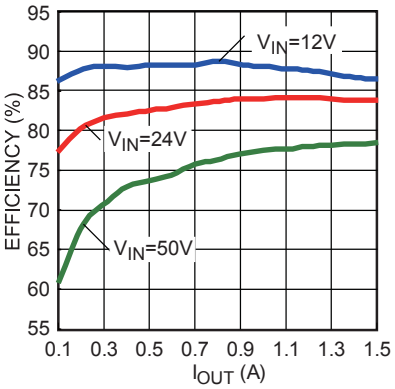
Loop Gain with Phase Margin

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.5A
Resistor Load



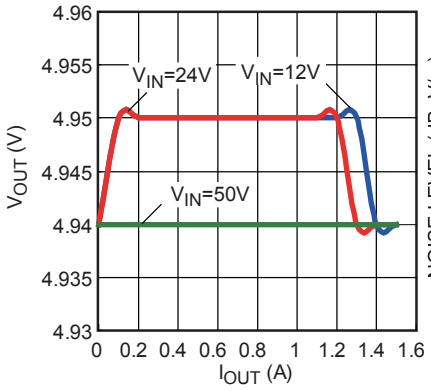
Efficiency vs. Output Current

V_{OUT}=5V



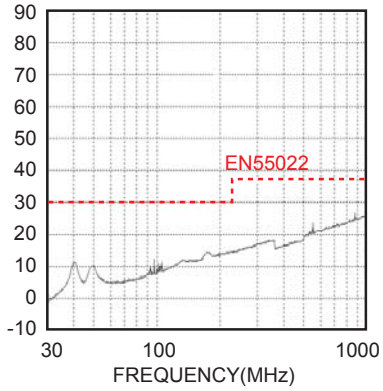
Load Regulation

Connect ISP, ISN to GND



EMI Radiation

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.5A
Resistor Load



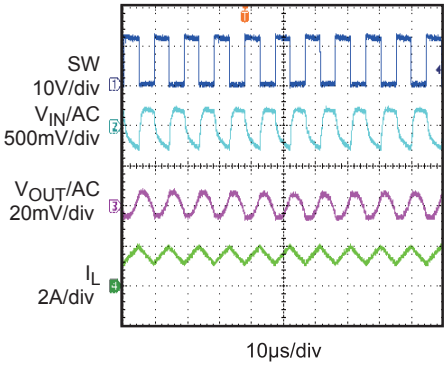
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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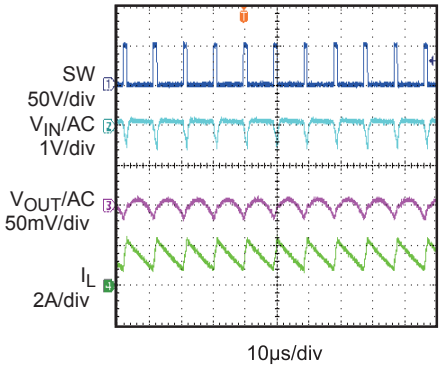
Steady State

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.5A E-Load



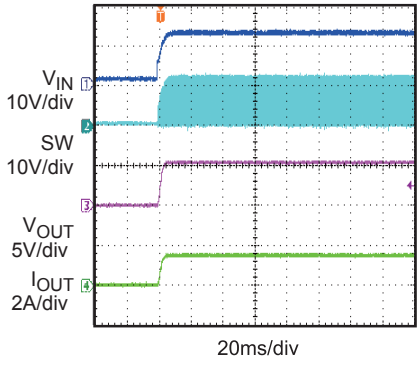
Steady State

V_{IN}=50V, V_{OUT}=5V, I_{OUT}=1.5A E-Load



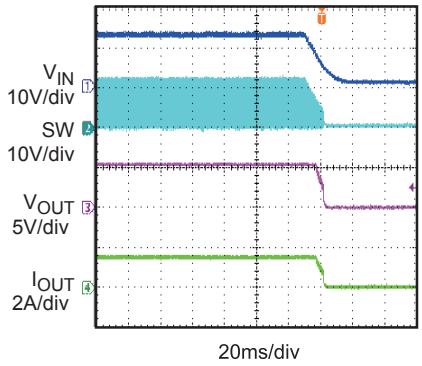
Power Ramp Up

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.5A
Resistor Load



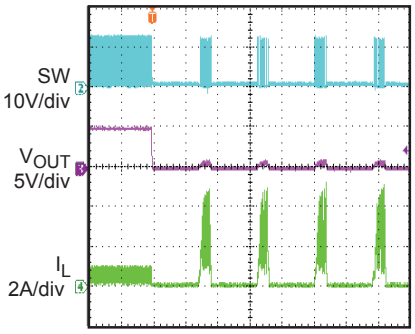
Power Ramp Down

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.5A
Resistor Load



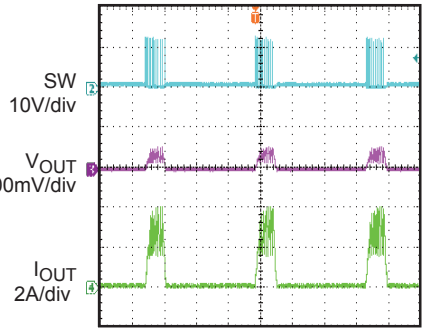
Short Circuit Enter

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.5A



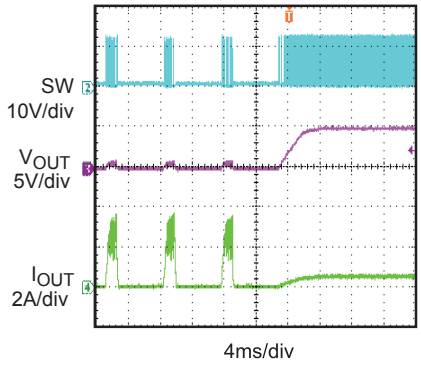
Short Circuit Steady

V_{IN}=12V, V_{OUT}=5V



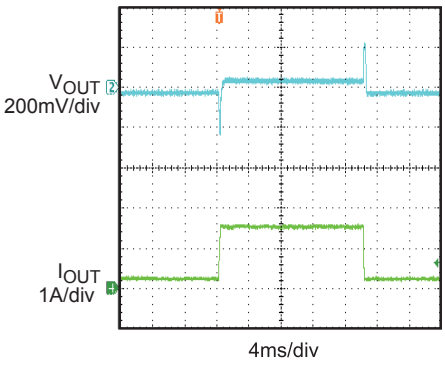
Short Circuit Recovery

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.5A



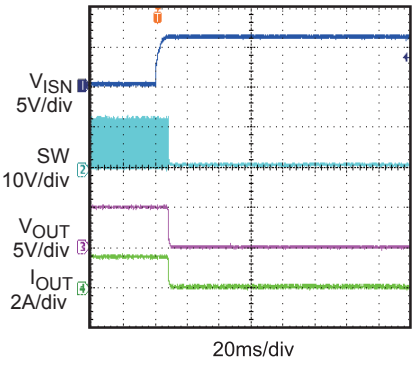
Load Transient Response

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.3A-1.5A
Slew Rate=6.4mA/□s



Over Voltage Protection

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.5A
Add an 6V External Power to ISN



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FUNCTIONAL BLOCK DIAGRAM

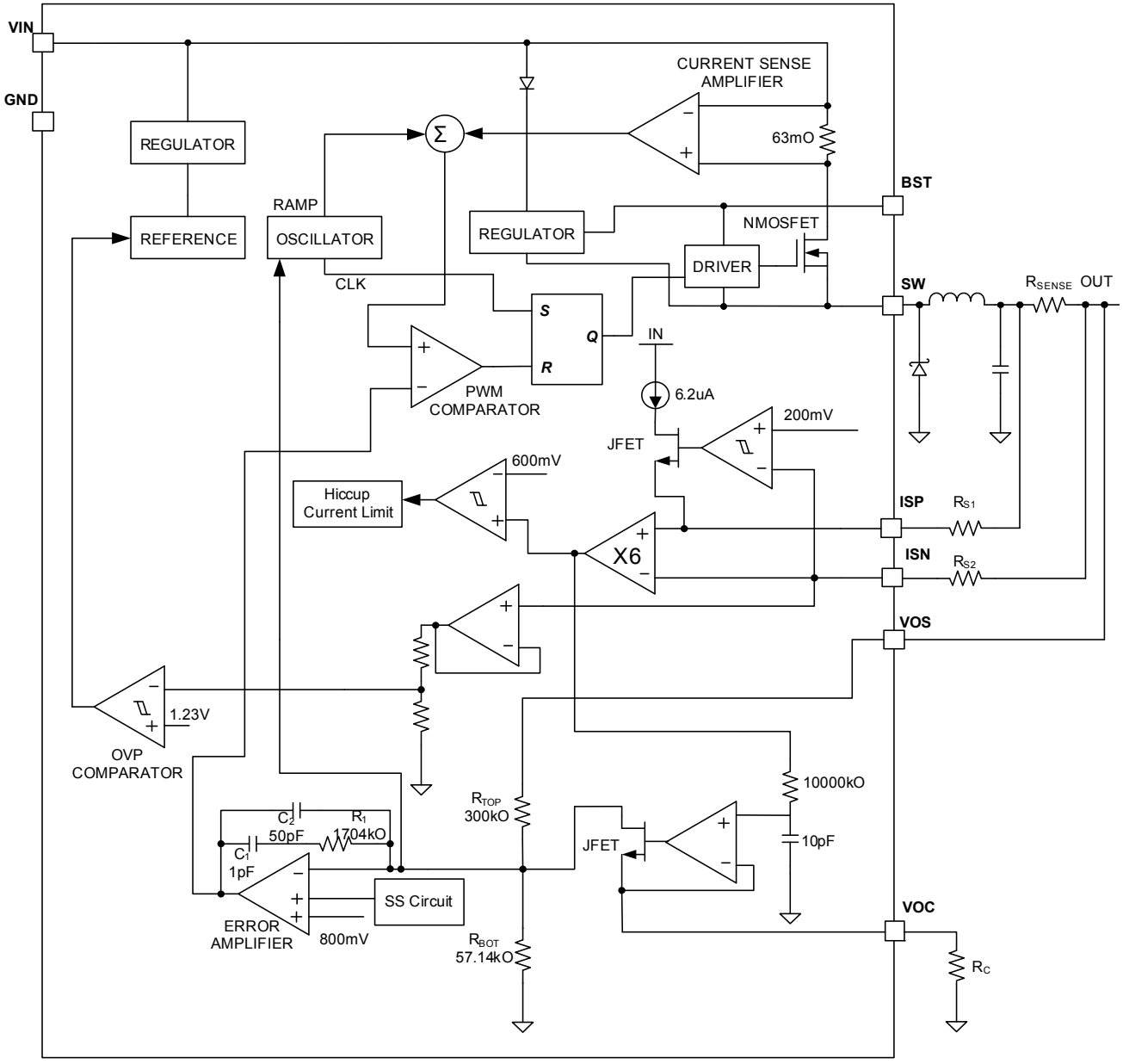


Figure 1—Function Block Diagram

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OPERATION

Main Control Loop

The MP24971 is a current-mode buck regulator where the output voltage of the error amplifier (EA) is proportional to the peak inductor current.

When a cycle starts, SW is disconnected and the EA output voltage is higher than the current sense amplifier (CSA) output. The rising edge of the 100kHz CLK signal sets the RS flip-flop, which connects SW and the inductor to the input supply.

The CSA amplifies the rising inductor current. The PWM comparator (PWM_{COMP}) compares sum of the CSA output and the ramp compensation (positive input) against the EA output (negative input). When the positive PWM_{COMP} input exceeds the negative PWM_{COMP} input, the RS flip-flop resets and the MP24971 reverts to its initial SW off state: Otherwise, the falling edge of the CLK resets the flip-flop.

The EA amplifies the voltage difference between V_{OUT} (connected through the VOS pin) and the 800mV reference: Because V_{OUT} connects to the negative input of the EA, when V_{OUT} drops below 5V, the EA output increases. Since the EA output voltage is proportional to the peak inductor current, an increase in inductor voltage increases current delivered to the output. An external Schottky Diode dissipates the inductor current when SW is off.

Hiccup-Mode Current Limit Protection

The ISP and ISN pins sense the output current information for current limit protection. Once the V_{SENSE} exceeds the 100mV voltage limit threshold, the current limit loop will turn off the high-side MOSFET immediately. The internal soft-start circuit resets after the VOS voltage drops below 1.9V and V_{COMP} rises above 3V; at this point, the high side switch turns on and MP24971 restarts with a full soft start. This hiccup process repeats until the device stops detecting a fault.

The current limit value can be lowered by an internal current source and external resistors connected to ISN and ISP pins when the output voltage drops below 200mV. This feature can greatly reduce the average short circuit current.

Output Over-Voltage Protection

The MP24971 has output over-voltage protection to prevent the output voltage from rising above a threshold of 6V—such as if the output sense is left open—and prevents any voltage damage to the circuit load. If the output voltage—as sensed by the ISN pin—rises above 6V, the high-side MOSFET will turn off immediately and part will be lathed off after a timer delay.

Output-Line–Drop Compensation

MP24971 is capable of compensating an output voltage drop—such as high impedance caused by a very long trace—to keep a constant 5V load-side voltage. Compensation feedback comes from the VOS pin and through the R_{TOP} resistor. Program the load line compensation gain using a resistor connected to VOC pin, selected based on R_{SENSE} and R_{TRACE} (Figure 2) values.

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APPLICATION INFORMATION

Setting the Output Line Drop Compensation

Long traces to the circuit load induce a voltage drop between V_{OUT} and V_{LOAD}. that can be described as:

$$V_{DROP} = I_{OUT} \times R_{TRACE} \quad (1)$$

Where $R_{TRACE} = R_{TRACE1} + R_{TRACE2}$ as seen in Figure 2. Then, the V_{LOAD} is:

$$V_{LOAD} = V_{OUT} - I_{OUT} \times R_{TRACE} \quad (2)$$

Supplying an accurate and consistent load voltage over current-dependant trace resistance necessitates line-drop compeonsation.

MP24971 offers a compensation method that adjusts the FB voltage slightly according to the load current.

The relation between V_{OUT} and V_{FB} can be described by:

$$\frac{V_{OUT} - V_{FB}}{R_{TOP}} = \frac{V_{FB}}{R_{BOT}} + \frac{I_{OUT} \times R_{SENSE} \times 6}{R_C} \quad (3)$$

Where, V_{FB} is 0.8V.
Then, the V_{OUT} can be calculated by:

$$V_{OUT} = 5V + \frac{I_{OUT} \times R_{SENSE} \times 6 \times R_{TOP}}{R_C} \quad (4)$$

The V_{LOAD} is determined by:

$$V_{LOAD} = 5V + \frac{I_{OUT} \times R_{SENSE} \times 6 \times R_{TOP}}{R_C} \quad (5)$$

$$-I_{OUT} \times R_{TRACE}$$

To maintain a V_{LOAD} that is not variable with load current, balance the equation below:

$$\frac{I_{OUT} \times R_{SENSE} \times 6 \times R_{TOP}}{R_C} = I_{OUT} \times R_{TRACE} \quad (6)$$

Where R_{TOP} is 300kΩ. Simplifying, we find that R_C comes out to:

$$R_C = \frac{R_{SENSE} \times 6 \times 300k\Omega}{R_{TRACE}} \quad (7)$$

Where R_{SENSE} is known and R_{TRACE} can be tested or evaluated

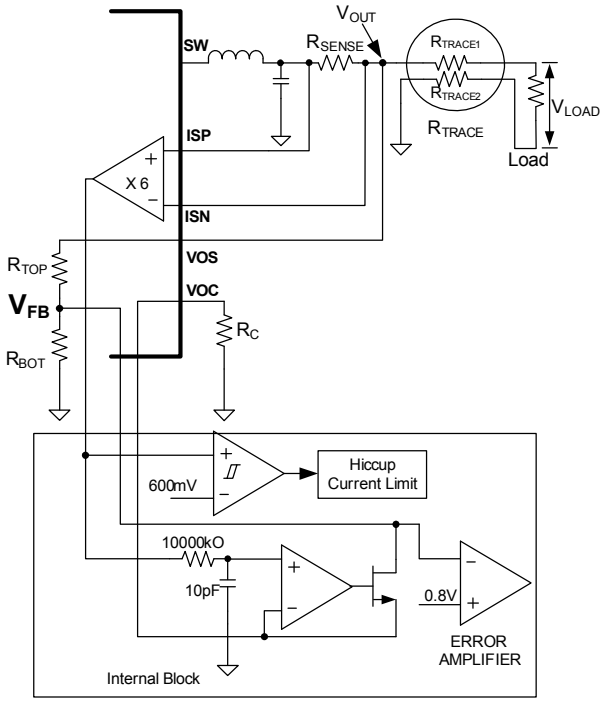


Figure 2—Output Line Drop Compensation

Selecting the Inductor

For most applications, use a 10μH to 47μH inductor with a DC current rating of at least 125% of the maximum load current. For best efficiency, select an inductor with a DC resistance less than 200mΩ. For most designs, the inductance value can be determined by.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (8)$$

Where ΔI_L is the inductor ripple current.

Choose inductor current ripple to equal approximately 30% of the maximum load current, 1.5A. Then maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (9)$$

Under light-load conditions below 100mA, use a larger inductor to improve efficiency.

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Selecting the Input Capacitor

An input capacitor reduces the surge current drawn from the input and any switching noise from the device. Chose a capacitor with a switching-frequency impedance less than the input source impedance. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. A capacitor value of 4.7μF will suffice for most applications.

Selecting the Output Capacitor

An output capacitor limits the output voltage and ensures regulator loop stability. Chose an output capacitor with a low impedance at the switching frequency; preferably ceramic with X5R or X7R dielectrics.

Setting the Current Limit

The inductor's DC resistance (DCR) sets the hiccup current limit. Use a sense resistor with high precision and accuracy for accurate sense measurement.

In Figure 3a, the output current limit is:

$$I_{OUT_L} = \frac{100mV}{DCR} \quad (10)$$

Where R_a and C_a form a low pass filter.

In Figure 3b, the output current limit is set as:

$$I_{OUT_L} = \frac{100mV}{R_{SENSE}} \quad (11)$$

Programming the Short Circuit Current Limit

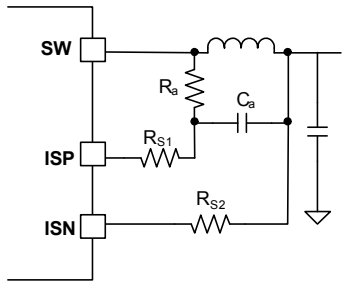
The hiccup current limit at output short condition can be programmed to be lower by external resisters (R_{S1}, R_{S2}, R_{S1}=R_{S2}), as shown in figure 4.

When output voltage is lower than 200mV, the current limit is described by:

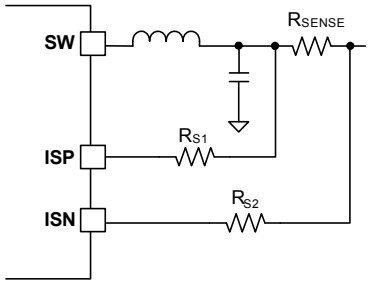
$$I_{OUT_SL} \times R_{SENSE} + 6.2\mu A \times R_{S1} = 100mV \quad (12)$$

The current limit at output short condition is:

$$I_{OUT_SL} = \frac{100mV - 6.2\mu A \times R_{S1}}{R_{SENSE}} \quad (13)$$



(a)



(b)

Figure 3—Current Sensing Methods

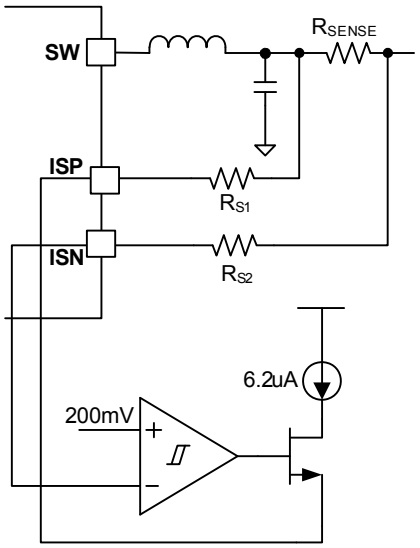


Figure 4—Short Circuit Current Limit

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PC Board Layout

The high frequency paths for VIN, SW and GND should be routed very close to the device with short, direct, and wide traces. Place the input capacitor as close as possible to the IN and GND pins. Place the external feedback resistors next to the FB pin. Keep the switching node SW short and away from the feedback network.

External Bootstrap Diode

An external bootstrap diode helps improve the efficiency of the regulator when the system has a 5V fixed input or the power supply generates a 5V output. The bootstrap diode can be low-cost, such as an IN4148 or a BAT54.

Add a diode for high duty-cycle operation (when $\frac{V_{OUT}}{V_{IN}}$ >65%).

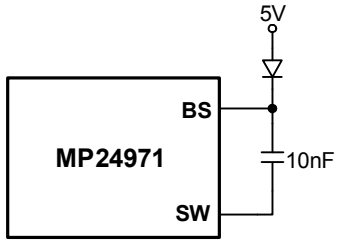


Figure 5—External Bootstrap Diode

Design Example

Below is a sample design that follows the application guidelines for the specifications below:

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	8 - 50	V
Output Voltage	V_{OUT}	5	V
Output Current Limit	I_{OUT-L}	1.5	A
Output OVP	V_{OVP}	6	V

Figure 6 shows the detailed application schematic. The Typical Performance Characteristics performance and circuit waveforms are all based on this design. For additional implentations, consult the Evaluation Board Data Sheets.

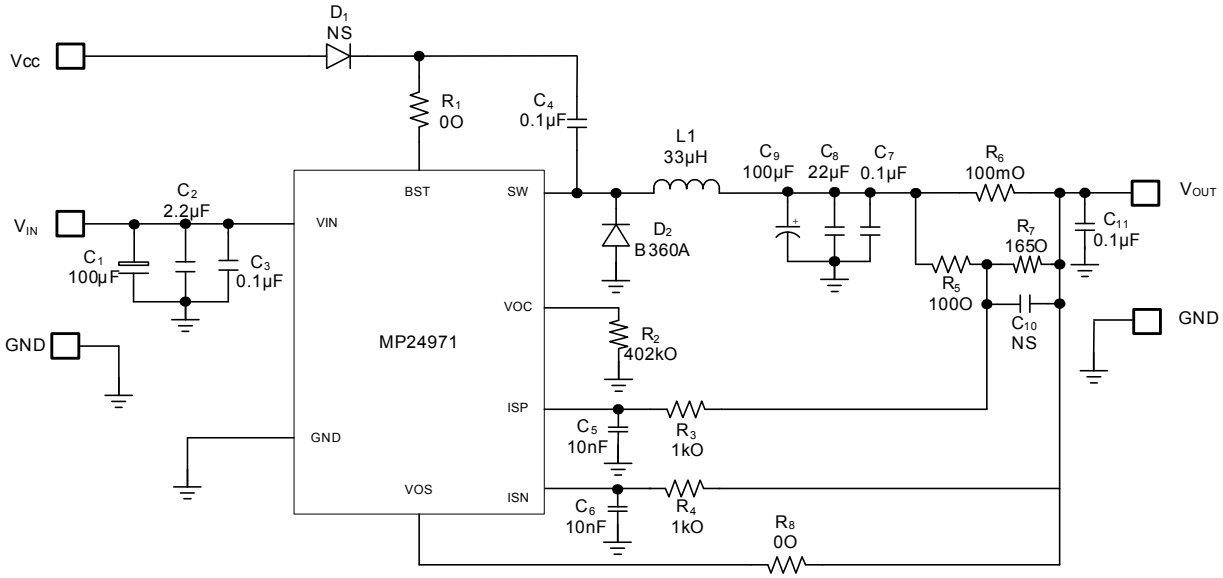
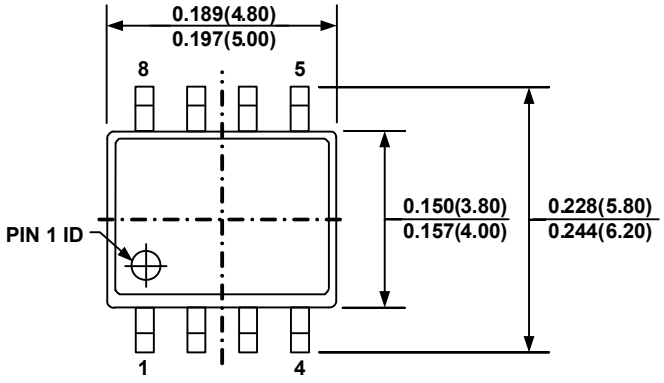


Figure 6—Detailed Sample Application Schematic

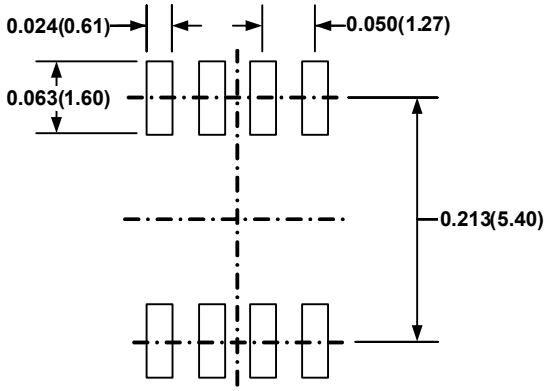
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PACKAGE INFORMATION

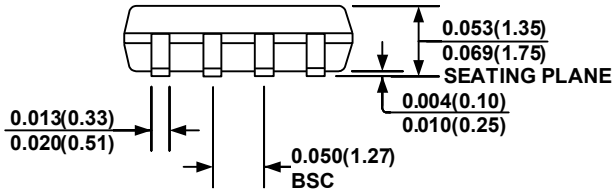
SOIC8



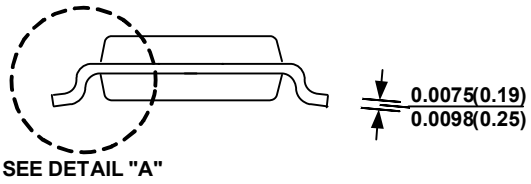
TOP VIEW



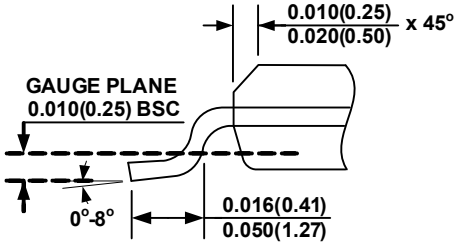
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

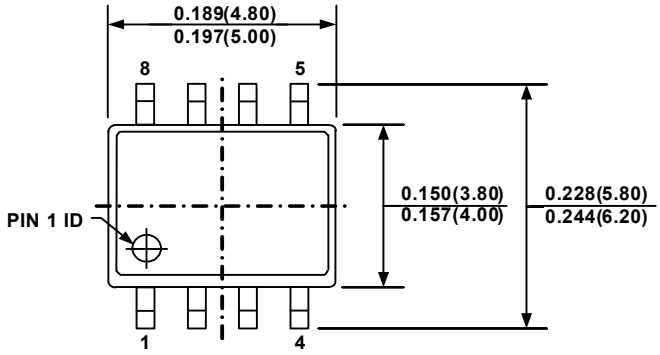
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE

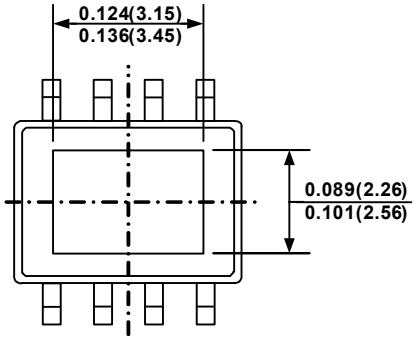
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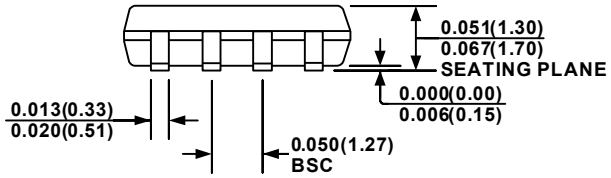
SOIC8E (EXPOSED PAD)



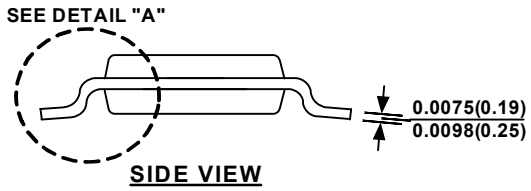
TOP VIEW



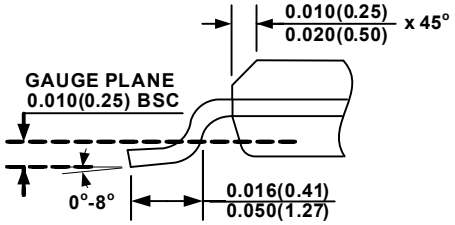
BOTTOM VIEW



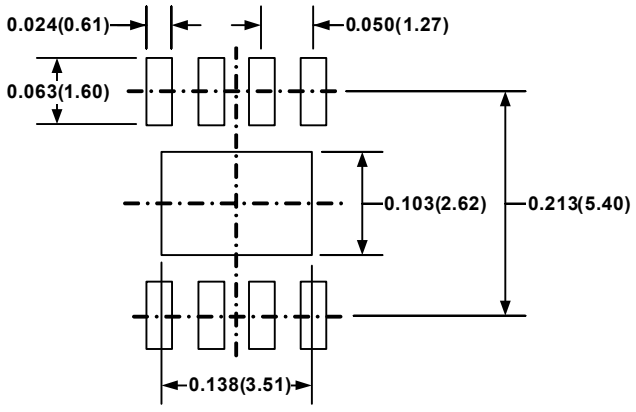
FRONT VIEW



SIDE VIEW



DETAIL "A"



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