MP2361

2A, 23V, 1.4MHz Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2361 is a monolithic step-down switch mode converter with a built-in internal power MOSFET. It achieves 2A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protections include cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws 20μA of supply current. Programmable soft-start minimizes the inrush supply current and the output overshoot at initial startup.

The MP2361 requires a minimum number of readily available standard external components.

FEATURES

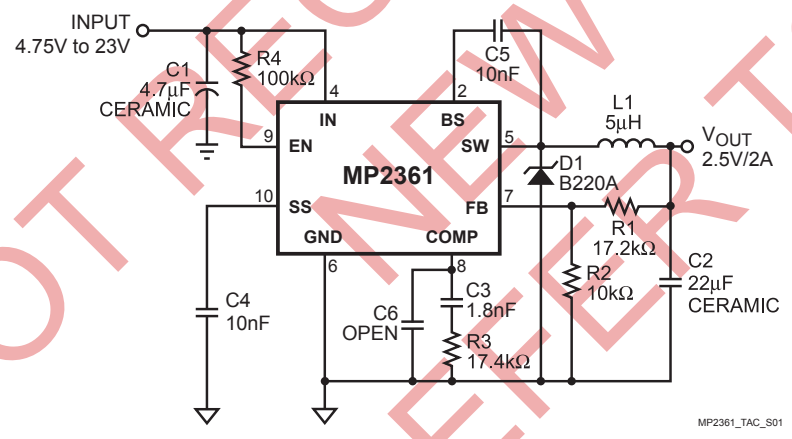
- 2A Output Current
- 0.18Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- 90% Efficiency
- 20μA Shutdown Mode
- Fixed 1.4MHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75V to 23V Operating Input Range
- Output Adjustable from 0.92V to 16V
- Programmable Under Voltage Lockout
- Available in QFN10, MSOP10, MSOP10E, and SOIC8 Packages

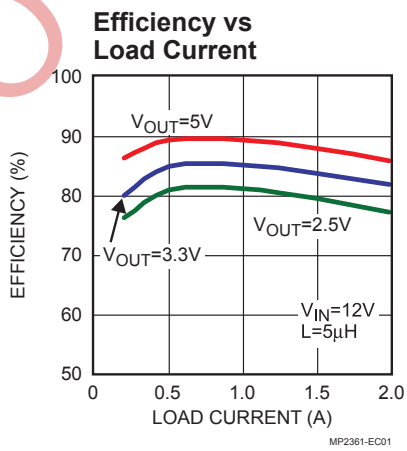
APPLICATIONS

- Distributed Power Systems
- Battery Charger
- DSL Modems
- Pre-Regulator for Linear Regulators

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2361DQ*	QFN10 (3mm x 3mm)	C8	–40°C to +85°C
MP2361DH**	MSOP10E	2361D	–40°C to +85°C
MP2361DK***	MSOP10	2361D	–40°C to +85°C
MP2361DS****	SOIC8	MP2361DS	–40°C to +85°C

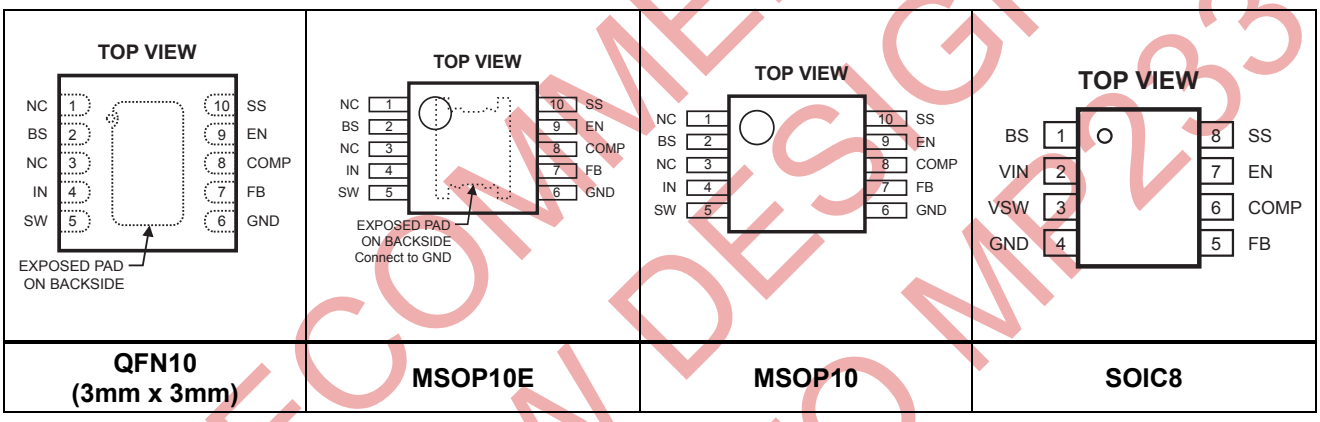
*For Tape & Reel, add suffix –Z (eg. MP2361DQ–Z);
For RoHS, compliant packaging, add suffix –LF (eg. MP2361DQ –LF–Z)

** For Tape & Reel, add suffix –Z (eg. MP2361DH–Z);
For RoHS, compliant packaging, add suffix –LF (eg. MP2361DH –LF–Z)

*** For Tape & Reel, add suffix –Z (eg. MP2361DK–Z);
For RoHS, compliant packaging, add suffix –LF (eg. MP2361DK –LF–Z)

**** For Tape & Reel, add suffix –Z (eg. MP2361DS–Z);
For RoHS, compliant packaging, add suffix –LF (eg. MP2361DS –LF–Z)

PACKAGE REFERENCE



QFN10 (3mm x 3mm)	MSOP10E	MSOP10	SOIC8

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}) 25V
Switch Node Voltage (V_{SW}) 26V
Bootstrap Voltage (V_{BS}) ..... V_{SW} + 6V
Feedback Voltage (V_{FB}) ..... –0.3V to +6V
Enable/UVLO Voltage (V_{EN}) ..... –0.3V to +6V
Comp Voltage (V_{COMP}) ..... –0.3V to +6V
Continuous Power Dissipation (T_A = +25°C)(2)
QFN10 (3mmx3mm) 2.5W
MSOP10 ..... 0.83W
MSOP10E 2.3W
SOIC8 ..... 1.38W
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (V_{IN}) ..... 4.75V to 23V
Operating Junct. Temp (T_J) .... –40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN10 (3mmx3mm)	50	12	°C/W
MSOP10	150	65	°C/W
MSOP10E	55	12	°C/W
SOIC8	90	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	0.892	0.920	0.948	V
Upper Switch On Resistance	$R_{DS(ON)1}$			0.18		Ω
Lower Switch On Resistance	$R_{DS(ON)2}$			10		Ω
Upper Switch Leakage		V_{EN} = 0V; V_{SW} = 0V		0	10	μA
Current Limit (5)			2.8	3.5		A
Current Sense Transconductance Output Current to Comp Pin Voltage	G_{CS}			1.95		A/V
Error Amplifier Voltage Gain	A_{VEA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10μA	630	930	1230	μA/V
Oscillator Frequency	f_S			1.4		MHz
Short Circuit Frequency		V_{FB} = 0V		210		kHz
Soft-Start Pin Equivalent Output Resistance				9		kΩ
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.8V		70		%
Minimum On Time	t_{ON}			100		ns
EN Shutdown Threshold Voltage	V_{EN}	I_{CC} > 100μA	0.7	1.0	1.3	V
Enable Pull Up Current	I_{EN}	V_{EN} = 0V		1.0		μA
EN UVLO Threshold Rising	V_{UVLO}	V_{EN} Rising	2.37	2.50	2.62	V
EN UVLO Threshold Hysteresis				210		mV
Supply Current (Shutdown)	I_{OFF}	V_{EN} ≤ 0.4V		20	36	μA
Supply Current (Quiescent)	I_{ON}	V_{EN} ≥ 3V		1.2	1.4	mA
Thermal Shutdown				160		°C

Note:

5) Equivalent output current = 1.5A ≥ 50% Duty Cycle
2.0A ≤ 50% Duty Cycle
Assumes ripple current = 30% of load current.
Slope compensation changes current limit above 40% duty cycle.

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PIN FUNCTIONS

QFN and MSOP Pin #	SOIC Pin #	Name	Description
1		NC	No Connect.
2	1	BS	Bootstrap (C5). This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to form a floating supply across the power switch driver. The voltage across C5 is about 5V and is supplied by the internal +5V supply when the SW pin voltage is low.
3		NC	No Connect.
4	2	IN	Supply Voltage. The MP2361 operates from a +4.75V to +23V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
5	3	SW	Switch. This connects the inductor to either IN through M1 or to GND through M2.
6	4	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
7	5	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV.
8	6	COMP	Compensation. This node is the output of the transconductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensation section for exact details.
9	7	EN	Enable/UVLO. A voltage greater than 2.62V enables operation. Leave EN unconnected for automatic startup. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from V_{IN} to GND. For complete low current shutdown it's the EN pin voltage needs to be less than 700mV.
10	8	SS	Soft-Start Pin. Connect SS to an external capacitor to program the soft-start. If unused, leave it open.

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OPERATION

The MP2361 is a current mode regulator. That is, the COMP pin voltage is proportional to the peak inductor current. At the beginning of a cycle: the upper transistor M1 is off; the lower transistor M2 is on (see Figure 1); the COMP pin voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 1.4MHz CLK signal sets the RS Flip-Flop. Its output turns off M2 and turns on M1 thus connecting the SW pin and inductor to the input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the Current Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the COMP pin voltage, the RS Flip-Flop is reset and the MP2361 reverts to its initial M1 off, M2 on state. If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.92V bandgap reference. The polarity is such that the FB pin voltage lower than 0.92V increases the COMP pin voltage. Since the COMP pin voltage is proportional to the peak inductor current an increase in its voltage increases current delivered to the output. The lower 10Ω switch ensures that the bootstrap capacitor voltage is charged during light load conditions. External Schottky Diode D1 carries the inductor current when M1 is off.

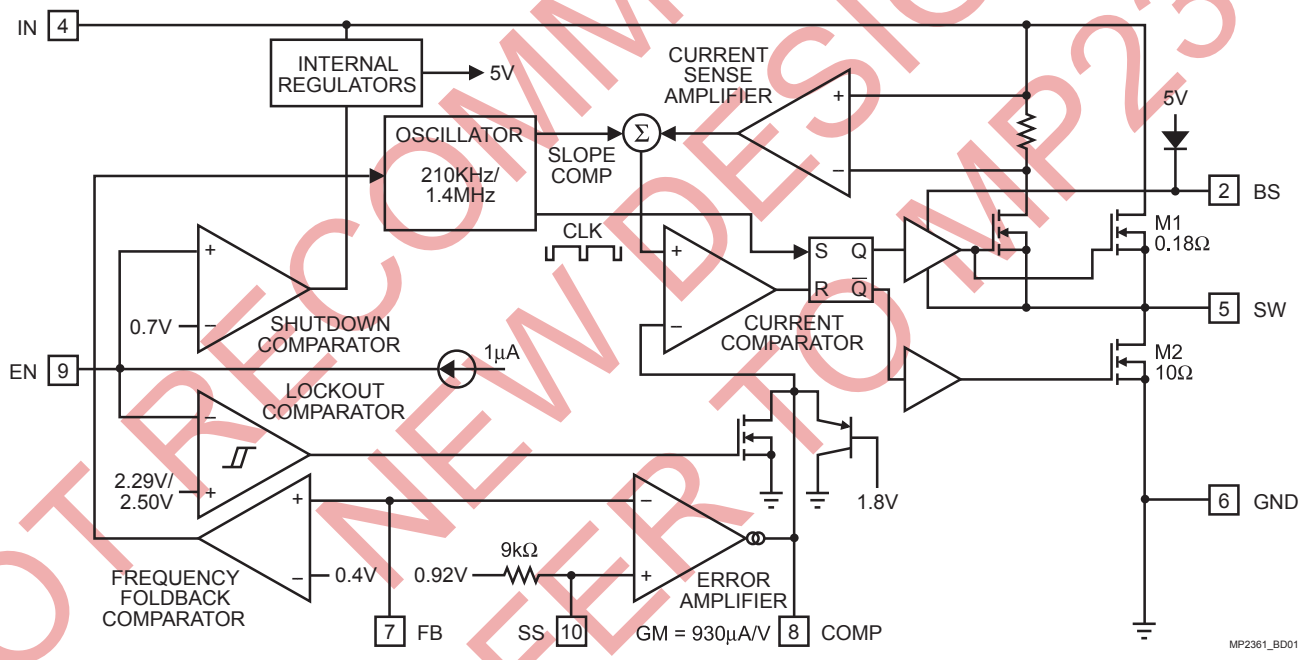


Figure 1—Functional Block Diagram

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.92 \times \frac{R1+R2}{R2}$$

Where V_{OUT} is the output voltage and V_{FB} is the feedback voltage.

A typical value for R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = 10.87 \times (V_{OUT} - 0.92)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 25.8kΩ.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where f_S is the switching frequency, ΔI_L is the peak-to-peak inductor ripple current and V_{IN} is the input voltage.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

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The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C2 is the output capacitance value.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2361 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

The MP2361 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where R_{LOAD} is the load resistor value, G_{CS} is the current sense transconductance and A_{VEA} is the error amplifier voltage gain.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

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In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system unstable. A good rule of thumb is to set the crossover frequency to below one-tenth of the switching frequency. To optimize the compensation components, the following procedure can be used:

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency, which is typically less than one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, to below one forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{2}{\pi \times R3 \times f_C}$$

Where R3 is the compensation resistor value.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure2

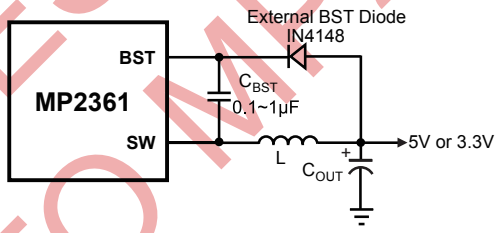


Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

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PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure3 for references (QFN10,MSOP10, MSOP10E).

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and schottky diode.
2) Keep the connection of schottky diode between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability. For single layer, do not solder exposed pad of the IC.

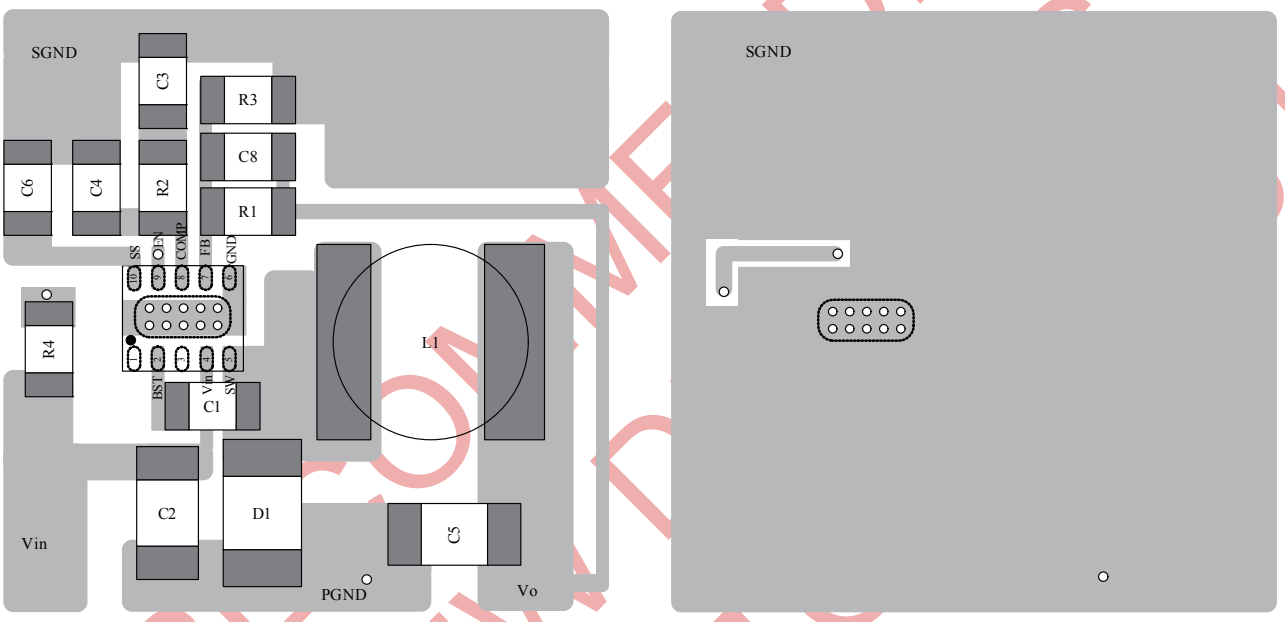


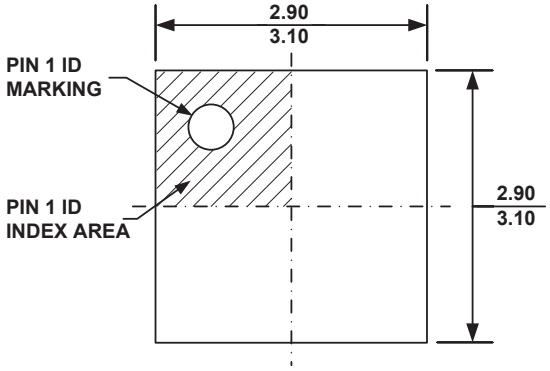
Figure3—PCB Layout

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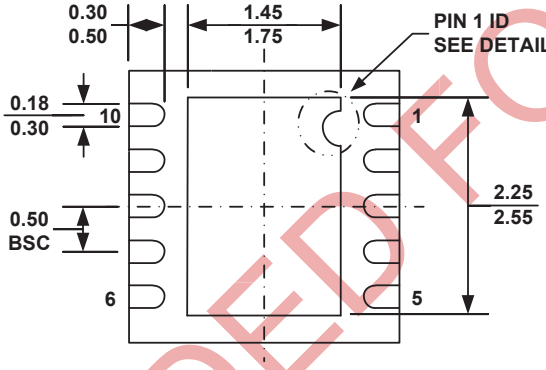
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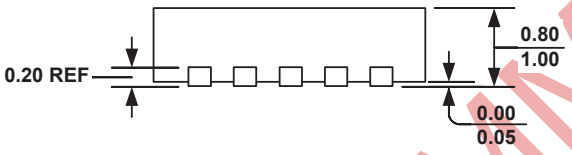
QFN10 (3mm x 3mm)



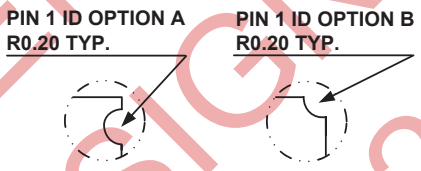
TOP VIEW



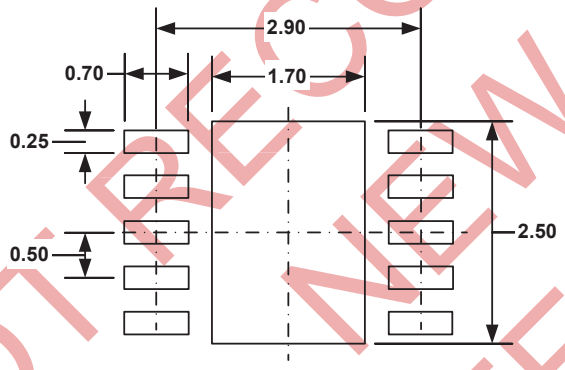
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

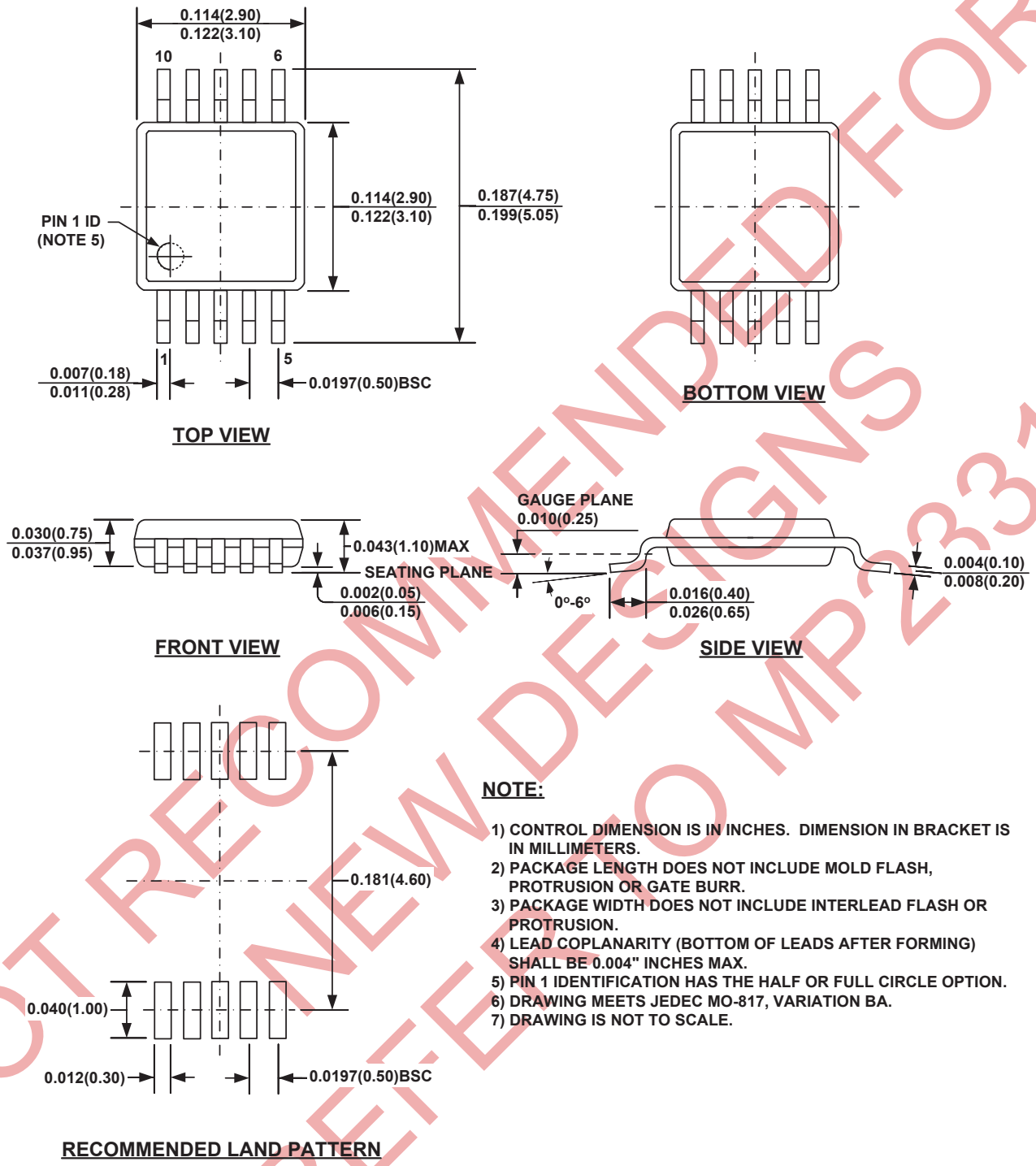
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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MSOP10



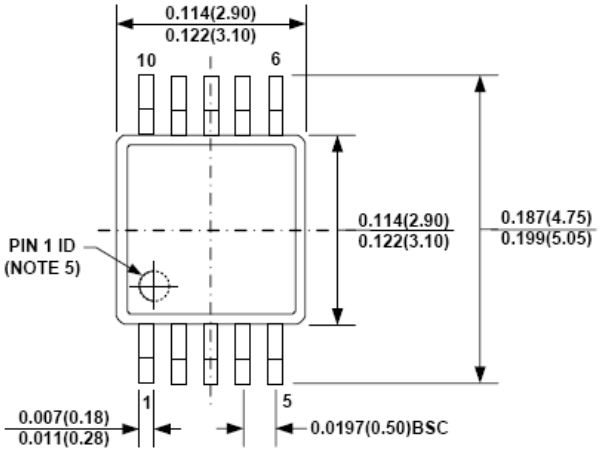
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

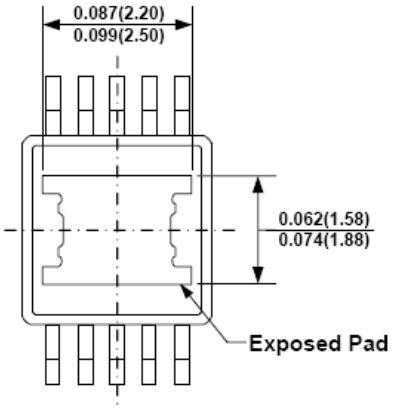
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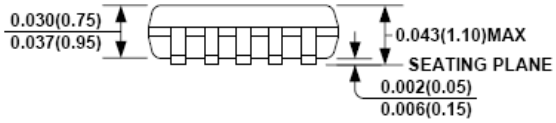
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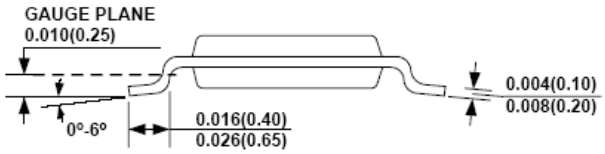
TOP VIEW



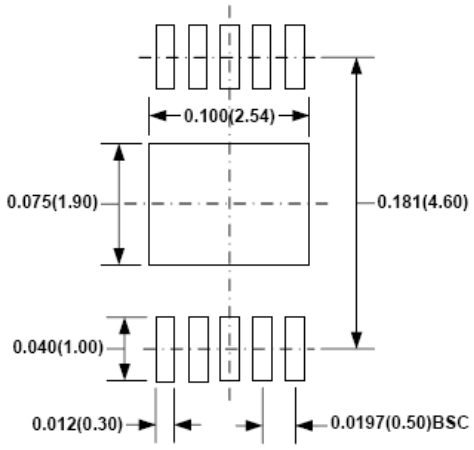
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



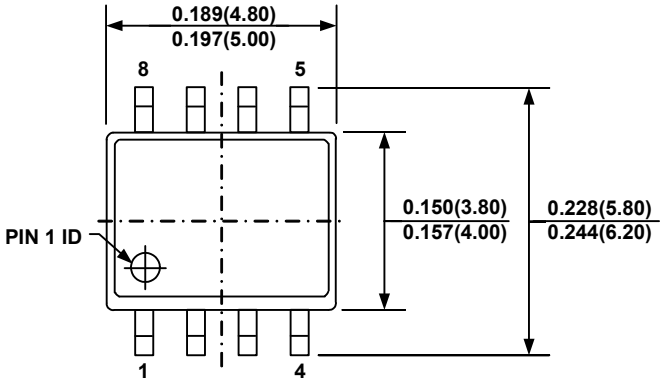
RECOMMENDED LAND PATTERN

NOTE:

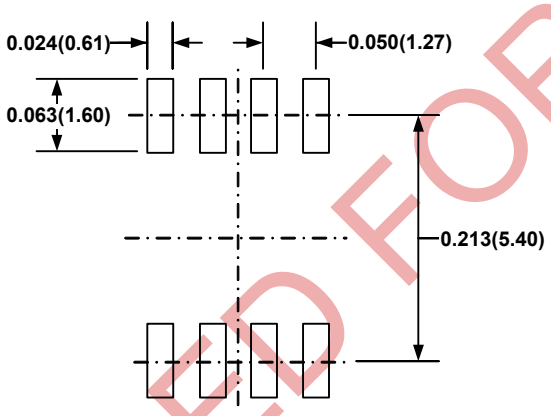
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION BA-T.
7) DRAWING IS NOT TO SCALE.

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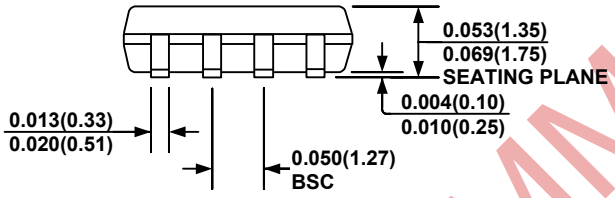
SOIC8



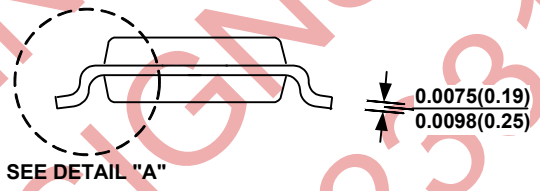
TOP VIEW



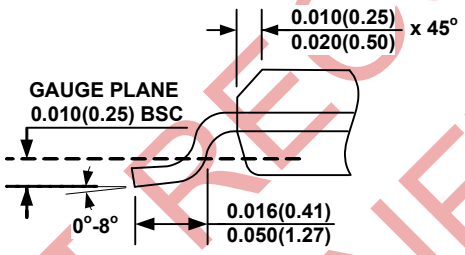
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2331H

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