MP2326

19V, 4A, 40µA I_Q, High-Efficiency Constant-On-Time (COT) Step-Down Converter in a 2mmx3mm QFN Package

The Future of Analog IC Technology

DESCRIPTION

The MP2326 is a fully integrated, high-efficiency, synchronous, step-down, switch-mode converter with only a 40µA quiescent current. This very compact device achieves a 4A continuous output current over a wide input-supply range with excellent load and line regulation, and it operates with high efficiency over a wide output current load range. It's optimized for battery-operated applications and applications requiring high light-load efficiency.

With constant-on-time (COT) control, the MP2326 provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include SCP, OCP, UVP, and thermal shutdown.

The MP2326 requires a minimal number of readily available, standard, external components with a space saving 2mmx3mm 14-pin QFN package.

FEATURES

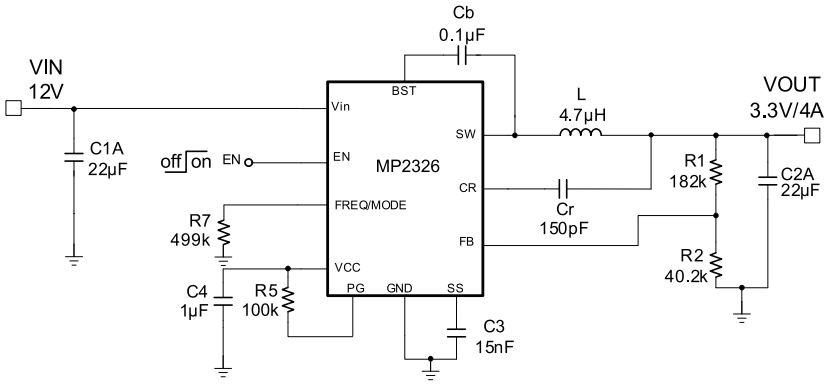
- 3.9V to 19V Operating Input Range
- 4A Output Current
- 40µA Quiescent Current
- Output Adjustable from 0.6V
- 90mΩ/30mΩ High Side/Low Side $R_{DS(ON)}$ for Internal Power MOSFETs
- Power Good Indicator
- Programmable Soft-Start Time
- Forced PWM or Auto PFM/PWM Mode Selectable
- Programmable Switching Frequency
- Thermal Shutdown
- Short-Circuit Protection: Hiccup Mode
- Available in a QFN-14 (2mmx3mm) Package

APPLICATIONS

- Tablet PCs
- Solid State Drives
- Gaming
- Battery-Operated Applications

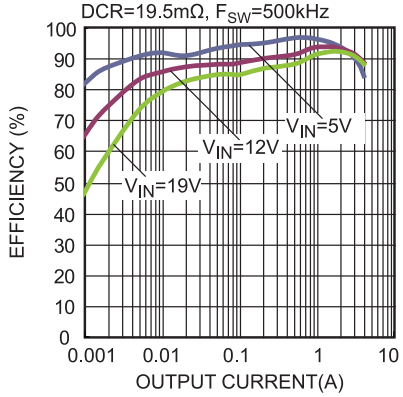
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TYPICAL APPLICATION



Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=3.3V, L=4.7µH, DCR=19.5mΩ, F_{SW}=500kHz



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2326GD	QFN-14 (2mmx3mm)	*See Below*

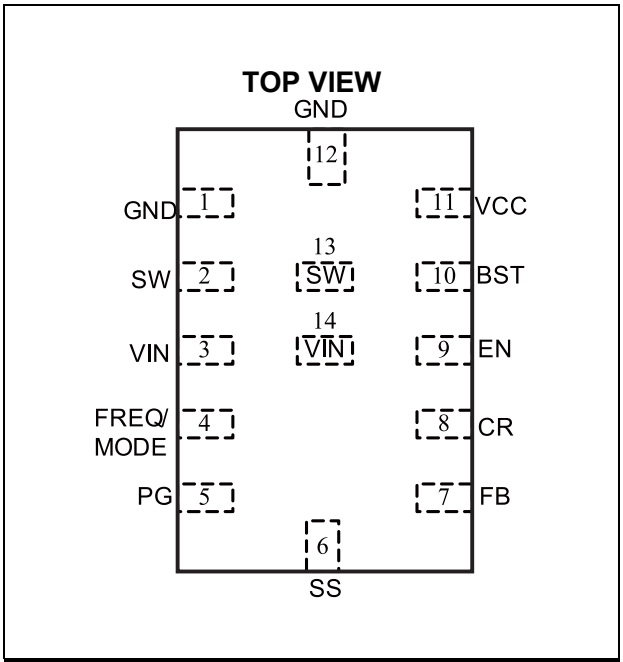
* For Tape & Reel, add suffix –Z (e.g. MP2326GD–Z);

TOP MARKING

AQV
YWW
LLL

AQV: Product Code of MP2326GD
Y: Year Code
WW: Week Code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... +21V
V_{SW} .. –0.3V (-5V<10ns) to V_{IN}+0.3V (23V<10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins ..... –0.3V to +6V(2)
Continuous Power Dissipation (3)
QFN-14 (2mmx3mm) 1.8W
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 3.9V to 19V
Output Voltage V_{OUT} ..... 0.6V to VIN*D_{MAX}(5)
Operating Junction Temp. ..... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-14 (2mmx3mm)	70	15 °C/W

Notes:

1) Exceeding these ratings may damage the device
2) Please refer to the “Enable Control” section on page 15 for the ABS MAX rating of EN.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) For details about the Dmax, see the “Application when Input Voltage is Close to Output Voltage” section on page 13 for more information.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J=-40°C to +125°C (7), typical value is tested at T_J=+25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0.1	1	μA
Supply current (quiescent)	I_Q	V_{EN} = 5V, T_J = 25°C, V_{FB} = 0.9V		40	55	μA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		3.5	3.7	3.9	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			200		mV
HS switch-on resistance	HS_{RDS-ON}			90		mΩ
LS switch-on resistance	LS_{RDS-ON}			30		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
High Side FET Current limit (8)	I_{LIMIT_HS}	Duty=10%, T_J = 25°C	5.5	7.5		A
Low Side FET Current limit	I_{LIMIT_LS}	Force PWM Mode, Sink Current		1.5		A
One-Shot on time(8)	T_{ON}	R_{FREQ}=180k from FREQ/MODE Pin to VIN		230		ns
Minimum on time(8)	T_{ON_min}			90		ns
Minimum off time	T_{OFF_min}			150		ns
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J=-40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft start current	I_{SS}		4	8	11	μA
EN Input High Voltage	V_{EN_H}		1.6			V
EN Input Low Voltage	V_{EN_L}				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
Power-good rising threshold	PG_{Vth-Hi}			0.9		V_{FB}
Power-good falling threshold	PG_{Vth-Lo}			0.85		V_{FB}
Power-good delay	PG_{Td}			140		μs
Power-good sink current capability	V_{PG}	Sink 1mA			0.4	V
Power-good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			50	nA
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD-HYS}			20		°C

Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by design and engineering sample characterization.

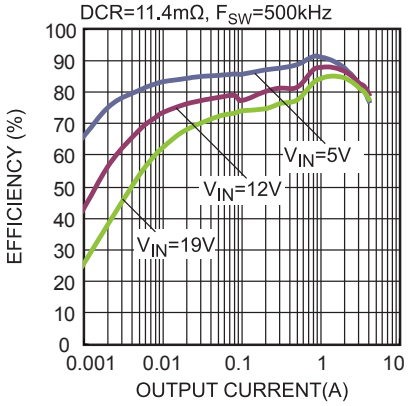
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TYPICAL PERFORMANCE CHARACTORISTICS

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=25°C, unless otherwise noted.

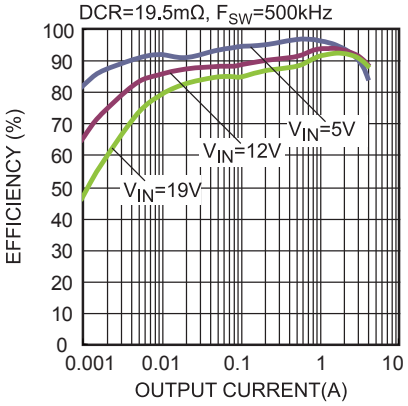
Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=1.2V, L=2.2µH, DCR=11.4mΩ, F_{SW}=500kHz



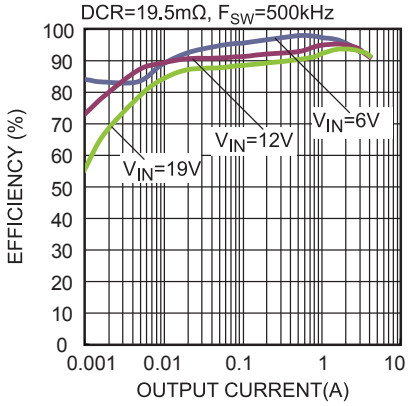
Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=3.3V, L=4.7µH, DCR=19.5mΩ, F_{SW}=500kHz



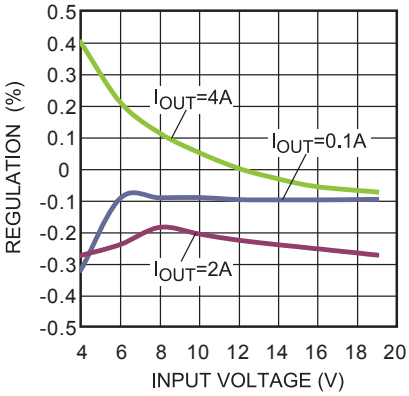
Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=5V, L=4.7µH, DCR=19.5mΩ, F_{SW}=500kHz



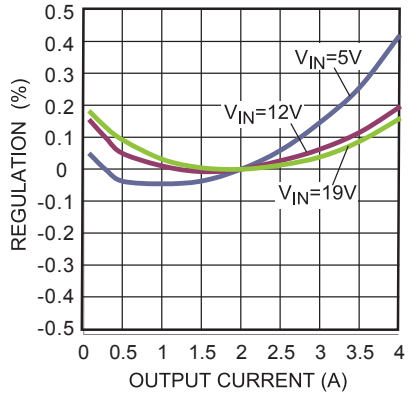
Line Regulation

V_{IN}=4V to 19V



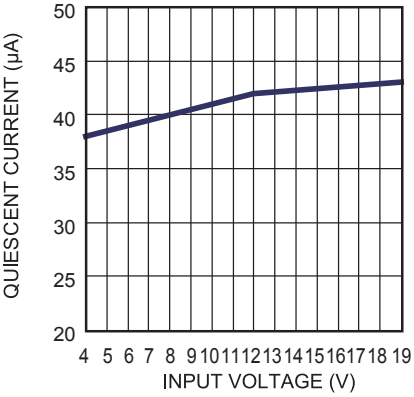
Load Regulation

I_{OUT}=0.1A to 4A



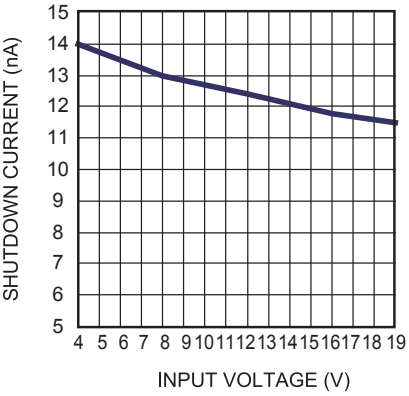
Quiescent Current vs. Input Voltage

V_{IN}=4 to 19V,V_{FB}=0.7V

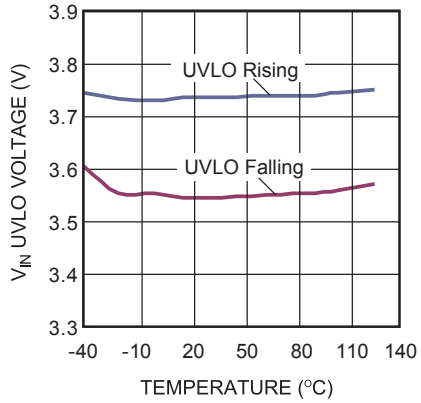


Shutdown Current vs. Supply voltage

V_{IN}=4 to19V,V_{EN}=0V

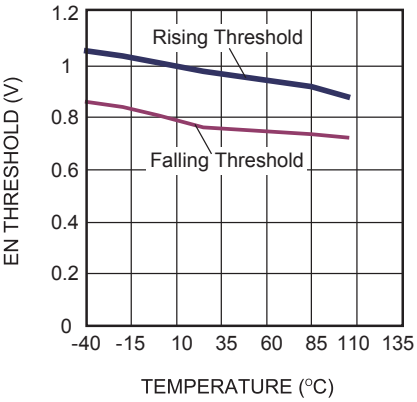


V_{IN} UVLO vs. Temperature



EN Rising Threshold vs. Temperature

V_{IN}=12V



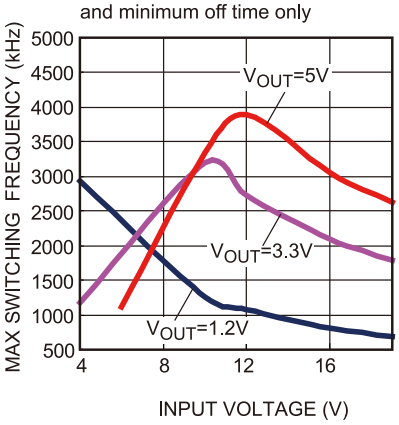
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TYPICAL PERFORMANCE CHARACTORISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=25°C, unless otherwise noted.

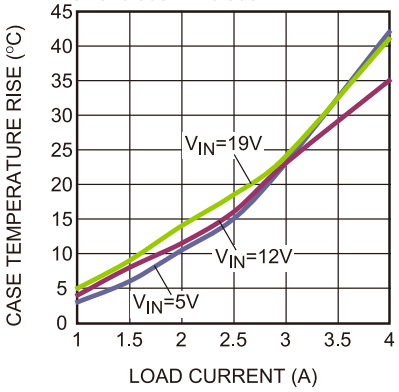
Max Frequency vs. Input Voltage

Consider the minimum on time and minimum off time only



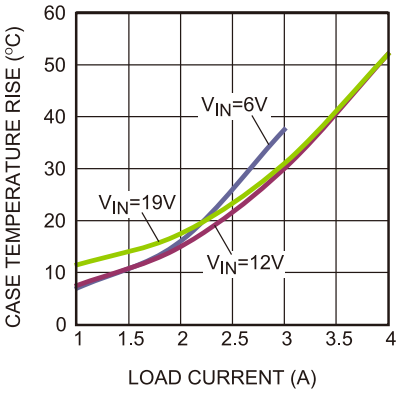
Case Temperature Rise vs. I_{OUT}

V_{OUT}=1.2V, I_{OUT}=1A to 4A, 4 Layers PCB, Size: 6.35cm X 6.35cm



Case Temperature Rise vs. I_{OUT}

V_{OUT}=5V, I_{OUT}=1A to 4A, 4 Layers PCB, Size: 6.35cm X 6.35cm

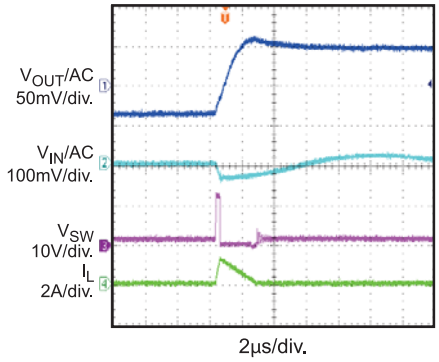


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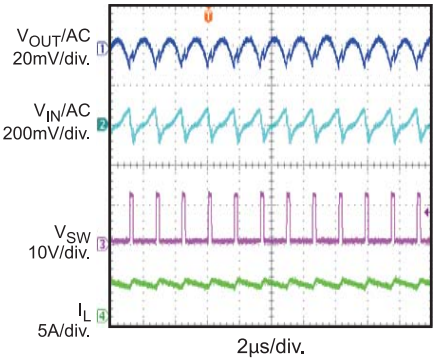
TYPICAL PERFORMANCE CHARACTORISTICS *(continued)*

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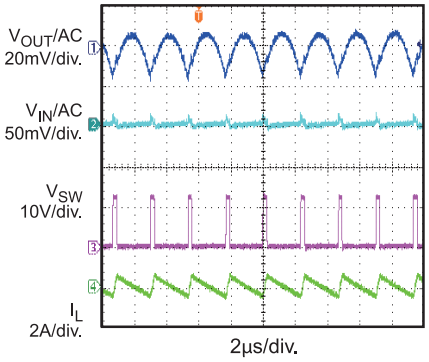
Input/Output Ripple
Auto PFM/PWM, I_{OUT}=0A



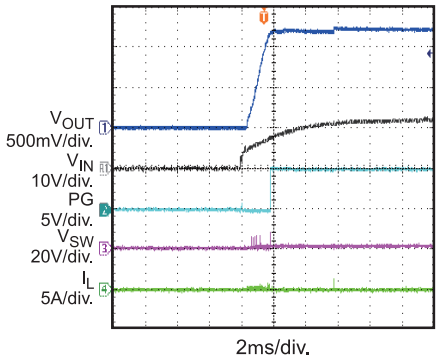
Input/Output Ripple
I_{OUT} = 4A



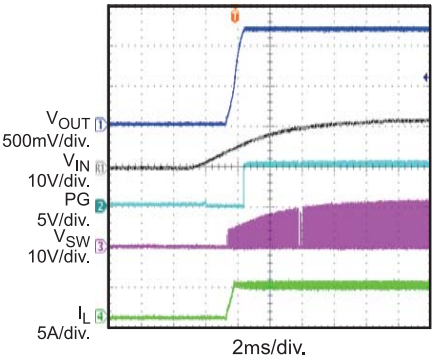
Input/Output Ripple
Forced PWM, I_{OUT}=0A



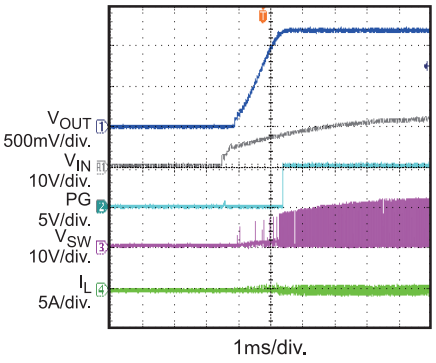
Start-Up through V_{IN}
Auto PFM/PWM, I_{OUT}=0A



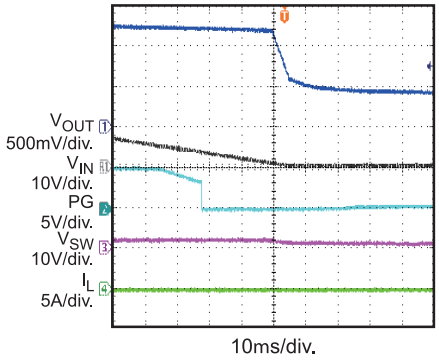
Start-Up through V_{IN}
I_{OUT} = 4A



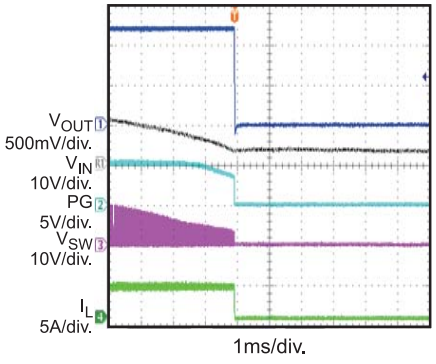
Start-Up through V_{IN}
Forced PWM, I_{OUT}=0A



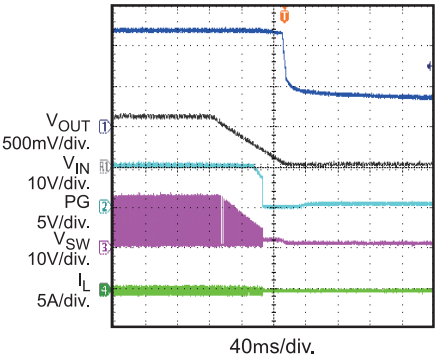
Shutdown through V_{IN}
Auto PFM/PWM, I_{OUT}=0A



Shutdown through V_{IN}
I_{OUT} = 4A



Shutdown through V_{IN}
Forced PWM, I_{OUT}=0A

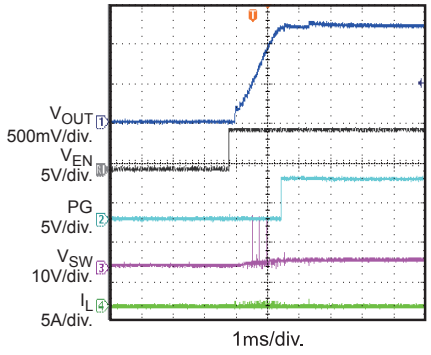


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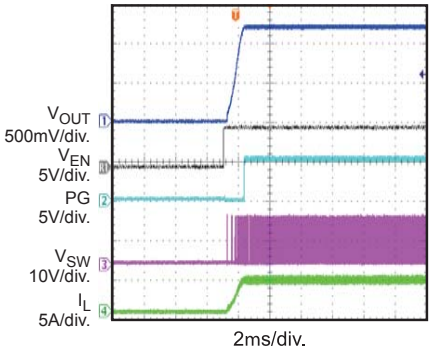
TYPICAL PERFORMANCE CHARACTORISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=25°C, unless otherwise noted.

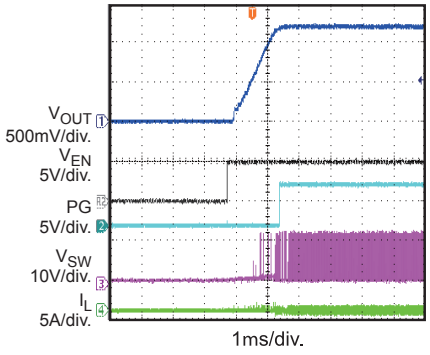
Start-Up through EN
Auto PFM/PWM, I_{OUT}=0A



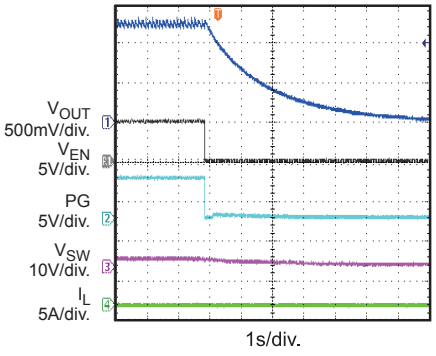
Start-Up through EN
I_{OUT} = 4A



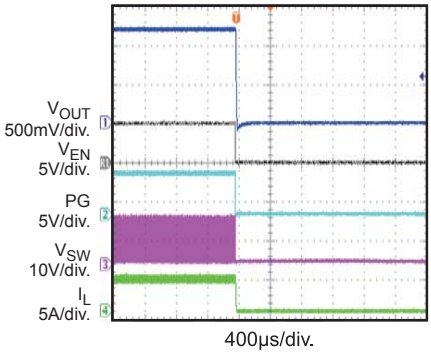
Start-Up through EN
Forced PWM, I_{OUT}=0A



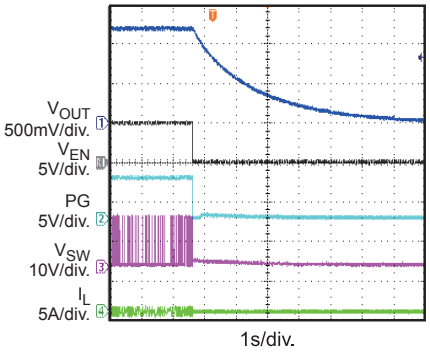
Shutdown through EN
Auto PFM/PWM, I_{OUT}=0A



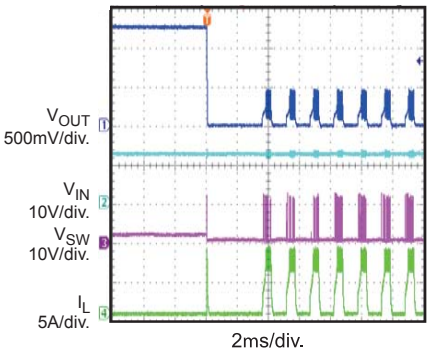
Shutdown through EN
I_{OUT} = 4A



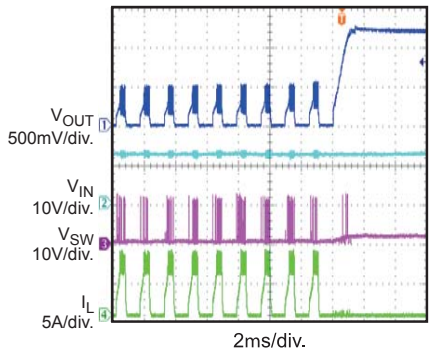
Shutdown through EN
Forced PWM, I_{OUT}=0A



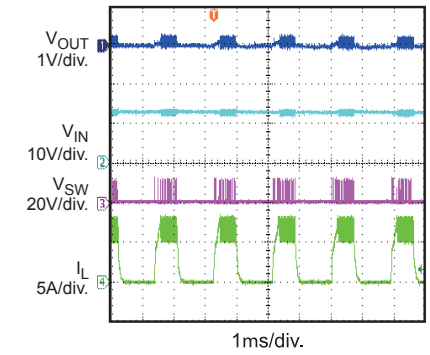
Short-Circuit Entry
I_{OUT}=0A



Short-Circuit Recovery
I_{OUT} = 0A



Short-Circuit Steady State
I_{OUT} = 0A



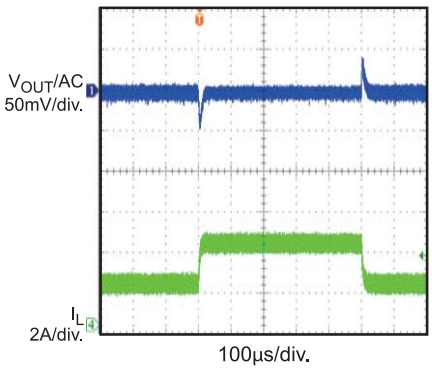
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TYPICAL PERFORMANCE CHARACTORISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=25°C, unless otherwise noted.

Load Transient

I_{OUT}=2A to 4A, 0.8A/µs



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PIN FUNCTIONS

Package Pin #	Name	Description
1,12	GND	System Ground. GND is the reference ground for the regulated output voltage, and it requires special consideration during PCB layout (see the recommended “PCB Layout Guidelines” section on page 19).
2, 13	SW	Switch Output. Connect SW using wide PCB traces.
3, 14	VIN	Supply Voltage. The MP2326 operates from a +3.9V to +19V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
4	FREQ/MODE	Frequency Set during CCM Operation. Connect a resistor to VIN to set the switching frequency; the part works in forced PWM mode. Connect a resistor to GND to set the switching frequency; the part works in auto PFM/PWM mode. Do NOT float FREQ/MODE.
5	PG	Power Good Output. The output of PG is an open drain that goes high if the output voltage is higher than 90% of the nominal voltage. There is a 40µs delay when FB ≥ 90% and when PG goes high. Note: If PG is pulled up to an external voltage, PG will not de-assert (Logic low) if EN is low or if input power is off. It is recommended that PG is pulled up to VCC pin and in this case PG will de-assert (Logic low) when EN is Low or if input power is off. Refer to Applications section for additional details.
6	SS	Soft-Start. Connect a capacitor across SS and GND to set the soft-start time to avoid a start-up inrush current.
7	FB	Feedback. FB sets the output voltage when connected to the tap of an external resistor divider that is connected between the output and GND.
8	CR	Internal Ramp Adjust. Connect a capacitor from VOUT to CR to adjust the internal ramp amplitude. This can be used to improve the transient performance.
9	EN	Enable/Disable Control. EN = 1 to enable the MP2326. For automatic start-up, connect EN to VIN with a pull-up resistor.
10	BST	Bootstrap. BST requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver.
11	VCC	Internal Bias Supply. Internal 5V LDO output. Decouple with a 1µF ceramic capacitor as close to VCC as possible.

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FUNCTIONAL BLOCK DIAGRAM

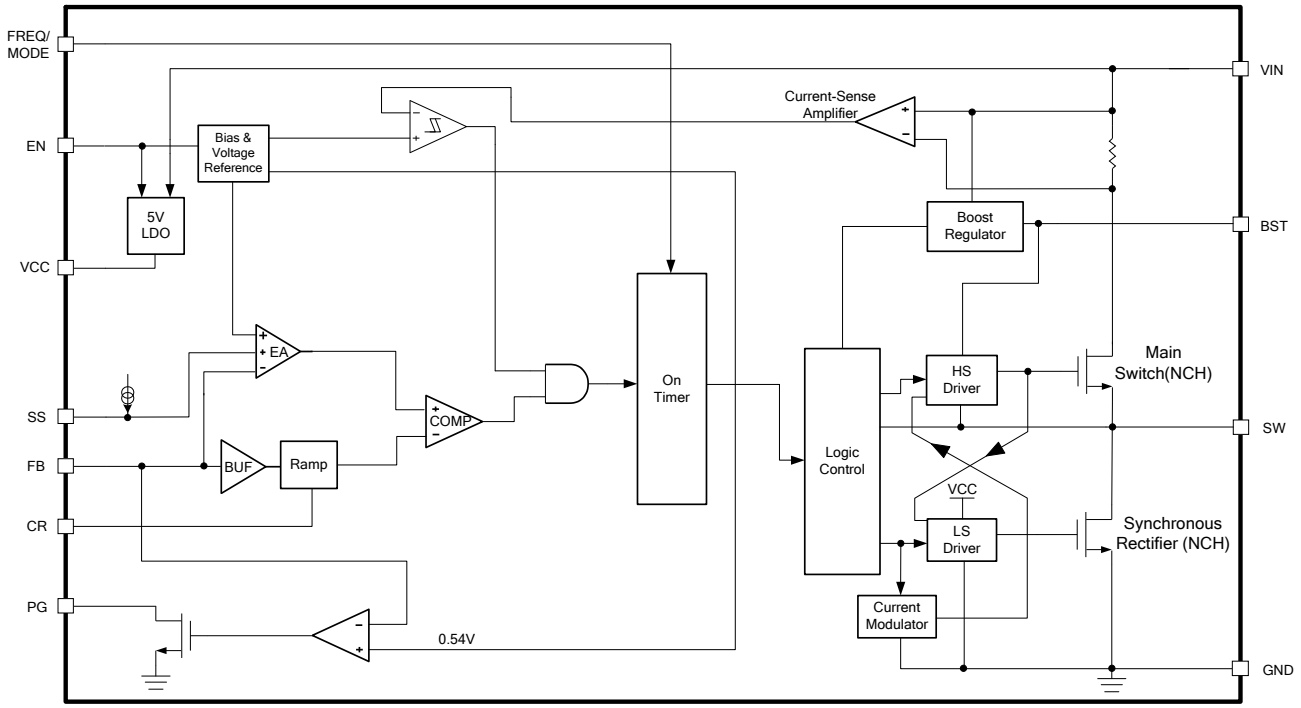


Figure 1: Functional Block Diagram

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OPERATION

PWM Operation

The MP2326 is a fully integrated, synchronous, rectified, step-down, switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop compensation. Fig. 2 shows the MP2326s simplified ramp compensation block. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the ramp voltage (V_{Ramp}) is lower than the error amplifier output voltage (V_{EAO}), which indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the HS-FET turn-on timer (T_{ON}).
After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on during the HS-FETs off state to minimize the conduction loss.

Shoot-through occurs when both the HS-FET and the LS-FET are turned on at the same time, causing a dead short between the input and GND. Shoot-through reduces efficiency dramatically. The MP2326 avoids shoot-through by internally generating a dead-time (DT) between the HS-FET off-time and the LS-FET on-time, and the LS-FET off-time and the HS-FET on-time. Depending on the output current, the device enters either heavy-load operation or light-load operation.

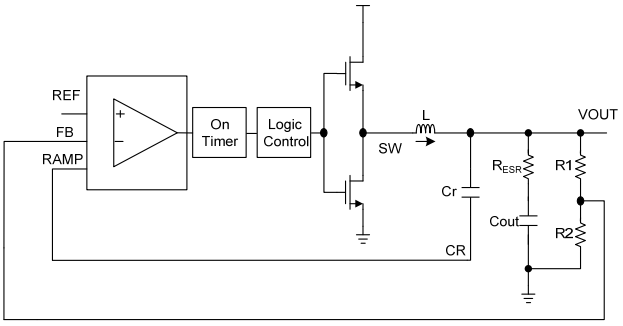


Figure 2: Simplified Ramp Compensation Block

MODE Selection

Connecting a resistor (R6) from FREQ/MODE to VIN sets the switching frequency (see Fig. 3). Meanwhile, the part works in forced PWM mode.

Connect a resistor (R7) from FREQ/MODE to GND to set the switching frequency. Meanwhile, the part works in auto PFM/PWM mode.

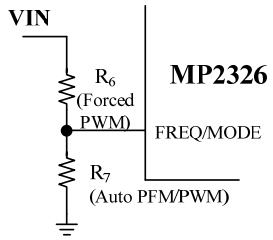


Figure 3: Mode Selection

Switching Frequency

MP2326 uses constant-on-time (COT) control; there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the frequency resistor. The duty ratio is kept at V_{OUT}/V_{IN}, and the switching frequency is fairly constant over the input voltage range. The approximate typical switching frequency can be determined with the following equation:

$$F_{SW}(kHz) = \frac{10^6}{T_{on}(ns) \times \frac{V_{IN}(V)}{V_{OUT}(V)}} \quad (1)$$

T_{ON} will be slightly different at forced PWM mode and auto PFM/PWM mode. The approximate typical T_{ON} formula is shown below:

Forced PWM mode:

$$T_{ON_PWM} = \frac{14.5 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} + T_{DELAY_PWM}(ns) \quad (2)$$

Auto PFM/PWM mode:

$$T_{ON_PFM} = \frac{13 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} + T_{DELAY_PFM}(ns) \quad (3)$$

Where T_{DELAY_PWM} and T_{DELAY_PFM} represent the comparator delay. The typical value equals approximately 15ns and 10ns, respectively.

When the part enters CCM mode, the duty ratio changes slightly from light load to full load due to power loss. This causes the frequency to change slightly from light load to full load even in CCM mode.

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Because of the minimum on time and minimum off time, the switching frequency is limited. The maximum frequency can be calculated by the following equations. Choose the lowest value between the two as the maximum frequency:

$$F_{SW\text{-}max}(KHz) = \frac{10^6}{T_{on\text{-}min}(ns) \times \frac{V_{IN}(V)}{V_{OUT}(V)}} \quad (4)$$

$$F_{SW\text{-}max}(KHz) = \frac{(V_{IN}(V) - V_{OUT}(V)) \times 10^6}{T_{off\text{-}min}(ns) \times V_{IN}(V)} \quad (5)$$

Where the $T_{on\text{-}min}$ typical value is 90ns and the $T_{off\text{-}min}$ typical value is 150ns. For example, if V_{IN}=12V and V_{OUT}=1.2V, the maximum frequency that can be set is about 1.1MHz. The MP2326 is optimized to operate at a high switching frequency with high efficiency. A high switching frequency makes it possible to use small-sized LC filter components to save system PCB space.

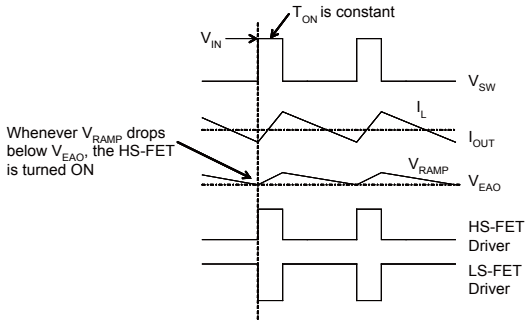


Figure 4: Forced PWM Operation

When the MP2326 works in forced PWM, the MP2326 enters CCM where the HS-FET and LS-FET repeat the on/off operation (even if the inductor current goes to zero or negative value). The switching frequency (F_{SW}) is fairly constant. Fig. 4 shows the timing diagram during forced PWM operation.

Light-Load Operation

In auto PFM/PWM mode (during light-load operation), the MP2326 reduces automatically the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). This causes the output capacitors to discharge slowly to GND through the LS-FET, R1, and R2.

This operation greatly improves device efficiency when the output current is low (see Fig. 5).

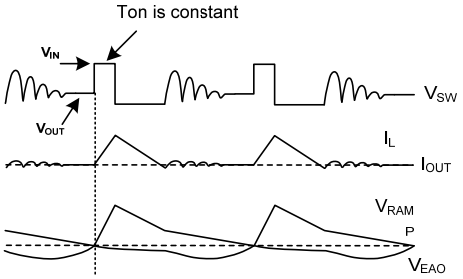


Figure 5: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period in which the current modulator regulates becomes shorter, causing the HS-FET to turn on more frequently. In turn, the switching frequency increases. The output current reaches the critical level when the current modulator time is zero. The output current can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (6)$$

The device reverts to PWM mode once the output current exceeds the critical level. Once in PWM mode, the switching frequency stays fairly constant over the output-current range.

Application when Input Voltage is Close to Output Voltage

MP2326 extends the on time when the output voltage looses regulation (when the input voltage is close to the output voltage). The switching frequency drops correspondingly in order to achieve a larger duty cycle to keep the output regulated. If V_{IN} is very close to V_{OUT}, the T_{ON} extension circuit forces MP2326 into PWM mode with a higher than expected frequency. Increasing V_{IN} to a certain level causes the part to exit PWM mode (see Fig. 6). The MP2326 works at auto PFM/PWM mode when V_{IN} is above the curve. If auto PFM/PWM mode is required at the input voltage below the curve, use Enable start-up instead of the input voltage start-up.

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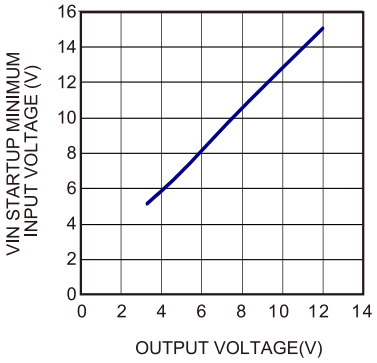


Figure 6: V_{IN} Start-Up Min V_{IN} vs. V_{OUT} to Guarantee the Auto PFM/PWM Mode Works Efficiently

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, Cb, L1, and C2A (see Fig. 7). If (V_{IN}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across Cb.

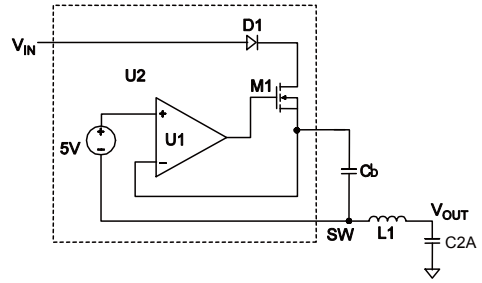


Figure 7: Bootstrap Charging Circuit

Ramp with Small ESR Output Capacitor

When the output capacitors are ceramic, the ESR ripple is not high enough to stabilize the system, so the external ramp compensation is needed.

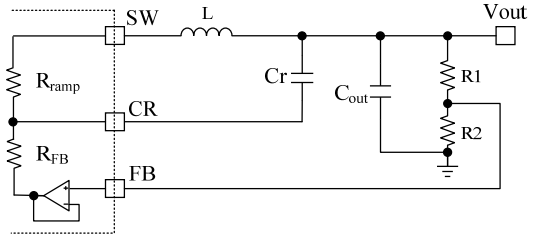


Figure 8: Simplified External Ramp Circuit in PWM Mode with Small ESR Cap

Figure 8 shows a simplified external ramp compensation for PWM mode. Chose the external ramp (C_r)to meet the following condition:

$$\frac{1}{2\pi \times F_{sw} \times C_r} < \frac{1}{5} R_{FB} \quad (7)$$

Where R_{FB} is set to 90k internally. Then:

$$I_{Rramp} = I_{Cr} + I_{RFB} \approx I_{Cr} \quad (8)$$

The V_{ramp} on the V_{CR} can be estimated as follows:

$$V_{ramp} = \frac{V_{in} - V_{out}}{R_{ramp} \times C_r} \times T_{on} \quad (9)$$

Where, R_{ramp} is set to 900k internally.

As can be seen from equation 9, if there is instability in PWM mode, C_r can be reduced. If C_r cannot be reduced further (due to limitations from equation 7), add an external resistor between SW and CR to reduce the equivalent R_{ramp}. Typically, set V_{ramp} to about 20-40mV for stable PWM operation.

Table 1 below shows the recommended C_r values for different output voltages. The recommended C_r values in Table 1 are based on a 500kHz switching frequency, selected output inductor, and 22µF output capacitors.

Table 1: C_r Selection for Common Output Voltages

V_{OUT}(V)	L(µH)	Cr(pF)	
		V_{IN}=12V	V_{IN}=5V
1.0	2.2	82	82
1.2	2.2	100	100
1.5	3.3	120	82
1.8	3.3	120	56
2.5	3.3	150	56
3.3	4.7	150	56
5	4.7	100	56(8)

Note:

9) When VOUT=5V, VIN should be higher than 6V.

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The C_r value may need to change with a different input voltage, output voltage, output inductor, output capacitor, and frequency set. If the design spec. is not the same as the specs. in Table 1, the C_r value must be adjusted accordingly. Use equation 9 as a design guide.

In skip mode, the stability is determined mainly by the ripple of V_{EAO}. A reasonable V_{ramp} chosen in PWM operation is generally acceptable for skip mode.

Soft-Start (SS)

MP2326 employs a soft-start (SS) mechanism to ensure smooth output ramping during power-up. When EN goes high, an internal current source (8μA) charges up the SS capacitor. The SS capacitor voltage transfers over to the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once SS voltage rises above V_{REF}, it continues to ramp up until the REF voltage takes over. At this point, the soft-start is complete and the device enters steady-state operation.

The SS capacitor value can be determined as follows:

$$C_{ss}(nF) = \frac{T_{ss}(ms) \times I_{ss}(uA)}{V_{REF}(V)} \quad (10)$$

If the output capacitance has a large value, setting too short of a SS time is not recommended. Otherwise, it's easy to hit the current limit during SS. A minimum value of 4.7nF is recommended if the output capacitance is larger than 330μF.

Pre-Bias Start-Up

The MP2326 has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged; the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at the FB, the part starts to operate.

Power Good (PG)

PG is an open-drain output. PG requires a pull-up resistor (eg. 100k). PG is pulled to GND before SS is ready. After FB voltage reaches 90% of V_{REF}, PG is pulled high after a 40μs delay. When the FB voltage drops below 85% of V_{REF}, PG is pulled low.

Note: If PG is pulled up to an external voltage, PG will not de-assert (Logic low) if EN is low or if Vin < 0.8V (typ). If PG is pulled up to the VCC pin, PG will de-assert (Logic low) if either EN is Low or if Vin < 0.8V (typ). If connecting two or more PG together, please refer to Application section.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP2326 has cycle-by-cycle over-current limit control. During the HS-FET on state, the inductor current is monitored. When the sensed inductor current hits the peak current limit, the HS limit comparator (see Fig. 1) is triggered, the device enters over-current protection mode immediately, and then turns off the HS-FET and turns on the LS-FET. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (50% below the reference, typically). Once UV is triggered, the MP2326 enters hiccup mode to re-start the part periodically.

During over-current protection, the device tries to recover from the over-current fault with hiccup mode. The chip disables the output power stage, discharges the soft-start cap, and then automatically tries to soft-start again. If the over-current condition still holds after the soft-start ends, the device repeats this operation cycle until the over-current condition disappears. Then the output rises back to regulation level. The OCP is non-latch protection.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 6.5V series-Zener-diode. Connect the EN input through a pull-up resistor to the voltage on V_{IN}. The pull-up resistance needs to be large enough to limit the EN current to less than100μA. For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the

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amplitude of the voltage to less than 6V to prevent damage to the Zener diode.

UVLO Protection

MP2326 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP2326 powers up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown (TSD)

The MP2326 employs thermal shutdown by monitoring internally the junction temperature of the IC. If the junction temperature exceeds the threshold value (150ºC, typically), the converter shuts off. This is non-latch protection. There is about 20ºC hysteresis. Once the junction temperature drops below 130ºC, it initiates the start-up.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably; a small value for R2 will lead to considerable quiescent current loss while too large of a value for R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ to 100kΩ for R2. Typically, set the current through R2 to create a good balance between system stability and no-load loss. Then R1 is determined as follows:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (11)$$

Where V_{REF} is 0.6V, typically.
The feedback circuit is shown in Fig. 9.

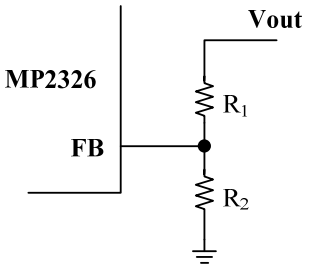


Figure 9: Feedback Network

Table 2 lists the recommended resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages(9)

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
1.0	27	40.2
1.2	40.2	40.2
1.5	60.4	40.2
1.8	80.6	40.2
2.5	127	40.2
3.3	182	40.2
5	294	40.2

Notes:
10) The feedback resistors in table 2 are optimized for a 500kHz switching frequency. The detailed schematics are shown in the "Typical Application Circuits" section.

Setting the Frequency

Refer to the "Mode Selection" section. Set the forced PWM mode switching frequency by connecting a resistor (R6) from VIN to FREQ/MODE, leaving R7 NS (see Fig.10) . R6 is determined as follows:

$$R6(k\Omega) = \frac{\left[\frac{Vo \times 10^6}{F_{SW}(kHz) \times V_{IN}} - T_{Delay_PWM}(ns)\right] \cdot (V_{IN} - 0.4)}{14.5} \quad (12)$$

Where T_{Delay_PWM} is about 15ns.

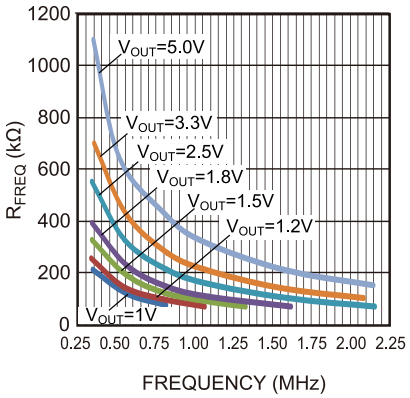


Figure 10: R6 vs. Forced PWM Mode Switching Frequency

Set the auto PFM/PWM mode switching frequency by connecting a resistor (R7) from FREQ/MODE to ground, leaving R6 NS (see Fig.11). R7 is determined as follows:

$$R7(k\Omega) = \frac{\left[\frac{Vo \times 10^6}{F_{SW}(kHz) \times V_{IN}} - T_{Delay_PFM}(ns)\right] \cdot (V_{IN} - 0.4)}{13} \quad (13)$$

Where T_{Delay_PFM} is about 10ns.

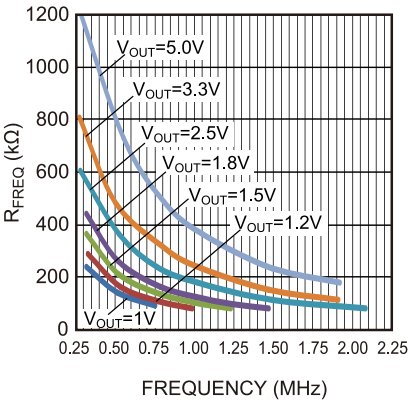


Figure 11: R7 vs. Auto PFM/PWM Mode Switching Frequency

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Equations 12 and 13 are the typical switching frequency calculation formulas. The actual frequency will change a little at different load currents and with different input voltages.

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current, which results in lower output-ripple voltage. However, a larger value inductor will have a larger physical footprint, a higher series resistance, and/or a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current. Make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (16)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (17)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input-voltage ripple of the converter. If there is an input-voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input-voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (19)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output-voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (20)$$

If using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output-voltage ripple is caused mainly by the capacitance. For simplification, the output-voltage ripple can be estimated as follows:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (21)$$

The output-voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through the capacitor Cr.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

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$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (22)$$

In addition to considering the output ripple, choosing a larger output capacitor can achieve improved load transient response. However, the maximum output capacitor limitation should be considered in design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (23)$$

Where, I_{LIM_AVG} is the average start-up current during the soft-start period. T_{ss} is the soft-start time.

PG Pull-Up

It is recommended that PG is pulled up to VCC for proper operation. If PG is pulled up to external voltage or if connecting two or more PG together, connect a diode from PG to EN as shown in Fig.12 and Fig.13. In this case PG will de-assert low when EN signal is low. But PG will not de-assert low when input power is off and EN signal is high condition.

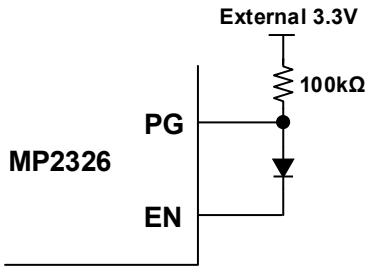


Figure 12: PG Pull up to external power supply with enable control signal --- Single PG Output

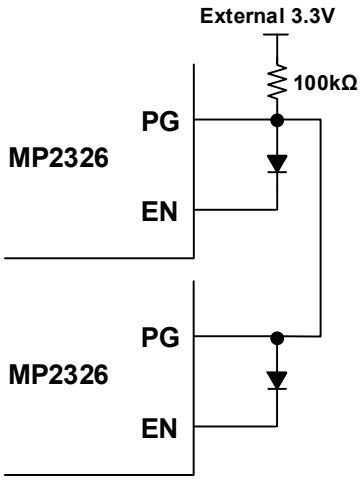


Figure 13: PG Pull up to external power supply with enable control signal --- PG parallel Output

External Bootstrap Diode

BST voltage may become insufficient during particular conditions. In these cases, an external bootstrap diode can enhance the efficiency of the regulator and help to avoid insufficient BST voltage during light-load PFM operation. The insufficient BST voltage is more likely to happen at either of the following conditions:

- V_{IN} is low
- The duty cycle is large: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases (if insufficient BST voltage occurs), the output-ripple voltage may become extremely large during a light-load condition, or there may be poor efficiency during a heavy-load condition. Add an external BST diode from VCC to BST as shown in Fig. 14.

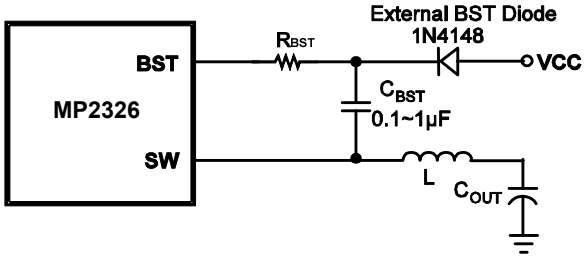


Figure 14: Optional External Bootstrap Diode

The recommended external BST diode is IN4148.

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PCB Layout Guidelines

Efficient PCB layout is critical for efficient operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, please refer to Fig.15 and follow the guidelines below:

1）Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.

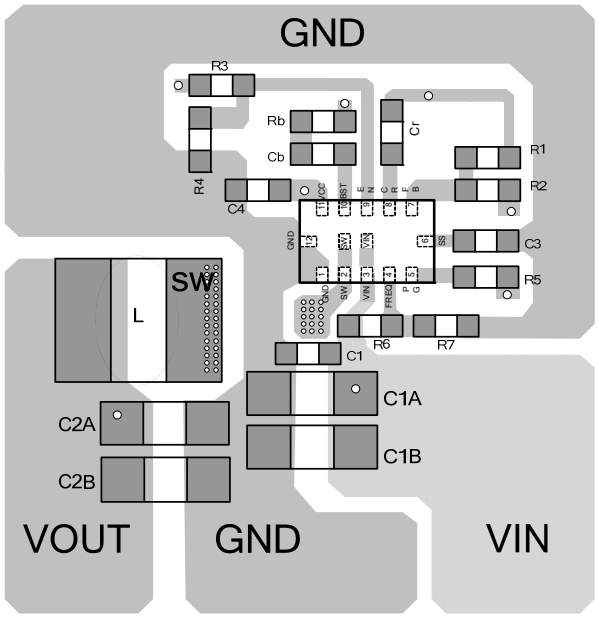
2）Place the input capacitor as close as possible to IN and GND.

3）Place the FREQ/MODE circuit very close to the part.

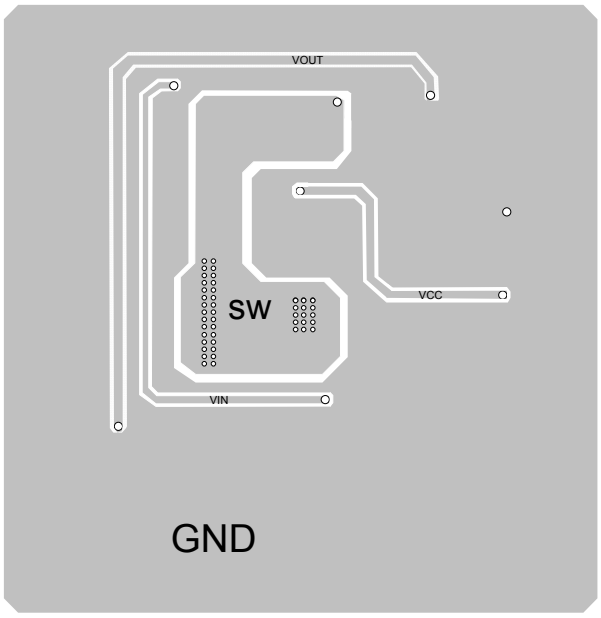
4）Place the external feedback resistors next to FB.

5）Keep the switching node SW short and away from the feedback network.

For optimum performance, use 4-layer boards. Fig. 15 shows the top and bottom layers of the PCB (Inner 1 and Inner 2 are all GND).



Top Layer



Bottom Layer

Figure 15: Recommended PCB Layout

Design Example

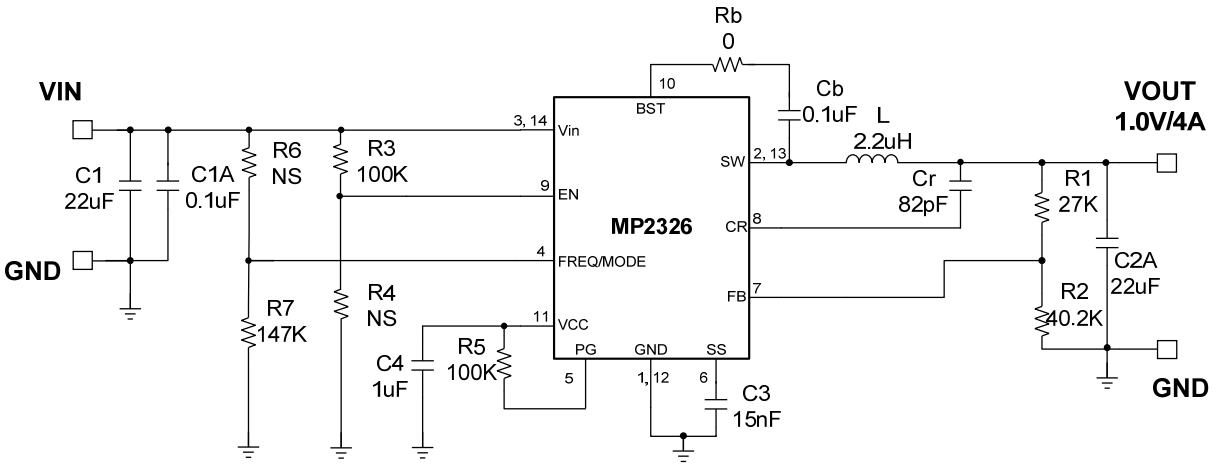
A design example is provided below when ceramic capacitors are applied:

V_{IN}	12V
V_{OUT}	1.2V
I_{OUT}	4A

The detailed application schematic is shown in Fig. 17. The typical performance and waveforms have been shown in the “Typical Characteristics” section. For additional device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

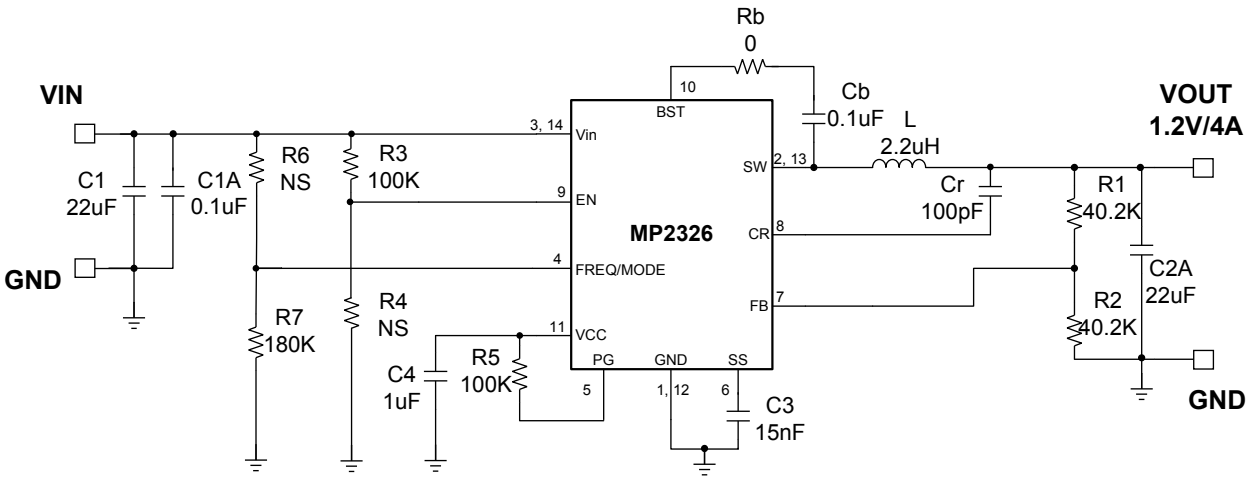


Note:

a. Do NOT use R7 to set the forced PWM; use R6=130k. Do NOT use R6 to set the auto PFM/PWM; use R7=147k. The recommended R6 and R7 values are based on equations 12 and 13, and they are optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 16: V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=4A, F_S=500kHz



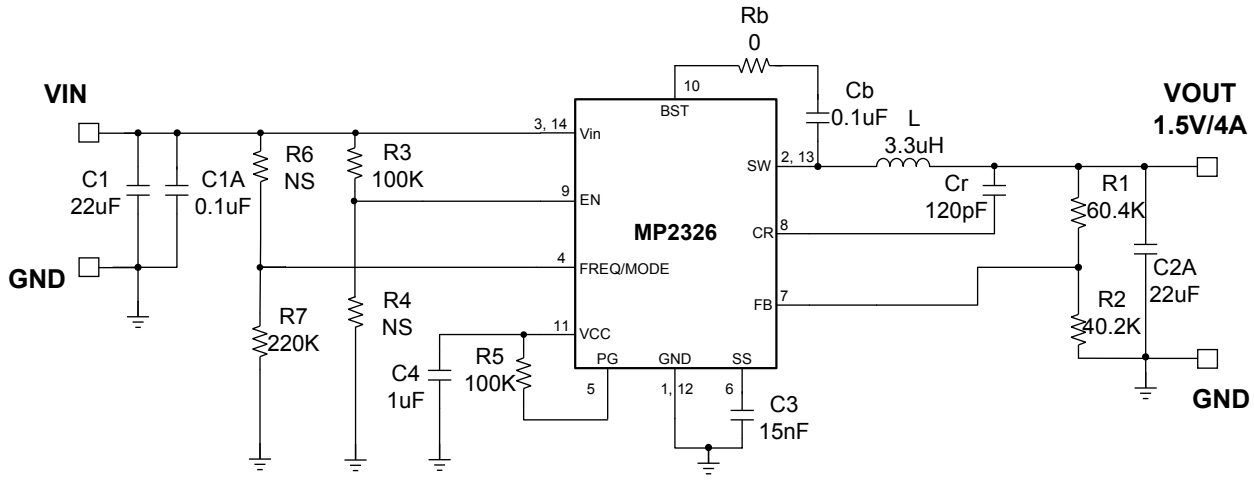
Note:

a. Do NOT use R7 to set the forced PWM; use R6=158k. Do NOT use R6 to set the auto PFM/PWM; use R7=180k. The recommended R6 and R7 values are based on equations 12 and 13, and they are optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 17: V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=4A, F_S=500kHz

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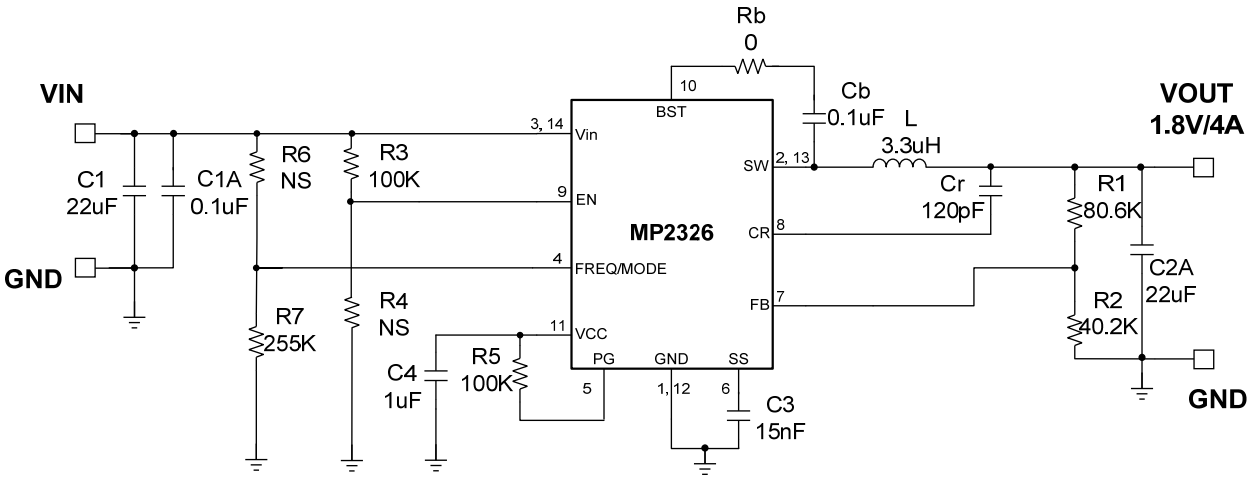


Note:

a. Do NOT use R7 to set the forced PWM; use R6=196k. Do NOT use R6 to set the auto PFM/PWM; use R7=220k. The recommended R6 and R7 values are based on equations 12 and 13, and they are optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 18: V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=4A, F_S=500kHz



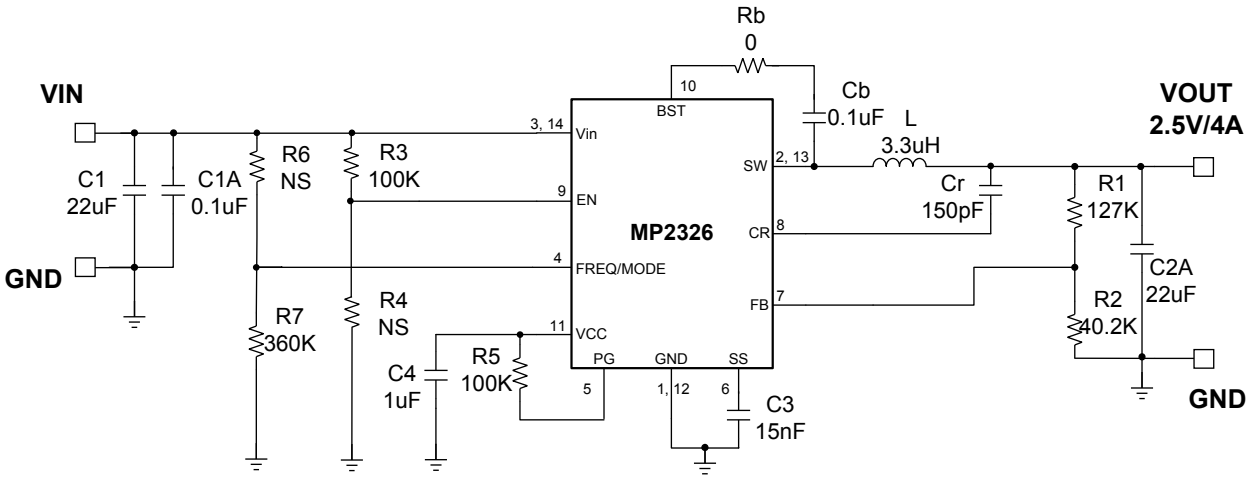
Note:

a. Do NOT use R7 to set the forced PWM; use R6=243k. Do NOT use R6 to set the auto PFM/PWM; use R7=255k. The recommended R6 and R7 values are based on equations 12 and 13, and they are optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 19: V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=4A, F_S=500kHz

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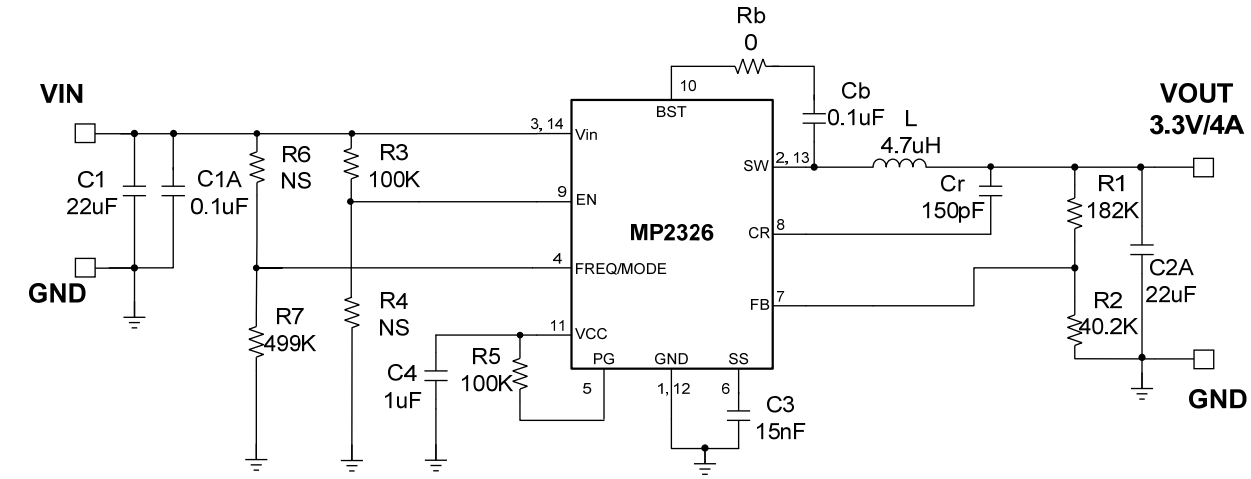


Note:

a. Do NOT use R7 to set the forced PWM; use R6 =348k. Do NOT use R6 to set the auto PFM/PWM; use R7= 360k. The recommended R6 and R7 values are based on equations 12 and 13, and they are optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 20: V_{IN}=12V, V_{OUT}=2.5V, I_{OUT}=4A, F_S=500kHz



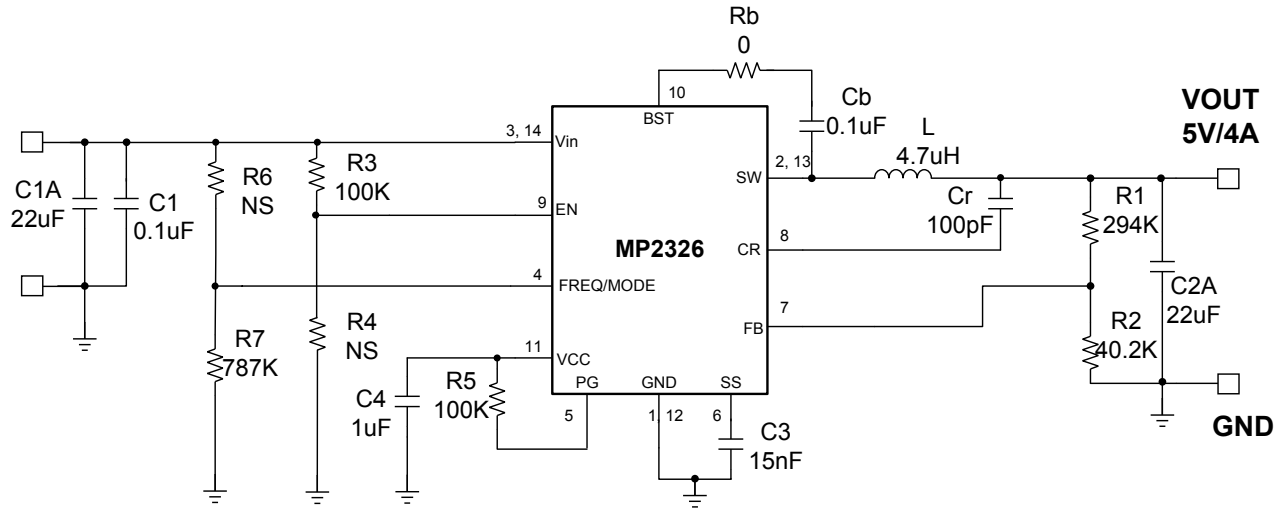
Note:

a. Do NOT use R7 to set the forced PWM; use R6=453k. Do NOT use R6 to set the auto PFM/PWM; use R7=499k.The recommended R6 and R7 values are based on equations 12 and 13, and they are optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 21: V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=4A, F_S=500kHz

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Note:

a. Do NOT use R7 to set the forced PWM; use R6=715k. Do NOT use R6 to set the auto PFM/PWM; use R7=787k. The recommended R6 and R7 values are based on equations 12 and13, and they are optimized according to test results.

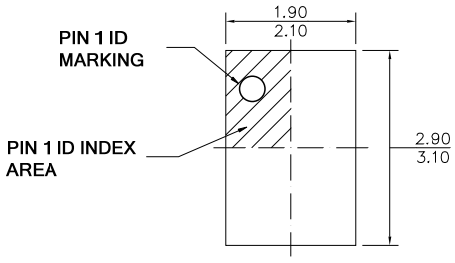
b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

Figure 22: V_{IN}=12V, V_{OUT}=5V, I_{OUT}=4A, F_S=500kHz

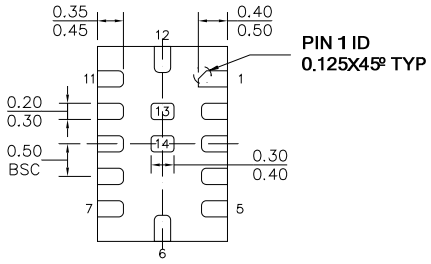
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PACKAGE INFORMATION

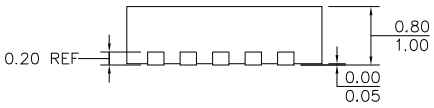
QFN-14 (2mmx3mm)



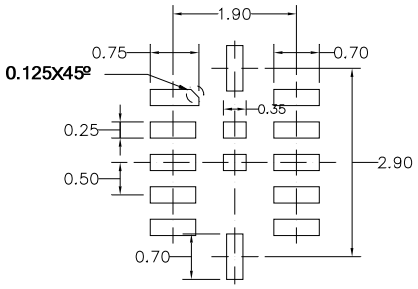
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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