# MP2315S

## 3A, 24V, 500kHz, High-Efficiency, Synchronous, Step-Down Converter

The Future of Analog IC Technology

## DESCRIPTION

The MP2315S is a high-efficiency, synchronous, rectified, step-down, switch mode converter with built-in, internal power MOSFETs. It is a next generation of the MP2315. It offers a very compact solution to achieve 3A continuous output current over a wide input supply range with excellent load and line regulation.

The MP2315S uses synchronous mode operation for higher efficiency over the output current-load range. Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

The MP2315S requires a minimal number of readily available, standard, external components and is available in a compact TSOT23-8 package.

## FEATURES

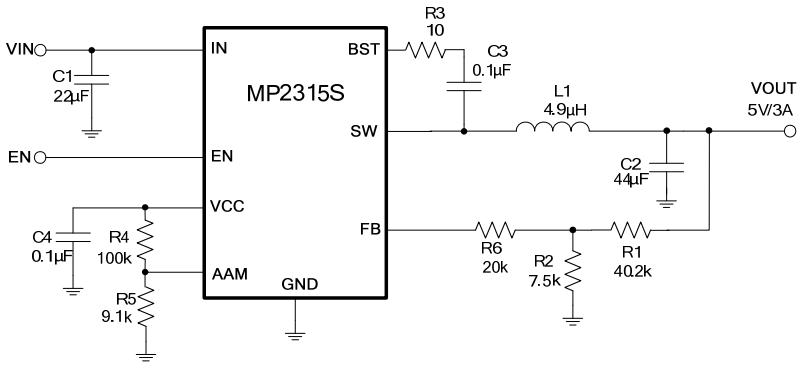
- Wide 4.5V to 24V Operating Input Range
- 3A Load Current
- 110mΩ/55mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Low Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- AAM Power Save Mode
- Internal Soft Start
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a TSOT23-8 Package

## APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat Panel Television and Monitors

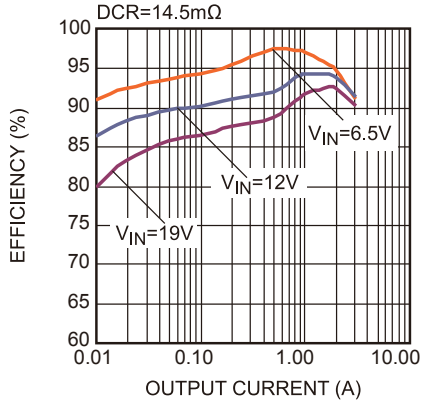
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## TYPICAL APPLICATION




**Efficiency vs. Output Current**

$V_{OUT}$=5V, $V_{AAM}$=0.48V, inductor DCR=14.5mΩ





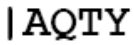
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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP2315SGJ | TSOT23-8 | *See below* |

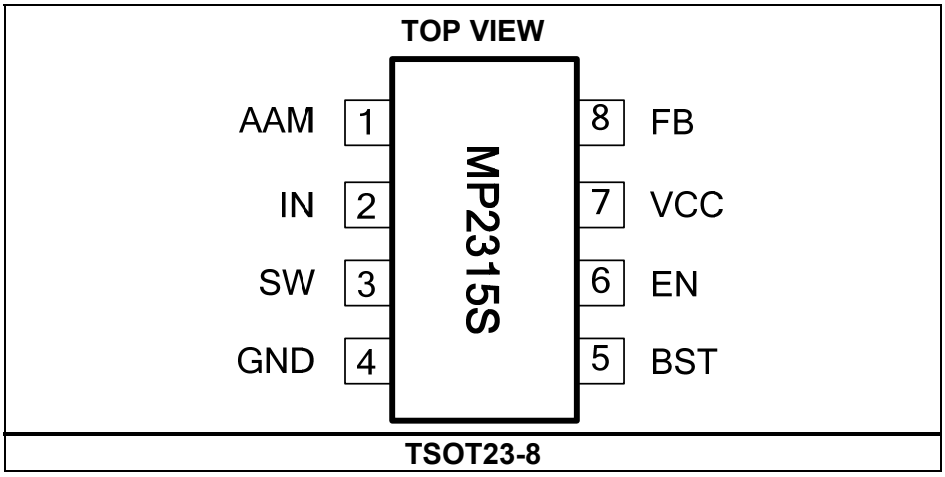
* For Tape & Reel, add suffix –Z (e.g. MP2315SGJ–Z)

## TOP MARKING




AQT: Product code
Y: Year code

## PACKAGE REFERENCE




## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ .....-0.3V to +26V
$V_{SW}$ .....-0.3V (-5V < 10ns) to +28V (30V < 10ns)
$V_{BST}$ ..... $V_{SW}$ + 6V
All other pins .....-0.3V to +5.5V (2)
Continuous power dissipation ($T_A$ = +25°C) (3) ... ..... 1.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to 150°C

### *Recommended Operating Conditions* (4)

Supply voltage ($V_{IN}$) ..... 4.5 to 24V
Output voltage ($V_{OUT}$).....0.8V to $V_{IN}$ * $D_{MAX}$
Operating junction temp ($T_J$). ... -40°C to +125°C

### *Thermal Resistance* (5) $\theta_{JA}$ $\theta_{JC}$

TSOT23-8……...…..100…..55...°C/W

**NOTES:**

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS MAX rating, please refer to the Enable Control section on page 9.
3) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C.[6] Typical value is tested at $T_J$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply current (shutdown) | $I_{IN}$ | $V_{EN}$ = 0V, $T_J$ = 25°C | | | 1 | μA |
| Supply current (quiescent) | $I_q$ | $V_{EN}$ = 2V, $V_{FB}$ = 0.85V, AAM = 0.4V | | 120 | | μA |
| HS switch on resistance | $HS_{RDS-ON}$ | $V_{BST-SW}$ = 5V | | 110 | | mΩ |
| LS switch on resistance | $LS_{RDS-ON}$ | $V_{CC}$ = 5V | | 55 | | mΩ |
| Switch leakage | $SW_{LKG}$ | $V_{EN}$ = 0V, $V_{SW}$ = 12V, $T_J$ = 25°C | | | 1 | μA |
| Current limit | $I_{LIMIT}$ | Duty cycle = 40% | 4.5 | 5.5 | 6.5 | A |
| Oscillator frequency | $f_{SW}$ | $V_{FB}$ = 750mV | 400 | 500 | 600 | kHz |
| Foldback frequency | $f_{FB}$ | $V_{FB}$ = 200mV | | 0.5 | | $f_{SW}$ |
| Maximum duty cycle | $D_{MAX}$ | $V_{FB}$ = 750mV | 90 | 95 | | % |
| Minimum on time [7] | $T_{ON_MIN}$ | | | 60 | | ns |
| Feedback voltage | $V_{FB}$ | | 783 | 791 | 800 | mV |
| Feedback current | $I_{FB}$ | $V_{FB}$ = 820mV | | 10 | 50 | nA |
| EN rising threshold | $V_{EN_RISING}$ | | 1.26 | 1.4 | 1.54 | V |
| EN hysteresis | $V_{EN_HYS}$ | | | 150 | | mV |
| EN input current | $I_{EN}$ | $V_{EN}$ = 2V | 1 | 2 | 3 | μA |
| | | $V_{EN}$ = 0 | | 0 | 50 | nA |
| EN turn-off delay | $EN_{Td-off}$ | | 5 | 9 | 13 | μs |
| $V_{IN}$ under-voltage lockout threshold rising | $INUV_{Vth}$ | | 3.85 | 4.05 | 4.25 | V |
| $V_{IN}$ under-voltage lockout threshold hysteresis | $INUV_{HYS}$ | | 600 | 750 | 900 | mV |
| VCC regulator | $V_{CC}$ | | 4.85 | 5.1 | 5.35 | V |
| VCC load regulation | | $I_{CC}$ = 5mA | | 1.5 | | % |
| Soft-start period | $T_{SS}$ | 10% to 90% | 0.8 | 1.5 | 2.2 | ms |
| Thermal shutdown [7] | $T_{SD}$ | | | 150 | | ºC |
| Thermal hysteresis [7] | $T_{HYS}$ | | | 20 | | ºC |
| AAM source current | $I_{AAM}$ | | | 6.7 | | μA |
| OVP rising threshold | $OV_{H_RISE}$ | FB voltage | 115% | 120% | 125% | VREF |
| OVP falling threshold | $OV_{L_FALL}$ | FB voltage | 104% | 109% | 114% | VREF |
| OVP delay [7] | $OV_{DEY}$ | | | 2 | | μs |

**NOTES:**

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guarantee by engineering sample characterization.

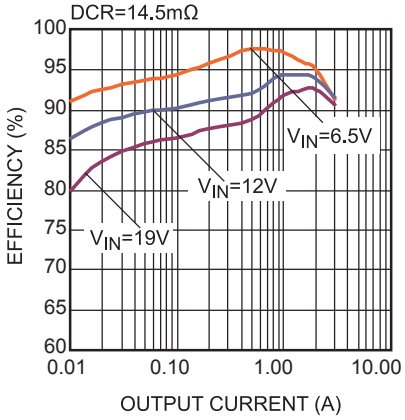

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# TYPICAL CHARACTERISTICS

**$V_{IN}$ = 19V, $V_{OUT}$ = 5V, L = 4.9µH, $T_A$ = 25°C, unless otherwise noted.**

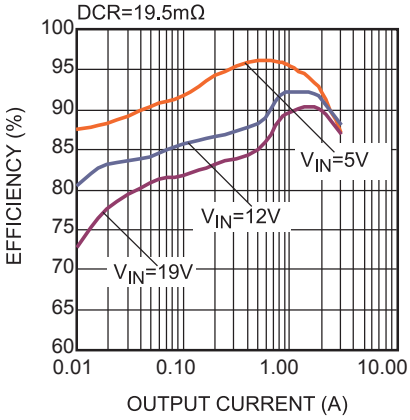
### Efficiency vs. Output Current

$V_{OUT}$=5V, $V_{AAM}$=0.48V, inductor DCR=14.5mΩ



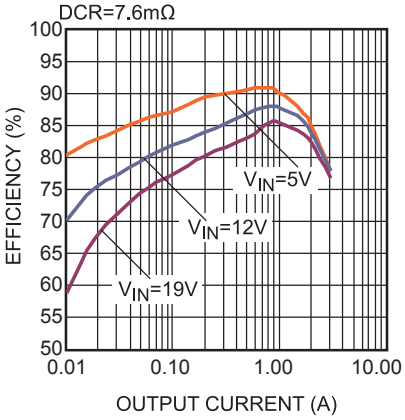

### Efficiency vs. Output Current

$V_{OUT}$=3.3V, $V_{AAM}$=0.4V, inductor DCR=19.5mΩ

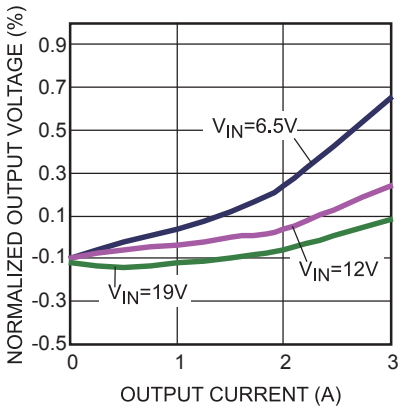



### Efficiency vs. Output Current

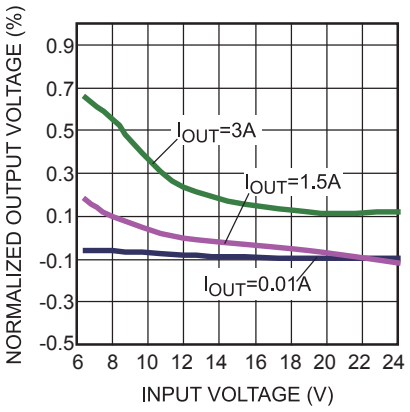
$V_{OUT}$=1.2V, $V_{AAM}$=0.28V, inductor DCR=7.6mΩ



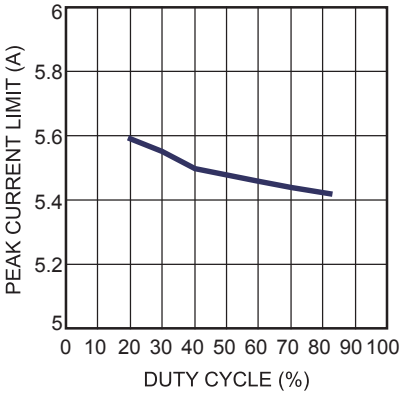

### Load Regulation




### Line Regulation

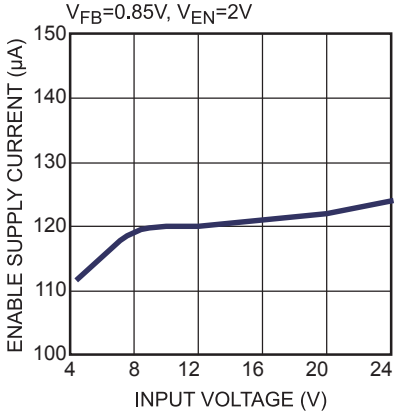



### Current Limit vs. Duty Cycle



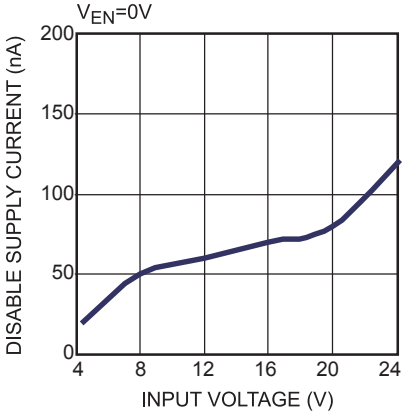

### Enabled Supply Current vs. Input Voltage

$V_{FB}$=0.85V, $V_{EN}$=2V

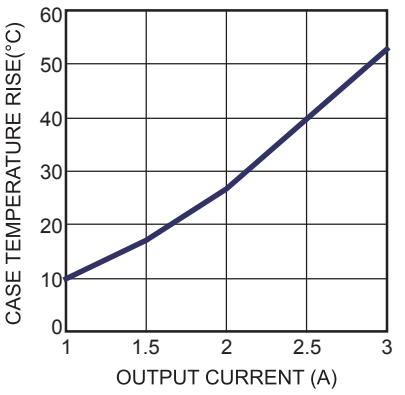



### Disabled Supply Current vs. Input Voltage

$V_{EN}$=0V




### Case Temperature Rise vs. Output Current





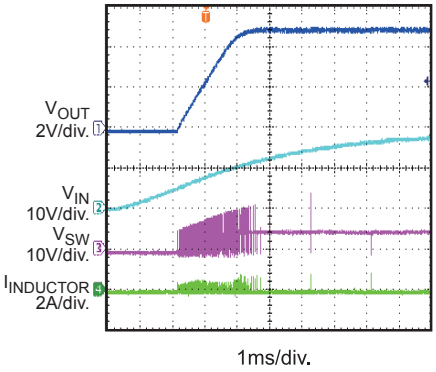
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# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 19V, $V_{OUT}$ = 5V, L = 4.9µH, $T_A$ = 25°C, unless otherwise noted.**

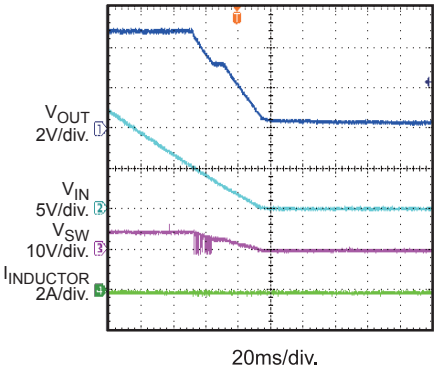
### Start-Up through Input Voltage

$I_{OUT}$=0A



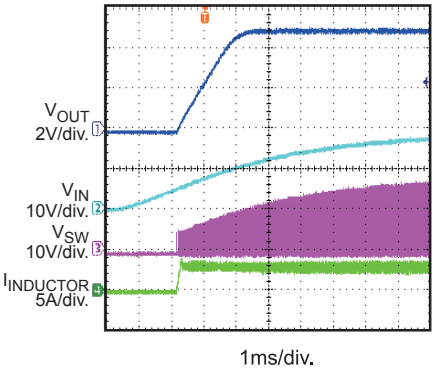

### Shutdown through Input Voltage

$I_{OUT}$=0A



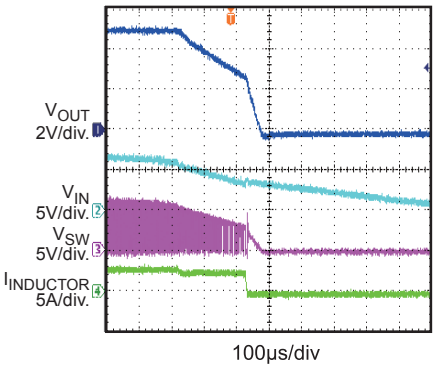

### Start-Up through Input Voltage

$I_{OUT}$=3A



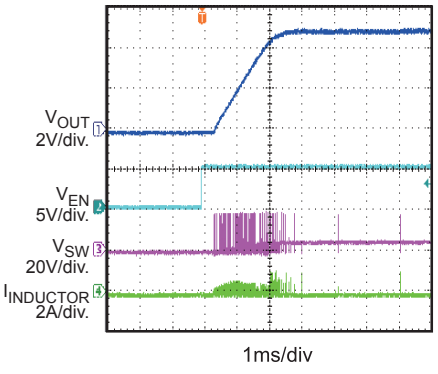

### Shutdown through Input Voltage

$I_{OUT}$=3A



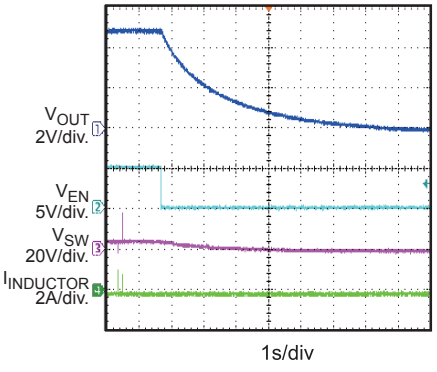

### Start-Up through Enable

$I_{OUT}$=0A



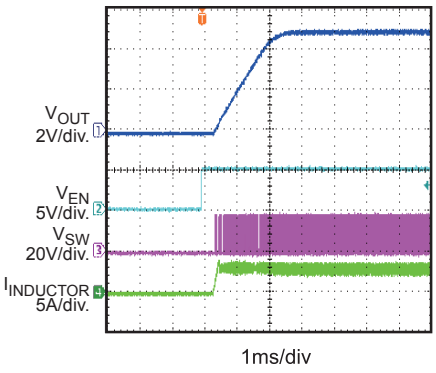

### Shutdown through Enable

$I_{OUT}$=0A



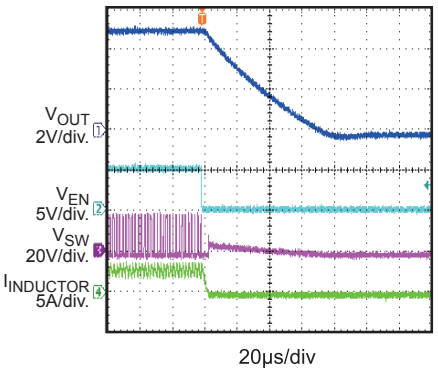

### Start-Up through Enable

$I_{OUT}$=3A



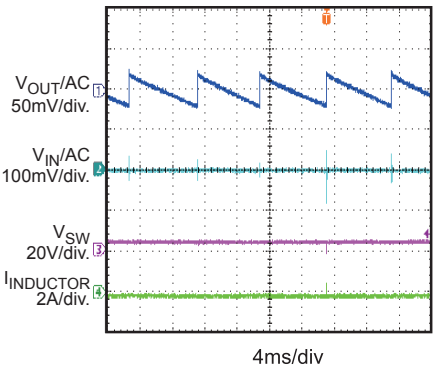

### Shutdown through Enable

$I_{OUT}$=3A




### Input / Output Ripple

$I_{OUT}$=0A





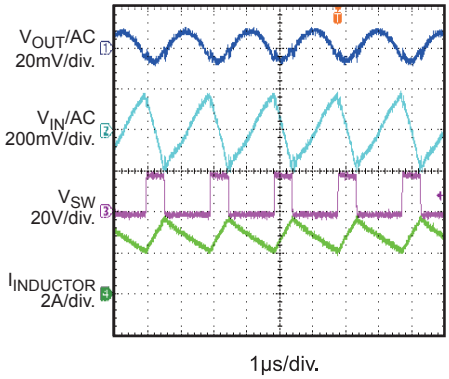
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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 19V, $V_{OUT}$ = 5V, L = 4.9µH, $T_A$ = 25°C, unless otherwise noted.**

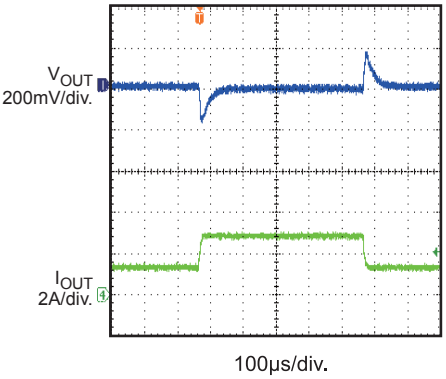
### Input / Output Ripple

$I_{OUT}$=3A



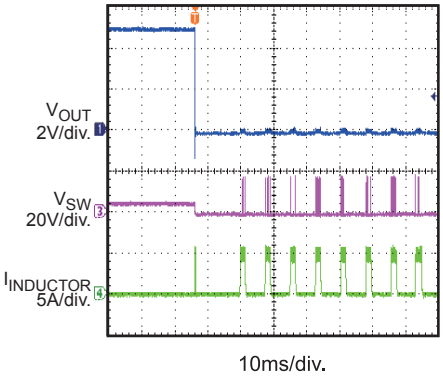

### Transient Response

$I_{OUT}$=1.5A-3A, 2.5A/µs



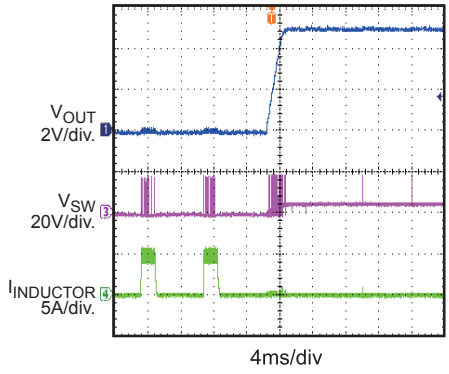

### Short Circuit Entry

$I_{OUT}$=0A



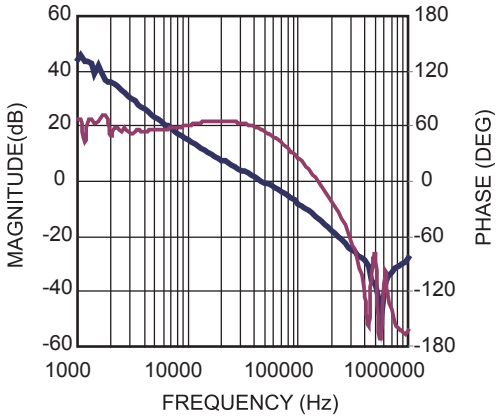

### Short Circuit Recovery

$I_{OUT}$=0A




### Bode Plot

$I_{OUT}$=3A





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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | AAM | **Advanced asynchronous modulation.** Connect AAM to a voltage supply through a resistor divider to force the MP2315S into non-synchronous mode under light-load conditions. Tie AAM to VCC or leave AAM floating to disable AAM mode and force the MP2315S into CCM. |
| 2 | IN | **Supply voltage.** The MP2315S operates with a 4.5V to 24V input rail. C1 is needed to decouple the input rail. Connect using a wide PCB trace. |
| 3 | SW | **Switch output.** Connect using a wide PCB trace. |
| 4 | GND | **System ground.** GND is the reference ground of the regulated output voltage. GND requires special consideration during PCB layout. Connect GND with copper traces and vias. |
| 5 | BST | **Bootstrap.** A capacitor and a resistor are required between SW and BST to form a floating supply across the high-side switch driver. |
| 6 | EN | **Enable.** Drive EN high to enable the MP2315S. |
| 7 | VCC | **Internal bias supply, internal 5.1V LDO output.** Decouple VCC with a 0.1μF - 0.22μF capacitor. The capacitance should be no more than 0.22μF. |
| 8 | FB | **Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current-limit runaway during a short-circuit fault condition. |


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## BLOCK DIAGRAM

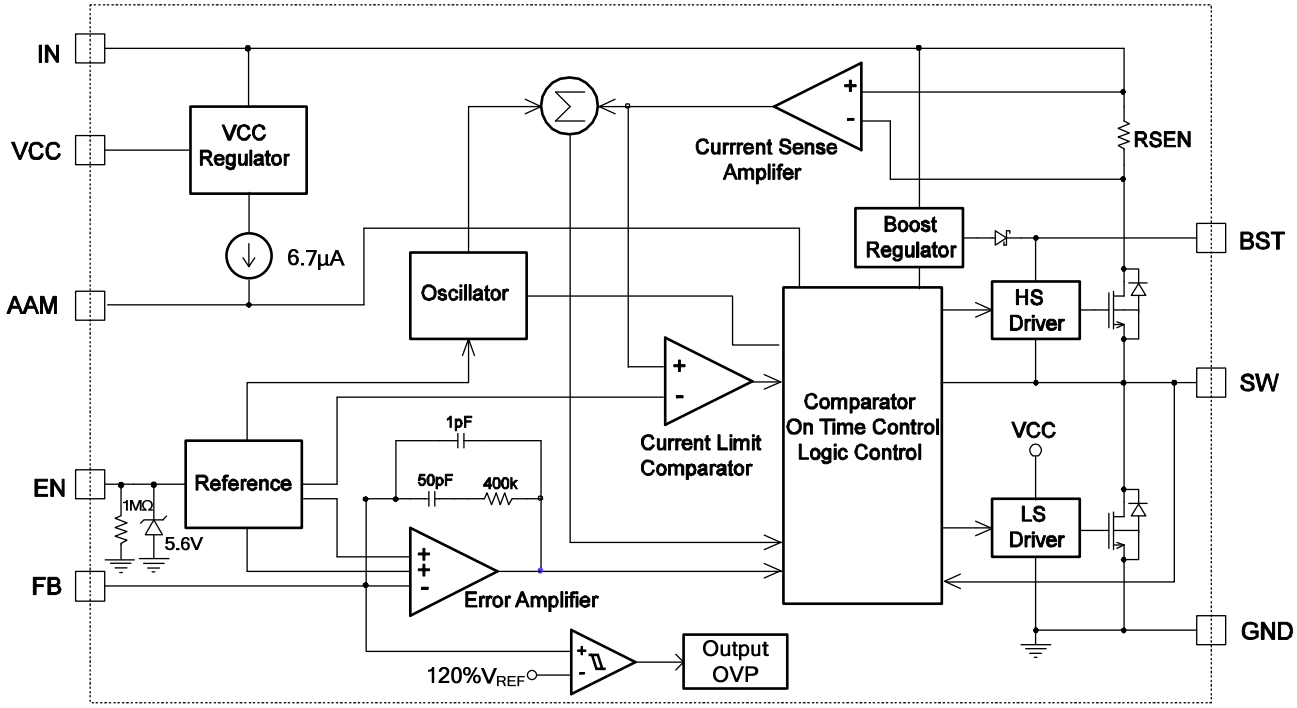



**Figure 1: Functional Block Diagram**


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## OPERATION

The MP2315S is a high-efficiency, synchronous, rectified, step-down, switch mode converter with built-in internal power MOSFETs. It offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input supply range.

When the MP2315S operates in a fixed frequency, the peak-current control mode regulates the output voltage. A pulse width modulation (PWM) cycle is initiated by the internal clock. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage ($V_{COMP}$). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the COMP set current value within 95% of one PWM period, the power MOSFET is forced off.

### Internal Regulator

Most of the internal circuitries are powered by the 5.1V internal regulator. This regulator takes the $V_{IN}$ input and operates in the full $V_{IN}$ range. When $V_{IN}$ is greater than 5.1V, the output of the regulator is in full regulation. When $V_{IN}$ drops below 5.1V, the output decreases. A 0.1μF ceramic capacitor is required for decoupling.

### Error Amplifier (EA)

The error amplifier compares the FB voltage with the internal 0.791V reference (REF) and outputs a COMP voltage which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

### AAM Operation

The MP2315S uses advanced asynchronous modulation (AAM) power save mode in light load. Set the AAM voltage with the tap of an external resistor divider from VCC to GND. Under heavy-load conditions, $V_{COMP}$ is higher than $V_{AAM}$. When the clock goes low, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by $V_{COMP}$. The internal clock resets whenever $V_{COMP}$ is higher than $V_{AAM}$.

Under light-load conditions, the value of $V_{COMP}$ is low. When $V_{COMP}$ is less than $V_{AAM}$, and $V_{FB}$ is less than $V_{REF}$, $V_{COMP}$ ramps up until it exceeds $V_{AAM}$. During this time, the internal clock is blocked, and the MP2315S skips some pulses for pulse frequency modulation (PFM) mode and achieves a light-load power save.

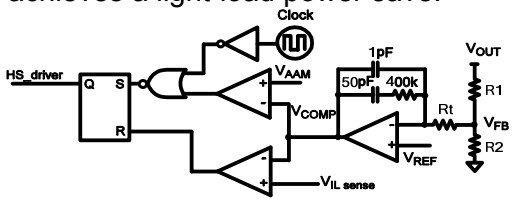



**Figure 2: Simplified AAM Control Logic**

### Enable Control (EN)

Enable (EN) is a digital control that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 5.6V series Zener diode. Connect the EN input through a pull-up resistor to the voltage on $V_{IN}$ to limit the EN input current below 100μA. For example, with 19V connected to $V_{IN}$, $R_{PULLUP}$ ≥ (19V - 5.6V) ÷ 100μA = 134kΩ.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source below 5.5V to prevent damage to the Zener diode.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to prevent the chip from operating at an insufficient supply voltage. The MP2315S UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.05V, while its falling threshold is 3.3V.

### Internal Soft-Start (SS)

The soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.791V. At this point, the reference voltage takes over. The soft-start time is internally set to around 1.5ms.


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### Output Over-Voltage Protection (OVP)

The MP2315S monitors the FB voltage to detect output over-voltage. When the FB voltage rises higher than 120% of the reference voltage, the MP2315S enters a dynamic regulation period. During this period, the IC forces the low-side MOSFET (LS-FET) on until a -800mA negative current limit is achieved. This discharges the output to keep it within the normal range. The MP2315S exits dynamic regulation when FB falls below 109% of the reference voltage.

### Over-Current Protection (OCP) and Hiccup

The MP2315S uses a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current-limit threshold. The output voltage begins dropping until FB is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP2315S enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate the thermal issue and protect the regulator. The MP2315S exits hiccup mode once the over-current condition is removed.

### Pre-Bias Start-Up

The MP2315S is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start capacitor voltage exceeds the sensed output voltage at FB, the part begins working normally.

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, the entire chip shuts down. When the temperature is lower than its lower threshold, typically 130°C, the chip is enabled again.

### Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by $V_{IN}$ through D1, R3, C3, L1, and C2 (see Figure 3). If $V_{IN}$ - $V_{SW}$ is more than 5V, U2 regulates M3 to maintain a 5V BST voltage across C3.

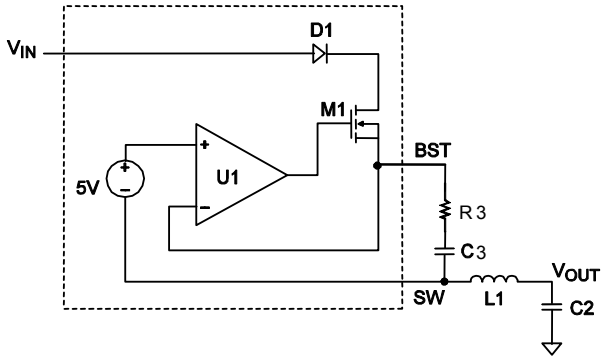



**Figure 3: Internal Bootstrap Charging Circuit**

### Start-Up and Shutdown

If both $V_{IN}$ and EN are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current. The internal regulator is then enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, $V_{IN}$ low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to prevent any fault triggering. $V_{COMP}$ and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.


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# APPLICATION INFORMATION

## Setting the Output Voltage

An external resistor divider is used to set the output voltage. The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). R2 can then be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.791V} - 1} \quad (1)$$

The T-type network is highly recommended (see Figure 4).

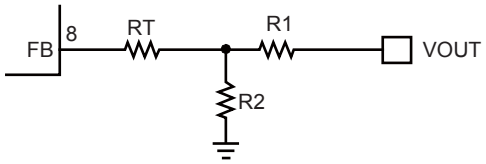



**Figure 4: T-Type Network**

Table 1 lists the recommended T-type resistor values for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages(8)**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | Rt (kΩ) |
|---|---|---|---|
| 1.05 | 20.5 | 62 | 100 |
| 1.2 | 20.5 | 39.2 | 75 |
| 1.8 | 40.2 | 31.6 | 59 |
| 2.5 | 40.2 | 18.7 | 40.2 |
| 3.3 | 40.2 | 12.7 | 33 |
| 5 | 40.2 | 7.5 | 20 |

**NOTE:**

8) The recommended parameters are based on a 44µF output capacitor. A different input voltage, output inductor value, and output capacitor value may affect the selection of R1, R2, and Rt. For additional component parameters, please refer to the Typical Application Circuits section on pages 15 and 16.

## Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% percent higher than the maximum load current is recommended for most applications. For the highest efficiency, the inductor DC resistance should be less than 20mΩ. For most designs, the inductance value can be derived using Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where $\Delta I_L$ is the inductor ripple current.

Choose the inductor current to be approximately 40% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions below 100mA, a larger inductance is recommended for better efficiency.

## Setting the AAM Voltage

The AAM voltage is used to set the transition point from AAM to PWM. It should be chosen to provide the best combination of efficiency, stability, ripple, and transient.

If the AAM voltage is set low, then the stability and ripple improve, but AAM mode and transient efficiency degrade. Likewise, if the AAM voltage is set high, then AAM mode and transient efficiency improves, but the stability and ripple degrade.

Adjust the AAM threshold by connecting divider resistors from VCC to GND. Note that there is a 6.7µA current source at AAM (see Figure 5).

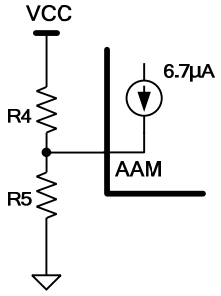



**Figure 5: AAM Network**

Generally, $V_{AAM}$ can be calculated with Equation (4):

$$V_{AAM} = \frac{R_5 \times (VCC + 6.7\mu A \times R_4)}{R_4 + R_5} \quad (4)$$

R5 should be no larger than 20k.


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The optimized AAM can be found in Figure 6.

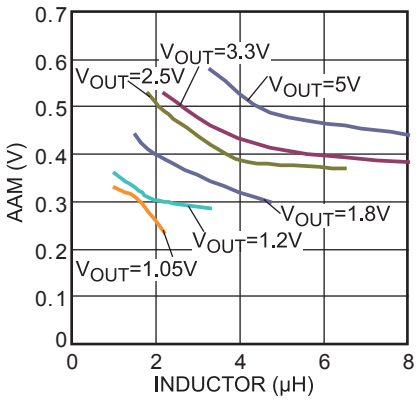



**Figure 6: AAM Selection for Common Output Voltages ($V_{IN}$ = 4.5V - 24V)**

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to a provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

### Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where $L_1$ is the inductor value and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2315S can be optimized for a wide range of capacitance and ESR values.

### External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator. The applicable conditions of the external BST diode are:

- $V_{OUT}$ is 5V or 3.3V
- Duty cycle is high: D = $\frac{V_{OUT}}{V_{IN}}$ > 65%


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In these cases, an external BST diode is recommended from VCC to BST (see Figure 7).

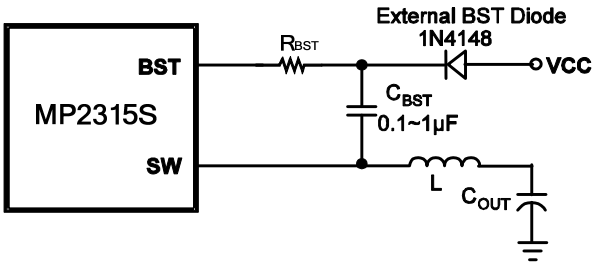



**Figure 7: Add Optional External Bootstrap Diode to Enhance Efficiency**

The recommended external BST diode is 1N4148, and the recommended BST capacitor is 0.1 - 1μF.

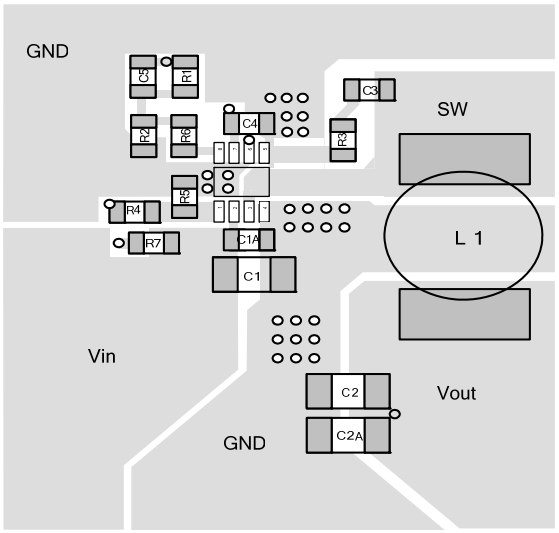
## PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 8 and follow the guidelines below:

1. Keep the connection of the input ground and GND as short and wide as possible.
2. Keep the connection of the input capacitor and IN as short and wide as possible.
3. Place the VCC capacitor as close to VCC and GND as possible.
4. Make the trace length of VCC - VCC capacitor anode - VCC capacitor cathode - IC GND as short as possible.
5. Ensure that all feedback connections are short and direct.
6. Place the feedback resistors and compensation components as close to the IC as possible.
7. Route SW away from sensitive analog areas, such as FB.

**NOTE:**

9) The recommended layout is based on Figure 9 on page 15.



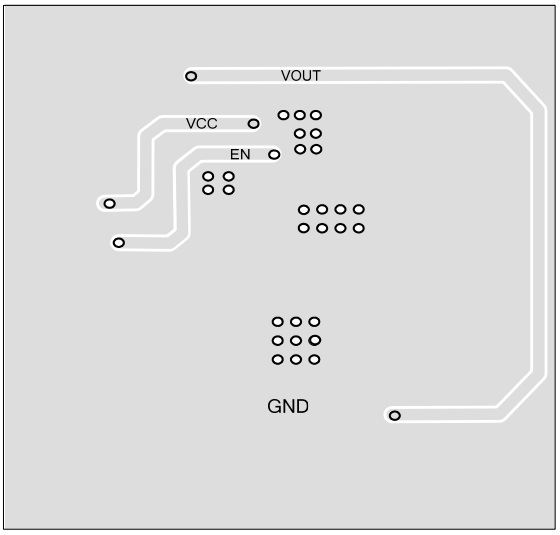




**Figure 8: Sample Board Layout**

## Design Example

Table 2 is a design example following the application guidelines for the specifications below:

**Table 2: Design Example**

| | |
|---|---|
| $V_{IN}$ | 19V |
| $V_{OUT}$ | 5V |
| $I_O$ | 3A |

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.


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## TYPICAL APPLICATION CIRCUITS

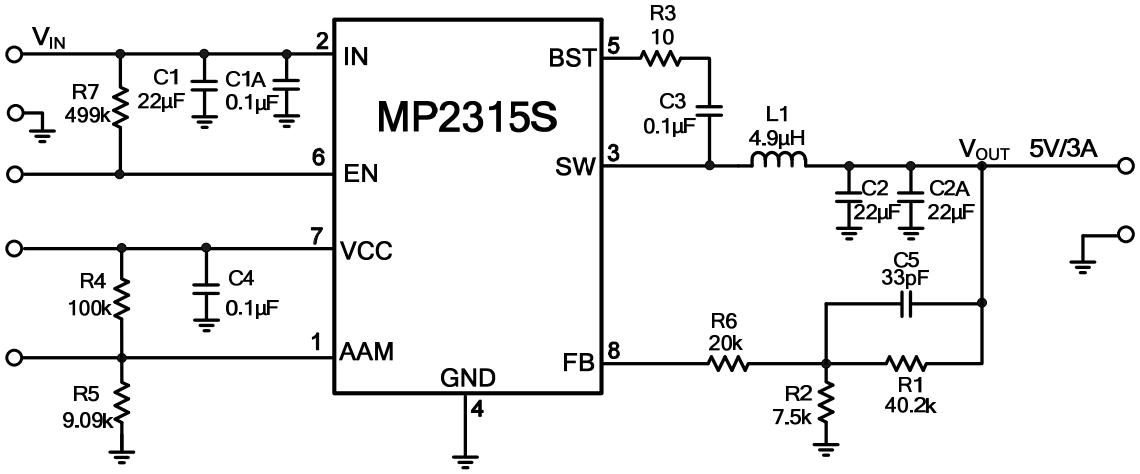



**Figure 9: $V_{IN}$ = 6.5V - 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 3A**

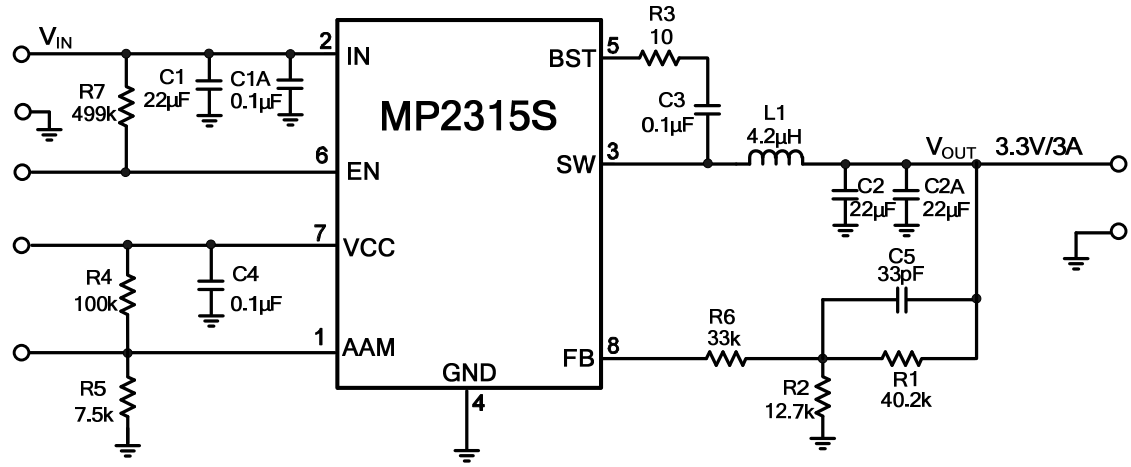



**Figure 10: $V_{IN}$ = 4.5V - 24V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 3A**

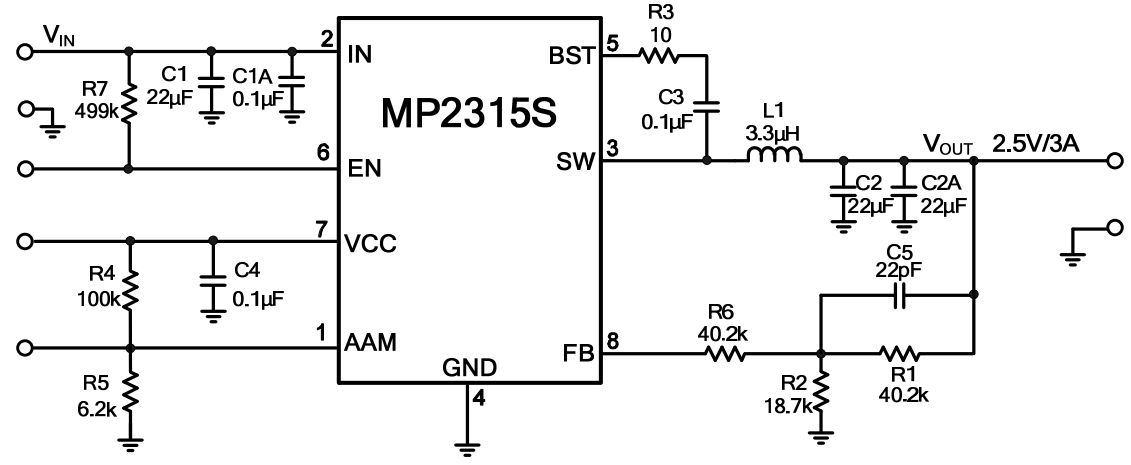



**Figure 11: $V_{IN}$ = 4.5V - 24V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 3A**


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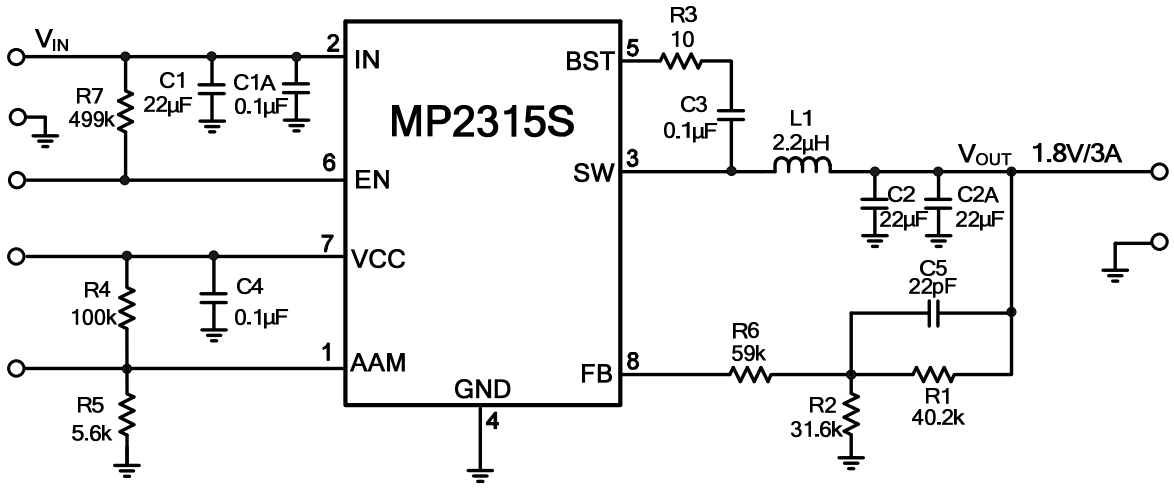



**Figure 12: $V_{IN}$ = 4.5V - 24V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

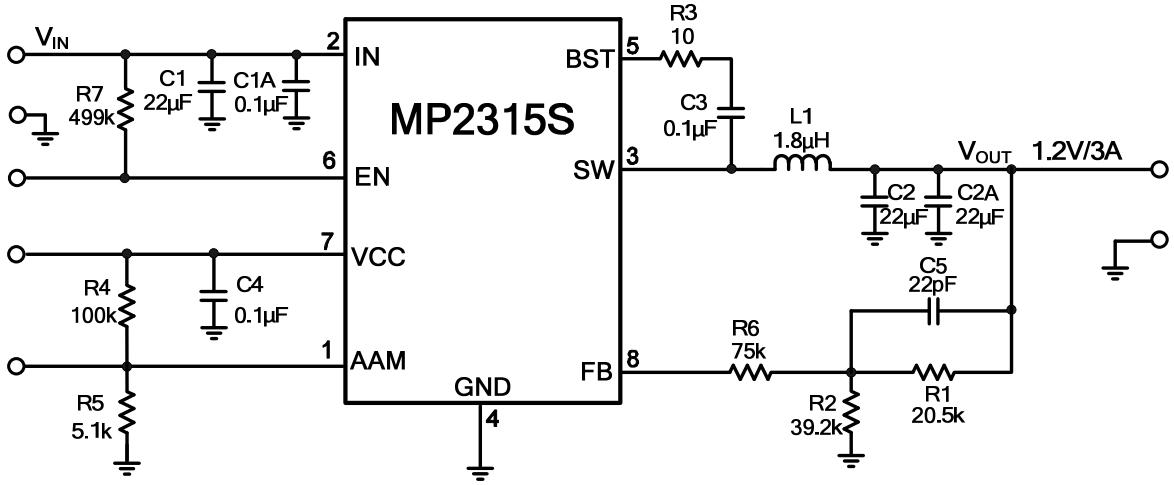



**Figure 13: $V_{IN}$ = 4.5V - 24V, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 3A**

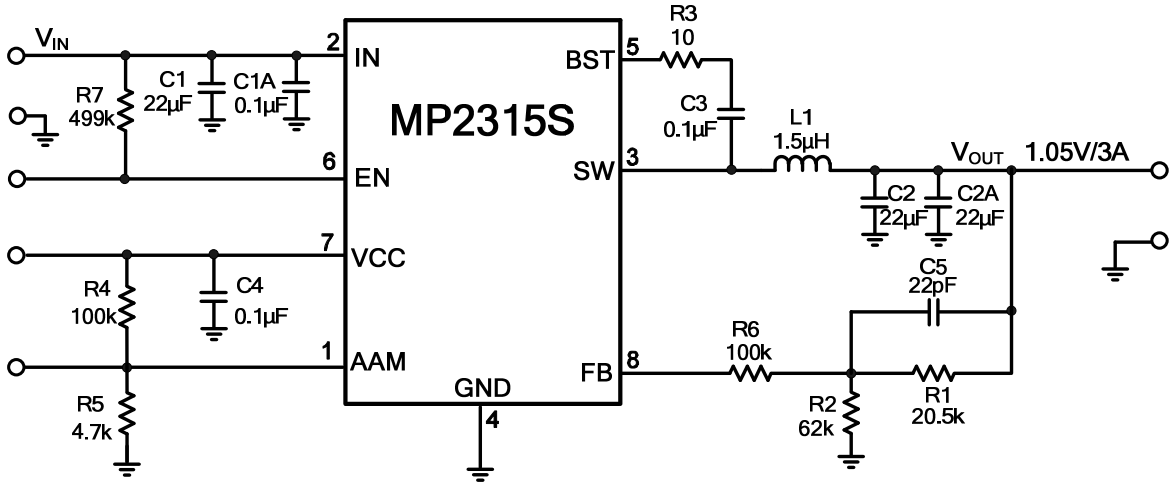
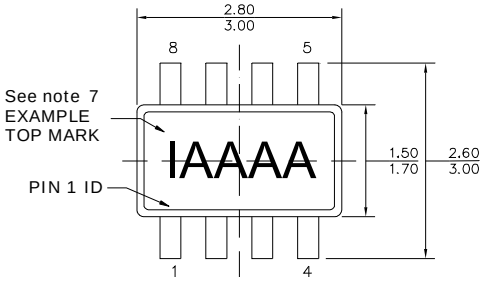



**Figure 14: $V_{IN}$ = 4.5V - 24V, $V_{OUT}$ = 1.05V, $I_{OUT}$ = 3A**

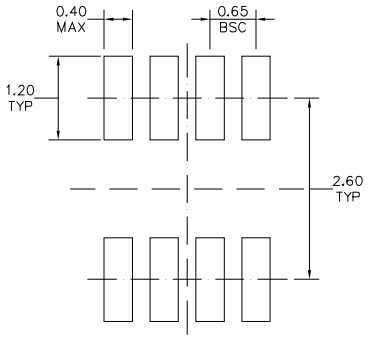

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# PACKAGE INFORMATION

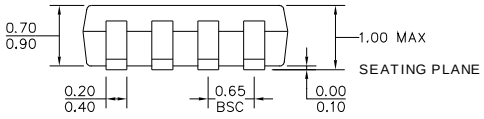
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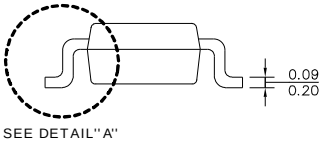

TOP VIEW



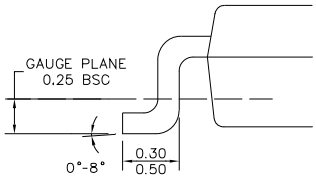

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW




DETAIL "A"

NOTE:

**1) ALL DIMENSIONS ARE IN MILLIMETERS**
**2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR**
**3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION**
**4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.**
**5) JEDEC REFERENCE IS MO193, VARIATION BA**
**6) DRAWING IS NOT TO SCALE**
**7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)**

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