# MP2209

**16V, 2A, 600kHz Synchronous Step-Down Converter**

The Future of Analog IC Technology

## DESCRIPTION

The MP2209 is an internally compensated 600kHz fixed frequency PWM synchronous step-down regulator. With a 3V to 6V bias supply, MP2209 operates from a 3V to 16V input and generates an adjustable output voltage from 0.8V to 0.9x$V_{IN}$ at up to 2A load current.

The MP2209 integrates a 80mΩ high-side switch and a 80mΩ synchronous rectifier for high efficiency without an external Schottky diode. With peak current mode control and internal compensation, it can be stabilized with ceramic capacitors and small inductors. Fault condition protection includes short-circuit protection, cycle-by-cycle current limiting and thermal shutdown.

The MP2209 is available in small 3mmx4mm 14-lead QFN packages.

## FEATURES

- 2A Output Current
- Input Supply Range: 3V to 16V
- 80mΩ Internal Power MOSFET Switches
- Stable with Ceramic Output Capacitors
- High Efficiency
- 600kHz Fixed Switching Frequency
- Adjustable Output from 0.8V to 0.9x$V_{IN}$
- Frequency Synchronization
- Power Good Pin
- Thermal Shutdown
- Cycle-by-Cycle Current Limiting
- Short Circuit Protection
- 3mmx4mm 14-lead QFN Package

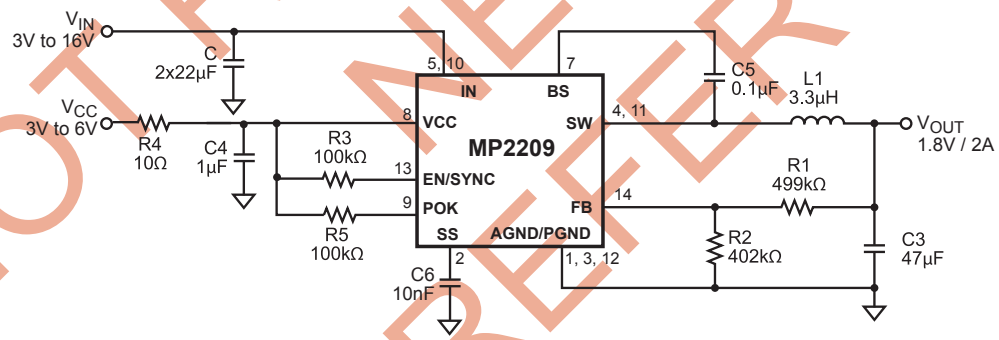
## APPLICATIONS

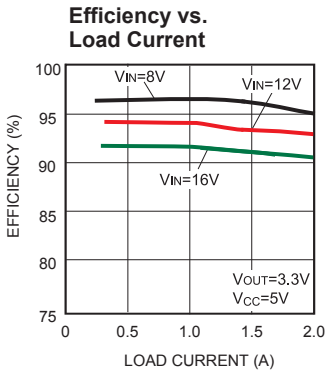
- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Printers and LCD TVs
- Network and Telecom Equipment
- Point of Load Regulators

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

## TYPICAL APPLICATION




NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474

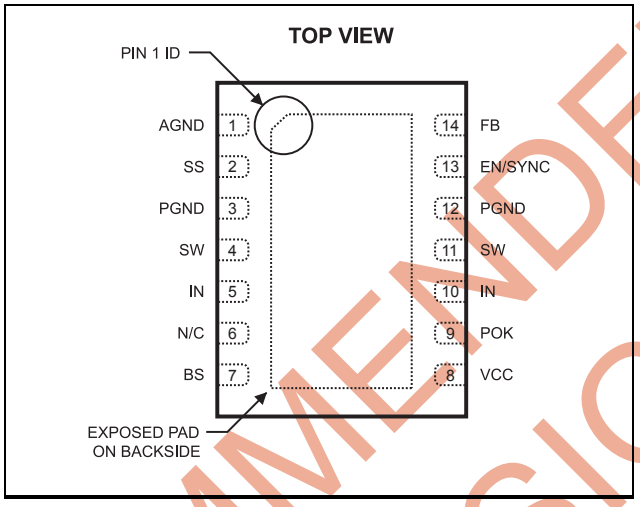

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## ORDERING INFORMATION

| Part Number* | Package | Top Marking | Free Air Temperature ($T_A$) |
|---|---|---|---|
| MP2209DL | QFN14 (3mm x 4mm) | 2209 | –40°C to +85°C |

* For Tape & Reel, add suffix –Z (eg. MP2209DL–Z).
For RoHS compliant packaging, add suffix –LF (eg. MP2209DL–LF–Z)

## PACKAGE REFERENCE




## ABSOLUTE MAXIMUM RATINGS (1)

IN to GND .....-0.3V to +18V
SW to GND .....-0.3V to $V_{IN}$ + 0.3V
.....-2.5V to $V_{IN}$ + 2.5V for < 50ns
FB, EN/SYNC, VCC to GND.....-0.3V to +6.5V
BS to SW .....-0.3V to +6.5V
Continuous Power Dissipation ($T_A$ = +25°C) (2)
.....2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ .....3V to 16V
Bias Voltage $V_{CC}$ .....3V to 6V
Output Voltage $V_{OUT}$.....0.8V to 0.9 x $V_{IN}$
Operating Junct. Temp ($T_J$)..... -40°C to +125°C
EN/SYNC Voltage..... No more than $V_{CC}$

## *Thermal Resistance* (4)

| | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| QFN14 (3mm x 4mm) | 48 | 11 °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J\ (MAX)}$, the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\ (MAX)} = (T_{J\ (MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## ELECTRICAL CHARACTERISTICS (5)

**$V_{IN}$ = 12V, $V_{CC}$ = $V_{EN}$ = 3.6V, $T_A$ = +25°C, unless otherwise noted.**

| Parameters | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ Supply Current | $V_{EN}$ = $V_{CC}$<br>$V_{FB}$ = 0.85V | | 750 | | μA |
| $V_{CC}$ Shutdown Current | $V_{EN}$ = 0V, $V_{IN}$ = 12V , $V_{CC}$ = 6V | | 1 | | μA |
| $V_{CC}$ Undervoltage Lockout Threshold | Rising Edge | | 2.8 | 2.95 | V |
| $V_{CC}$ Undervoltage Lockout Hysteresis | | | 200 | | mV |
| IN Under voltage lockout threshold | Rising Edge | | 2.85 | 2.95 | V |
| IN Under voltage lockout hysteresis | | | 300 | | mV |
| Regulated FB Voltage | $T_A$ = +25°C | 0.781 | 0.794 | 0.807 | V |
| | –40°C ≤ $T_A$ ≤ +85°C | 0.770 | | 0.818 | V |
| FB Input Current | $V_{FB}$ = 0.85V | –50 | | 50 | nA |
| EN High Threshold | –40°C ≤ $T_A$ ≤ +85°C | 1.6 | | | V |
| EN Low Threshold | –40°C ≤ $T_A$ ≤ +85°C | | | 0.4 | V |
| Soft-Start Charging Current | | | 5 | | μA |
| High-Side Switch On-Resistance | $I_{SW}$ = 300mA | | 80 | | mΩ |
| Low-Side Switch On-Resistance | $I_{SW}$ = –300mA | | 80 | | mΩ |
| SW Leakage Current | $V_{EN}$ = 0V; $V_{IN}$ = 12V<br>$V_{SW}$ = 0V or 12V | –10 | | 10 | μA |
| BS Under Voltage Lockout Threshold | | | 2 | | V |
| High-Side Switch Current Limit | Sourcing | | 4 | | A |
| Low-Side Switch Current Limit | Sinking | | 2 | | A |
| Oscillator Frequency | | 450 | 600 | 750 | kHz |
| Synch Frequency | | 0.5 | | 2 | MHz |
| Minimum On Time | | | 50 | | ns |
| Maximum Duty Cycle | | | 90 | | % |
| Thermal Shutdown Threshold | Hysteresis = 20°C | | 150 | | °C |

**Note:**

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1, 3, 12 | PGND, AGND, Exposed Pad | Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors.<br>Connect exposed pad to GND plane for proper thermal performance. |
| 2 | SS | Soft-Start Input. Place a capacitor from SS to AGND. The SS pin sources 5μA. As the SS voltage rises, the feedback threshold voltage increases to limit the inrush current during start-up. Do not leave this pin open. |
| 4, 11 | SW | Switch Node Connection to the Inductor. These pins connect to the internal high and low-side power MOSFET switches. All SW pins must be connected together externally. |
| 5, 10 | IN | Input Supply. This supplies power to the high side switch. A decoupling capacitor to ground is required close to this pin to reduce switching spikes. |
| 6 | N/C | No Connect. |
| 7 | BS | Bootstrap. A capacitor between this pin and SW provides a floating supply for the high-side gate driver. |
| 8 | VCC | Bias Supply. This supplies power to both the internal control circuit and the gate drivers. A decoupling capacitor to ground is required close to this pin. |
| 9 | POK | Power Okay Pin. Open drain power Good output. “HIGH” input indicates $V_{OUT}$ is within ±10% window, “LOW” output indicates $V_{OUT}$ is out of ±10% window. |
| 13 | EN/SYNC | Enable and Frequency Synchronization Input Pin. Forcing this pin below 0.4V shuts down the part. Forcing this pin above 1.6V turns on the part. Applying a 500kHz to 2MHz clock signal to this pin synchronizes the internal oscillator frequency to the external source. |
| 14 | FB | Feedback. This is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal 0.8V reference to set the regulation voltage. Don’t apply a voltage more than $V_{CC}$ to this pin. |

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474

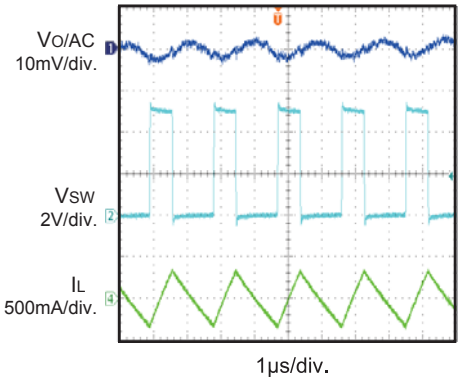

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 5V, $V_{OUT}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.**

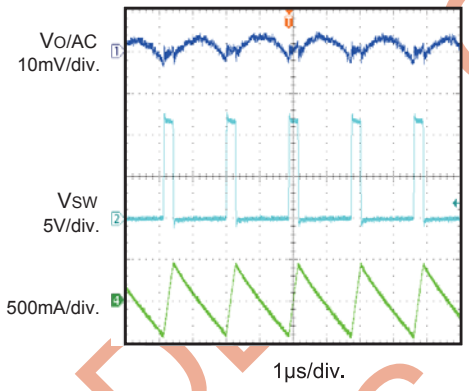
### Switching Waveform

$V_{IN}$=5V,$I_O$=0A



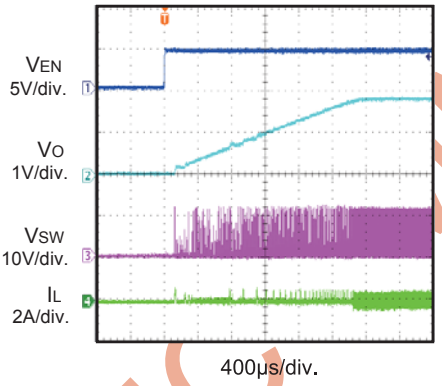

### Switching Waveform

$V_{IN}$=12V,$I_O$=0A



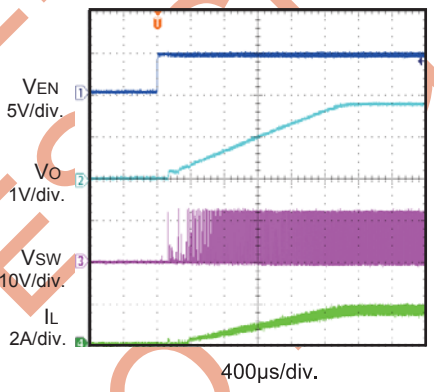

### Enable Start-up

$V_{IN}$=12V,$I_O$=0A



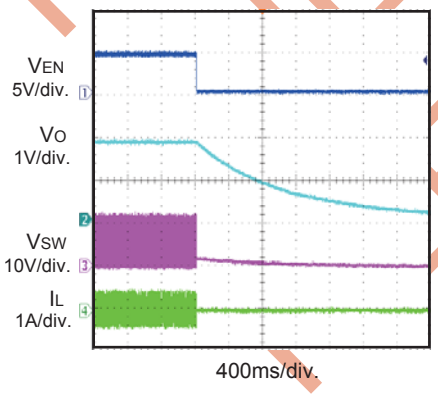

### Enable Start-up

$V_{IN}$=12V,$I_O$=2A



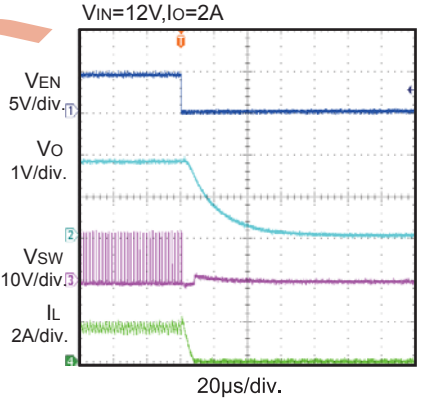

### Enable Shut-down

$V_{IN}$=12V,$I_O$=0A




### Enable Shut-down

$V_{IN}$=12V,$I_O$=2A



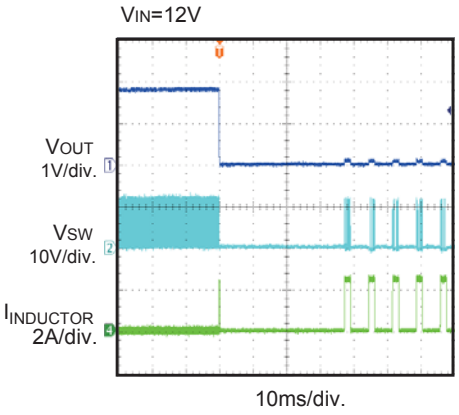

NOT RECOMMENDED FOR NEW DESIGNS REFER TO 1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

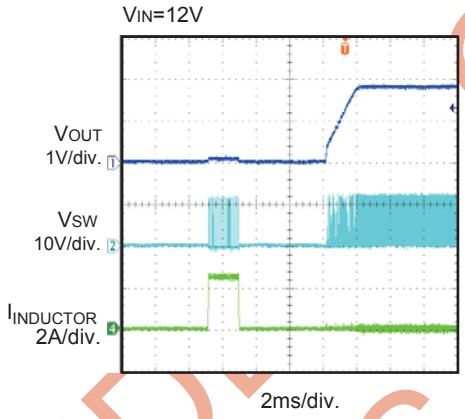
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 5V, $V_{OUT}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted. (*continued*)**

### Short Circuit Protection

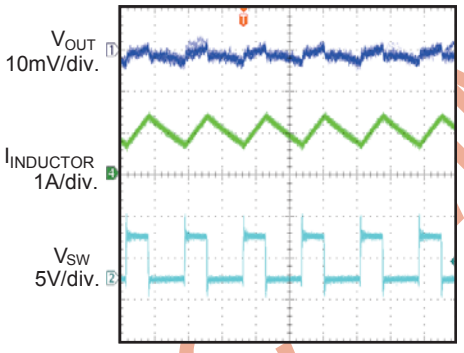



### Short Circuit Recovery



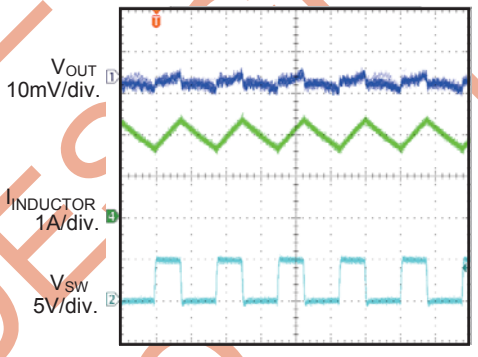

### Steady State Operation

Half Load



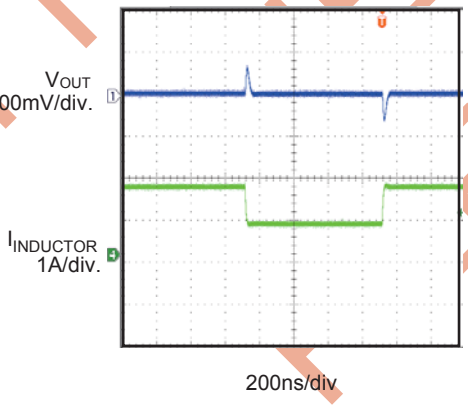

### Steady State Operation

Full Load




### Load Transient

1A-2A Step Resistive Load




NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## FUNCTIONAL BLOCK DIAGRAM

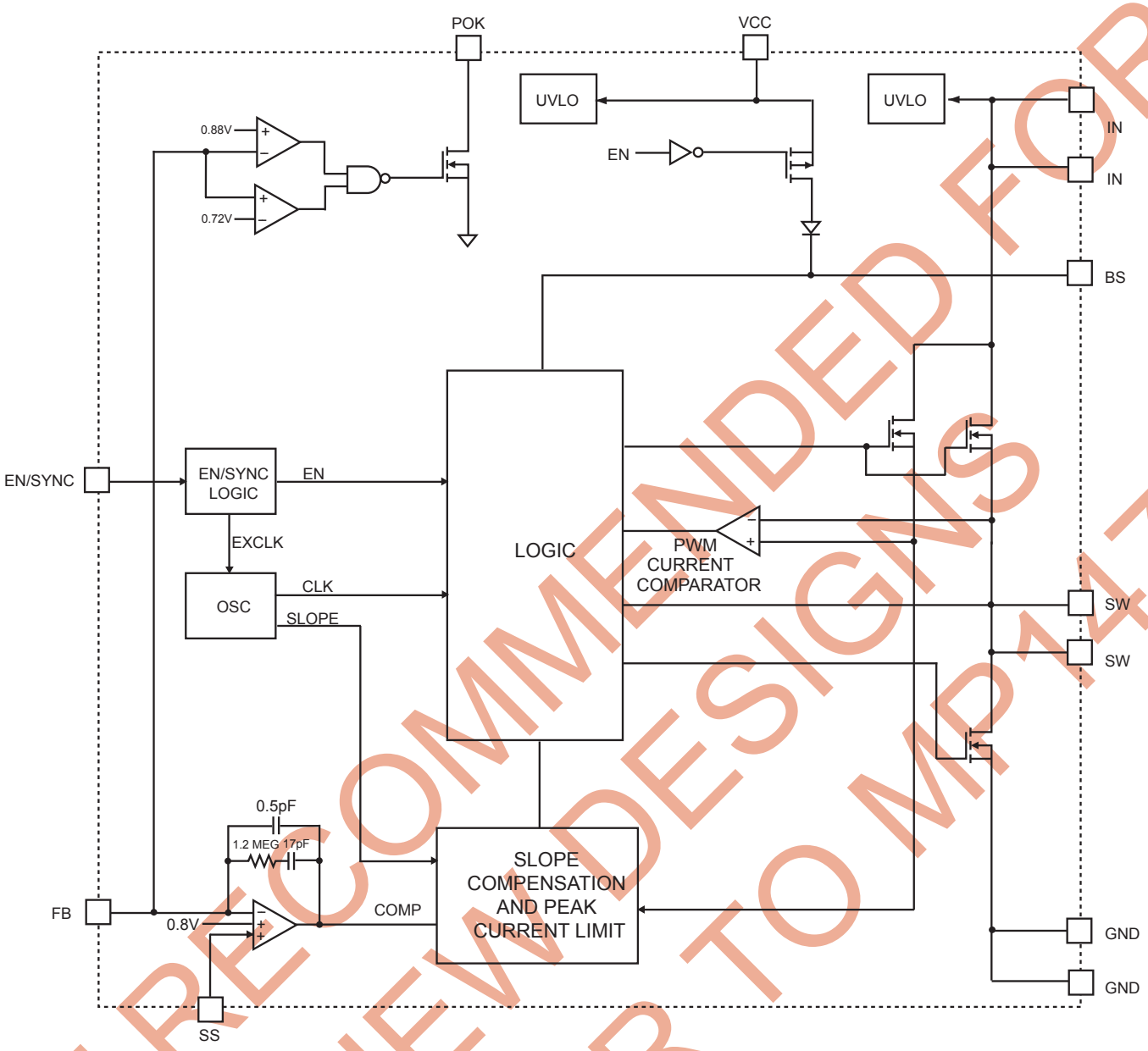



**Figure 1—Functional Block Diagram**

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## OPERATION

### PWM Control

The MP2209 is a constant frequency peak-current-mode control PWM switching regulator. Refer to the functional block diagram. The high side N-Channel DMOS power switch turns on at the beginning of each clock cycle. The current in the inductor increases until the PWM current comparator trips to turn off the high side DMOS switch. The peak inductor current at which the current comparator shuts off the high side power switch is controlled by the COMP voltage at the output of feedback error amplifier. The transconductance from the COMP voltage to the output current is set at 11.25A/V.

This current-mode control greatly simplifies the feedback compensation design by approximating the switching converter as a single-pole system. Only Type II compensation network is needed, which is integrated into the MP2209. The loop bandwidth is adjusted by changing the upper resistor value of the resistor divider at the FB pin. The internal compensation in the MP2209 simplifies the compensation design, minimizes external component counts, and keeps the flexibility of external compensation for optimal stability and transient response.

### Enable and Frequency Synchronization (EN/SYNC PIN)

This is a dual function input pin. Forcing this pin below 0.4V for longer than 4us shuts down the part; forcing this pin above 1.6V for longer than 4μs turns on the part. Applying a 0.5MHz to 2MHz clock signal to this pin also synchronizes the internal oscillator frequency to the external clock. When the external clock is used, the part turns on after detecting the first few clocks regardless of duty cycles. If any ON or OFF period of the clock is longer than 4μs, the signal will be intercepted as an enable input and disables the synchronization. For automatic start up, connect this pin to $V_{CC}$ with a pull-up resistor; don't apply a voltage more than $V_{CC}$ to this pin.

### Soft-Start and Output Pre-Bias Startup

The soft start time can be adjusted by connecting a capacitor from this pin to ground. When the soft-start period starts, an internal 5μA current source begins charging the external capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V. At this point the reference voltage takes over at the no inverting error amplifier input. The soft-start time can be calculated as follows:

$$t_{SS}(ms) = \frac{0.8V \times C_{SS}(nF)}{5\mu A}$$

If the output of the MP2209 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

### Over Current Protection

The MP2209 offers cycle-to-cycle current limiting for both high-side and low-side switches. The high-side current limit is relatively constant regardless of duty cycles. When the output is shorted to ground, causing the output voltage to drop below 50% of its nominal output, the IC is shut down momentarily and begins discharging the soft start capacitor. It will restart with a full soft-start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

### Power Good Output (POK pin)

The MP2209 includes an open-drain power good output that indicates whether the regulator output is within ±10% of its nominal output. When the output voltage moves outside this range, the POK output is pulled to ground. There is a 30μs deglitch time when POK output change its state. Connect this pin to $V_{CC}$ through a pull-up resistor to get a proper power good output.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

### Bootstrap (BST PIN)

The gate driver for the high-side N-channel DMOS power switch is supplied by a bootstrap capacitor connected between the BS and SW pins. When the low-side switch is on, the capacitor is charged through an internal boost diode. When the high-side switch is off and the high-side switch turns on, the voltage on the bootstrap capacitor is boosted above the input voltage and the internal bootstrap diode prevents the capacitor from discharging.

### Input UVLO

Both VCC and IN pins have input UVLO detection. Until both VCC and IN voltage exceed under voltage lockout threshold, the parts remain in shutdown condition. There are also under voltage lockout hysesteres at both VCC and IN pins.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage (see Figure 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation network (see Figure 1). The relation between R1 and feedback loop bandwidth ($f_C$), output capacitance ($C_O$) is as follows:

$$R1(K\Omega) = \frac{1.24 \times 10^6}{f_C(KHz) \times C_O(uF)}$$

The recommended feedback loop bandwidth ($f_C$) is no higher than 1/10th of switching frequency of MP2209. In the case of ceramic capacitor as $C_O$, it's usually set to be in the range of 30KHz and 50KHz for optimal transient performance and good phase margin. If electrolytic capacitor is used, the recommended loop bandwidth is no higher than 1/4th of the ESR zero frequency ($f_{ESR}$). $f_{ESR}$ is given by:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

For example, choose $f_C$=50KHz with ceramic capacitor, $C_O$=47uF, R1 is estimated to be 523KΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

**Table 1—Resistor Selection vs. Output Voltage Setting**

| VOUT (V) | R1 (kΩ) | R2 (kΩ) | L (μH) | COUT (ceramic) |
|---|---|---|---|---|
| 1.2 | 499 | 1000 | 1μH-4.7μH | 47μF |
| 1.5 | 499 | 562 | 1μH-4.7μH | 47μF |
| 1.8 | 499 | 402 | 1μH-4.7μH | 47μF |
| 3.3 | 499 | 158 | 1μH-4.7μH | 47μF |
| 5 | 499 | 95.3 | 1μH-4.7μH | 47μF |

**Table 2—Suggested Surface Mount Inductors**

| Manufacturer | Part Number | Inductance (μH) | Max DCR (mΩ) | Current Rating (A) | Dimensions L x W x H (mm3) |
|---|---|---|---|---|---|
| TOKO | | | | | |
| | FDA1055-3R3M | 3.3 | 7.3 | 11.7 | 10.8x11.6x5.5 |
| Wurth Electronics | | | | | |
| | 744314330 | 3.3 | 9.6 | 8 | 7x6.9x5 |
| TDK | | | | | |
| | ULF100457-3R3N6R9 | 3.3 | 11.6 | 7.5 | 10x9.7x4.5 |

### Selecting the Inductor

A 1μH to 4.7μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <10mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x \Delta I_L x f_{OSC}}$$

where $\Delta I_L$ is Inductor Ripple Current. Choose inductor ripple current approximately 30% of the maximum load current, 2A. The maximum inductor peak current is

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions, larger inductance is recommended for improved efficiency

### Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 47μF capacitor is sufficient.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

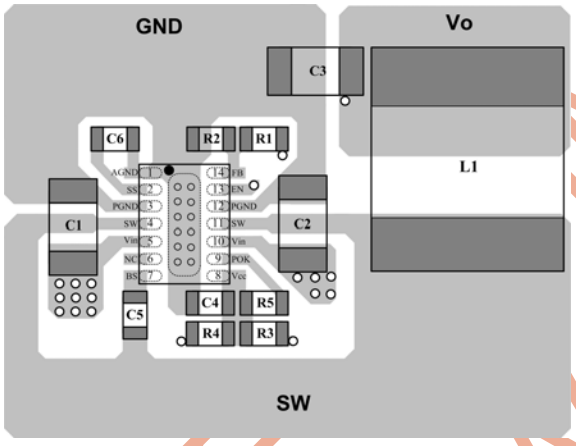
### Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. If electrolytic capacitor is used, pay attention to output ripple voltage, extra heating, and the selection of feedback resistor R1 (refer to "Output Voltage Setting" section) due to large ESR of electrolytic capacitor.

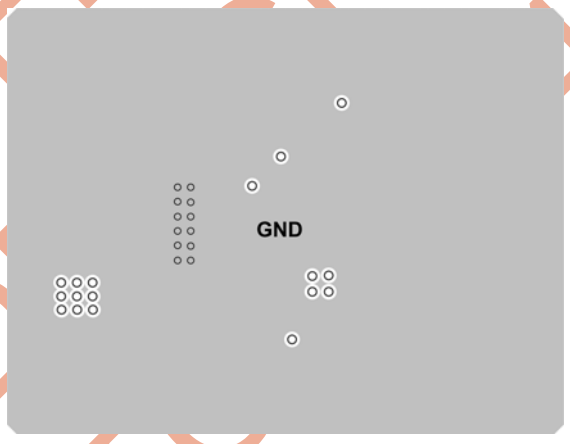
### PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow the guidelines as follows. Here, the typical application circuit is taken as an example to illustrate the layout rules should be followed.

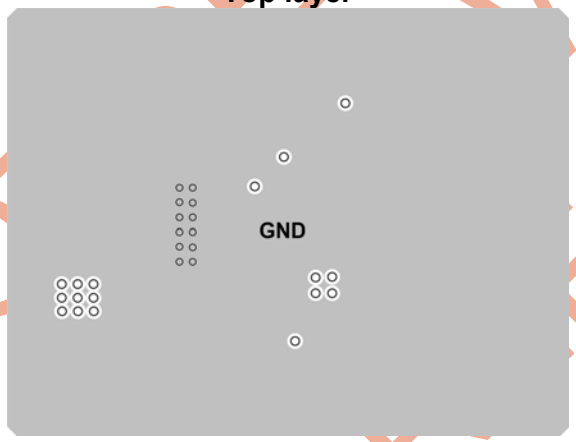
1) For MP2209, a PCB layout with >=4 layers is recommended.
2) The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces.
3) Two input ceramic capacitors (2 x (10μF~22μF)) are strongly recommended to be placed on both sides of the MP2209DL package and keep them as close as possible to the "IN" and "GND" pins.
4) A RC (see the typical application circuit, R4=10Ω, C4=1μF ceramic capacitor) low pass filter is recommended for VCC supply. C4 must be placed as close as possible to "VCC" pin and "GND" pin.
5) The external feedback resistors shall be placed next to the FB pin. Keep the FB trace as short as possible.
6) Keep the switching node SW short and away from the feedback network.



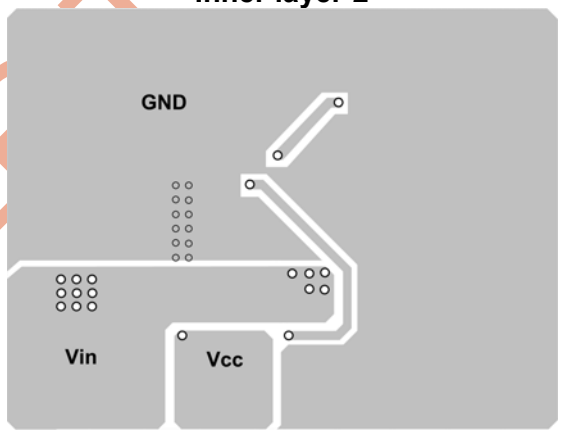

Top layer




Inner layer-2




Inner layer-1




Bottom layer

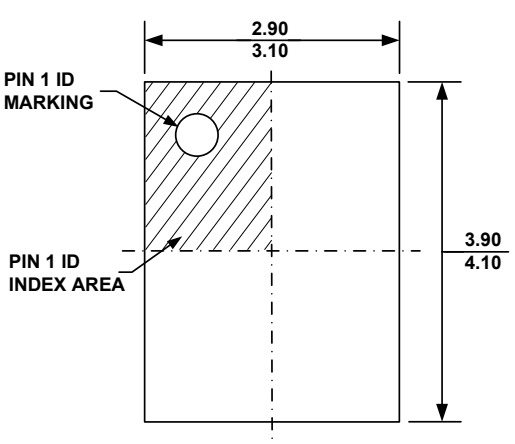
Figure 2—PCB Layout (Four Layers)

NOT RECOMMENDED FOR NEW DESIGNS
OBSOLETE

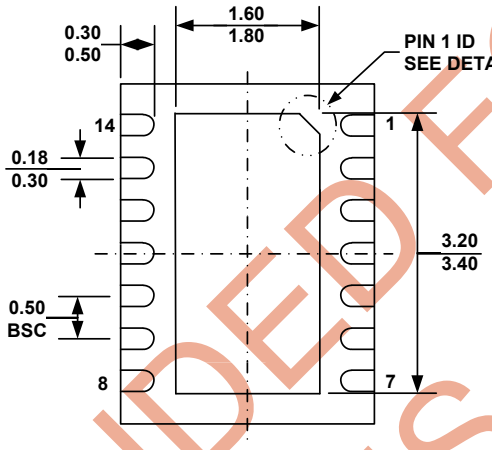

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

## PACKAGE INFORMATION

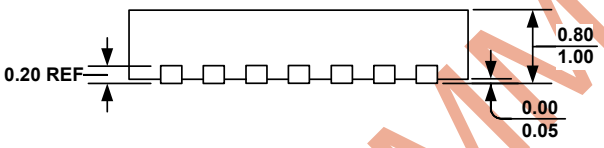
### 3mm x 4mm QFN14



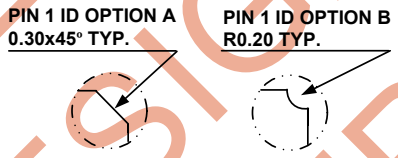

TOP VIEW



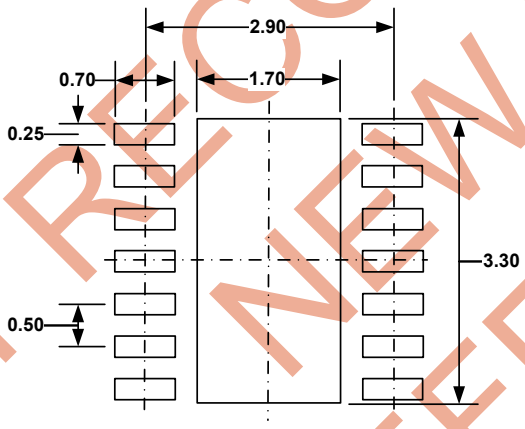

BOTTOM VIEW




SIDE VIEW




DETAIL A




RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1474

**NOTICE:** The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.