MP2125

Dual 1.5A, 1.2MHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2125 is a fully integrated dual PWM step-down converter with built-in internal power MOSFETs. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery, with an input range from 2.7V to 6V. The MP2125 can provide up to 1.5A of load current with output voltage as low as 0.8V for each output. It can also operate at 100% duty cycle for low dropout applications.

With peak current mode control and internal compensation, the MP2125 is stable with ceramic capacitors and small inductors.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

MP2125 is available in the small 14-pin 3mmx4mm QFN package.

FEATURES

- 2.7V-6V Input Operation Range
- Each Output Adjustable from 0.8V to VIN
- 1uA Shutdown Current
- Up to 92% Efficiency
- 100% Duty Cycle for Low Dropout Applications
- Fixed 1.2MHz Frequency
- Stable with Low ESR Output Ceramic Capacitors
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown
- Short Circuit Protection
- Available in 14-pin 3mmx4mm QFN package

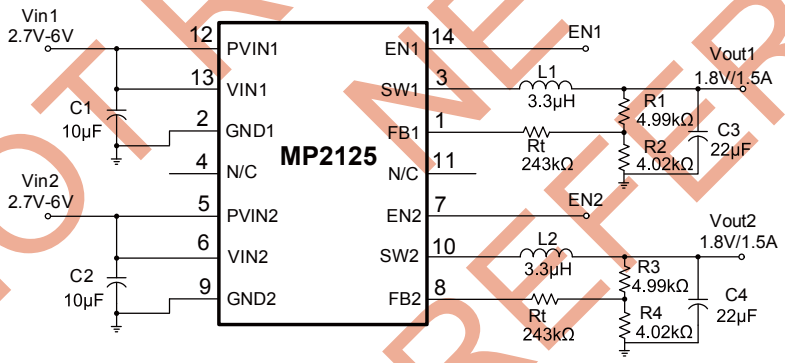
APPLICATIONS

- Solid State Disk
- DVD+/-RW Drivers
- Smart Phones
- PDAs
- Digital Cameras
- Portable Instruments

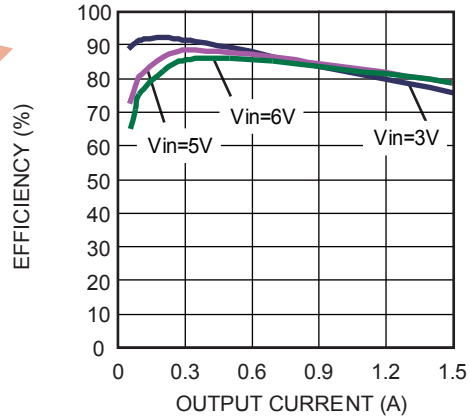
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TYPICAL APPLICATION



Efficiency Curve



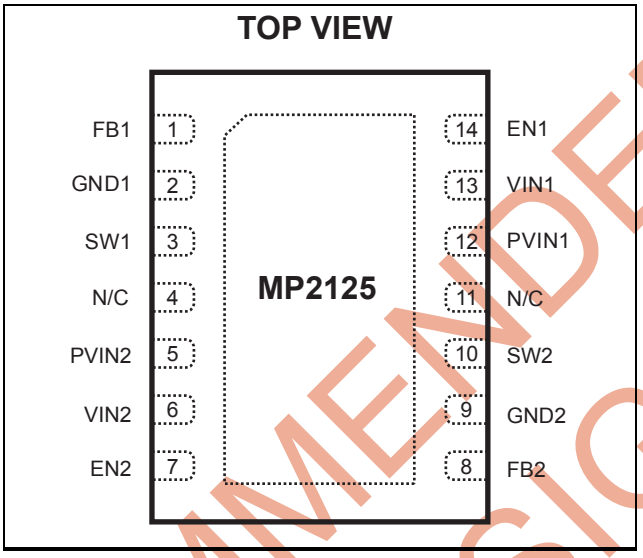
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ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2125DL	QFN14 (3mm x 4mm)	2125	–40°C to +85°C

For Tape & Reel, add suffix –Z (e.g. MP2125DL–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2125DL–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

PIN, VIN to GND .....-0.3V to +6.5V
SW to GND .....-0.3V to V_{IN} + 0.3V
EN, FB to GND .....-0.3V to +6.5V
Operating Temperature.....-40°C to +85°C
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....2.7V to 6V
Operating Junct. Temp (T_J).....-40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN14(3mm X 4mm)	50	12 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (5)

V_{IN} = V_{EN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Condition	Min	Typ	Max	Units
Supply Current	V_{EN}= V_{IN}, V_{FB} = 0.9V		600	750	μA
Shutdown Current	V_{EN}= 0V, V_{IN} = 6V		0.01	1	μA
Thermal Shutdown Trip Threshold	Hysteresis = 20°C		150		°C
EN Trip Threshold	-40°C ≤ T_A ≤ +85°C	0.3	1.0	1.5	V
EN Input Current	V_{EN} = 0V		0.1	1.0	μA
EN Input Current	V_{EN} = 6V		6		μA
IN Undervoltage Lockout Threshold	Rising Edge	2.15	2.40	2.65	V
IN Undervoltage Lockout Hysteresis			160		mV
Regulated FB Voltage	T_A = +25°C	0.784	0.800	0.816	V
	-40°C≤ T_A≤ +85°C	0.776	0.800	0.824	V
FB Input Bias Current	V_{FB} = 0.8V	-50	-2	+50	nA
SW PFET On Resistance	I_{SW} = 100mA		0.25		Ω
SW NFET On Resistance	I_{SW} = -100mA		0.2		Ω
SW Leakage Current	V_{EN}=0V; V_{IN}=6V V_{SW} =0V	-1	0.1	1	μA
SW Leakage Current	V_{EN}=0V; V_{IN}=6V V_{SW} =6V	-5	1.5	5	μA
SW PFET Peak Current Limit	Duty Cycle=100%		3.0		A
Switching Frequency		1.0	1.2	1.4	MHz

Notes:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization

PIN FUNCTIONS

Pin #	Name	Description
1	FB1	Feedback input voltage for channel 1
2	GND1	Ground pin 1
3	SW1	Switch node to the inductor for channel 1
4	N/C	Not connect
5	PVIN2	Channel 2 input supply pin for power FET
6	VIN2	Channel 2 input supply pin for controller
7	EN2	Enable input for channel 2, “High” enables channel 2. EN2 is pulled to GND with 1Meg internal resistor
8	FB2	Feedback input voltage for channel 2
9	GND2	Ground pin 2
10	SW2	Switch node to the inductor for channel 2
11	N/C	Not connect
12	PVIN1	Channel 1 input supply pin for power FET
13	VIN1	Channel 1 input supply pin for controller
14	EN1	Enable input for channel 1, “High” enables channel 1. EN1 is pulled to GND with 1Meg internal resistor

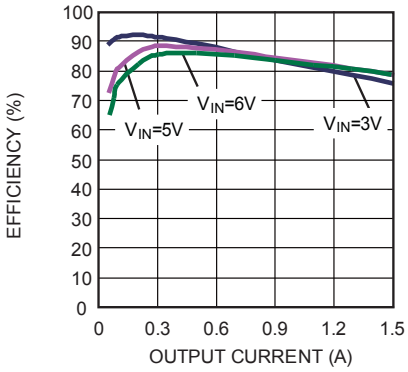
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TYPICAL PERFORMANCE CHARACTERISTICS

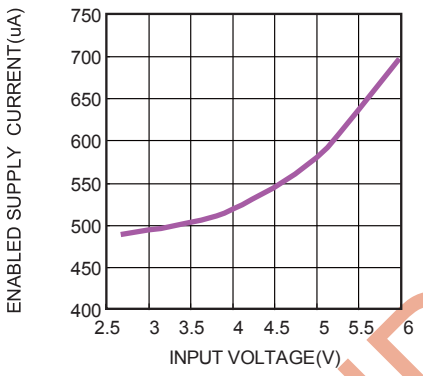
V_{IN} = 5V, V_{OUT} = 1.8V, L=3.3uH, T_A = +25ºC, one channel, unless otherwise noted.

Efficiency Curve



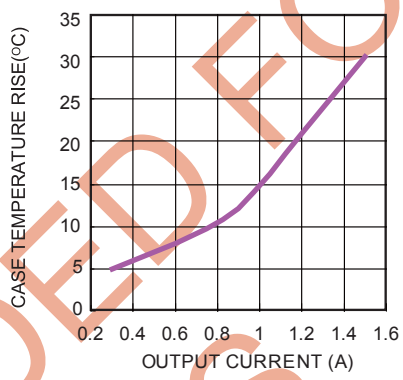
EenableSupply Current vs. Input Voltage

V_{EN}=3V



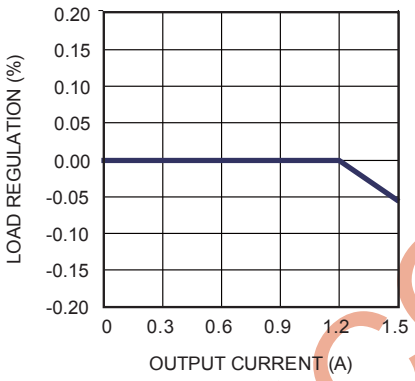
Case Temperature Risevs. Output Current

$I_{OUT}1=I_{OUT}2$



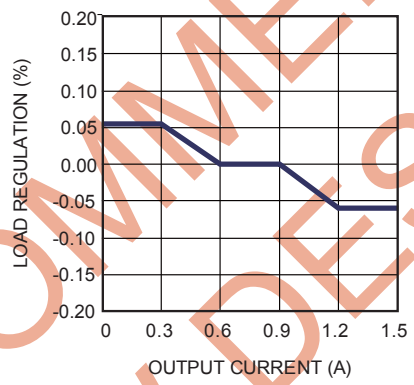
Load Regulation

V_{IN}=3V



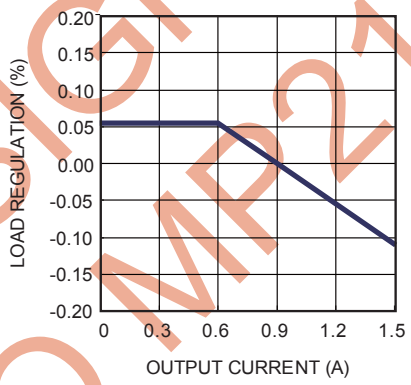
Load Regulation

V_{IN}=5V

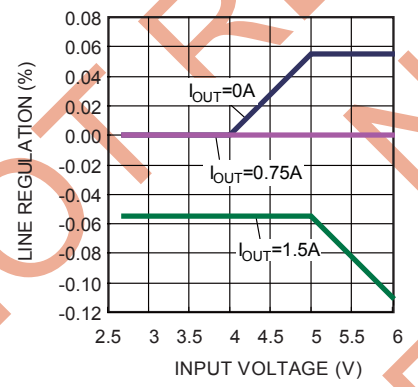


Load Regulation

V_{IN}=6V



Line Regulation



Peak Current vs. Duty Cycle



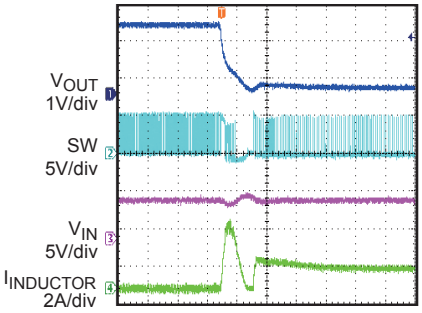
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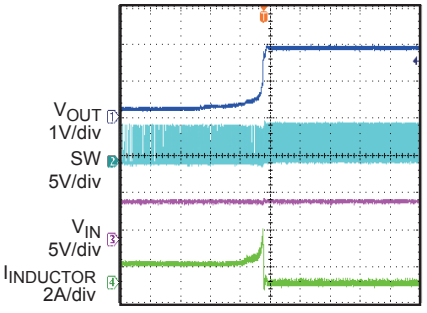
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L=3.3uH, T_A = +25ºC, one channel, unless otherwise noted.

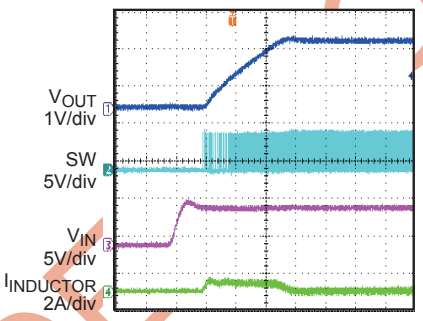
Short Entry



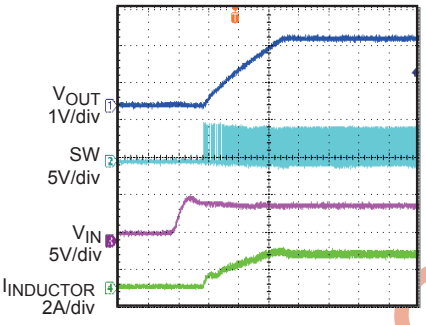
Short Recovery



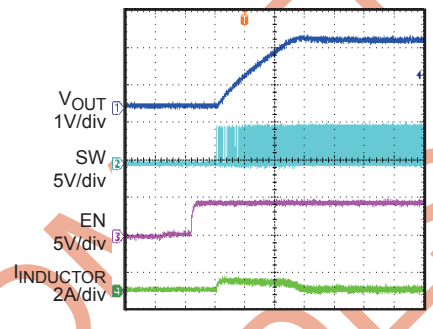
Power Up without Load



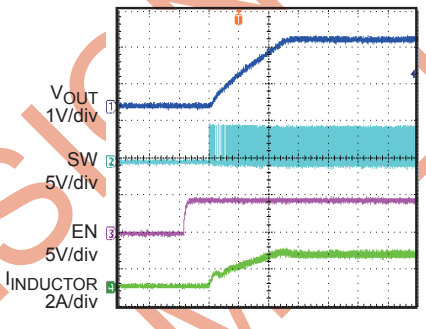
Power Up with Full Load



EN Start Up without Load

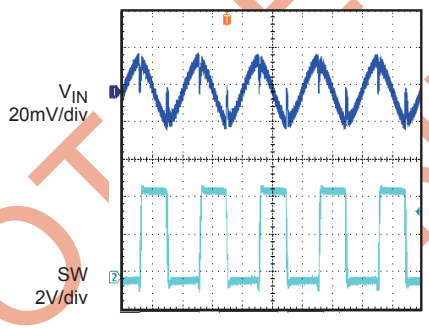


EN Start up with Full Load



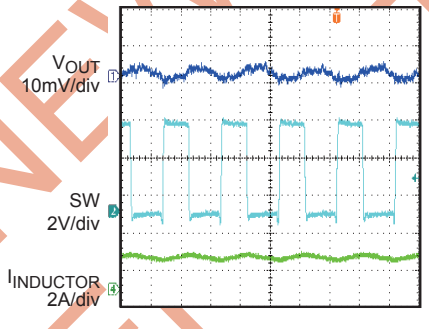
Input Ripple Voltage

I_{OUT}=1.5A



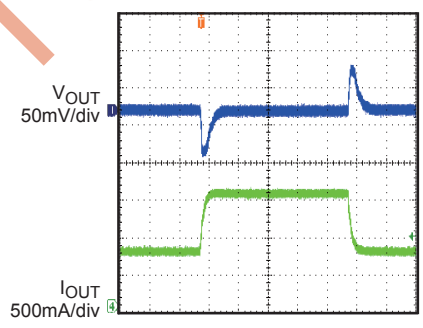
Output Ripple Voltage

I_{OUT}=1.5A



Load Transient Response

Load: 0.75A--1.5A with slew rate 1A/µs



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FUNCTIONAL BLOCK DIAGRAM

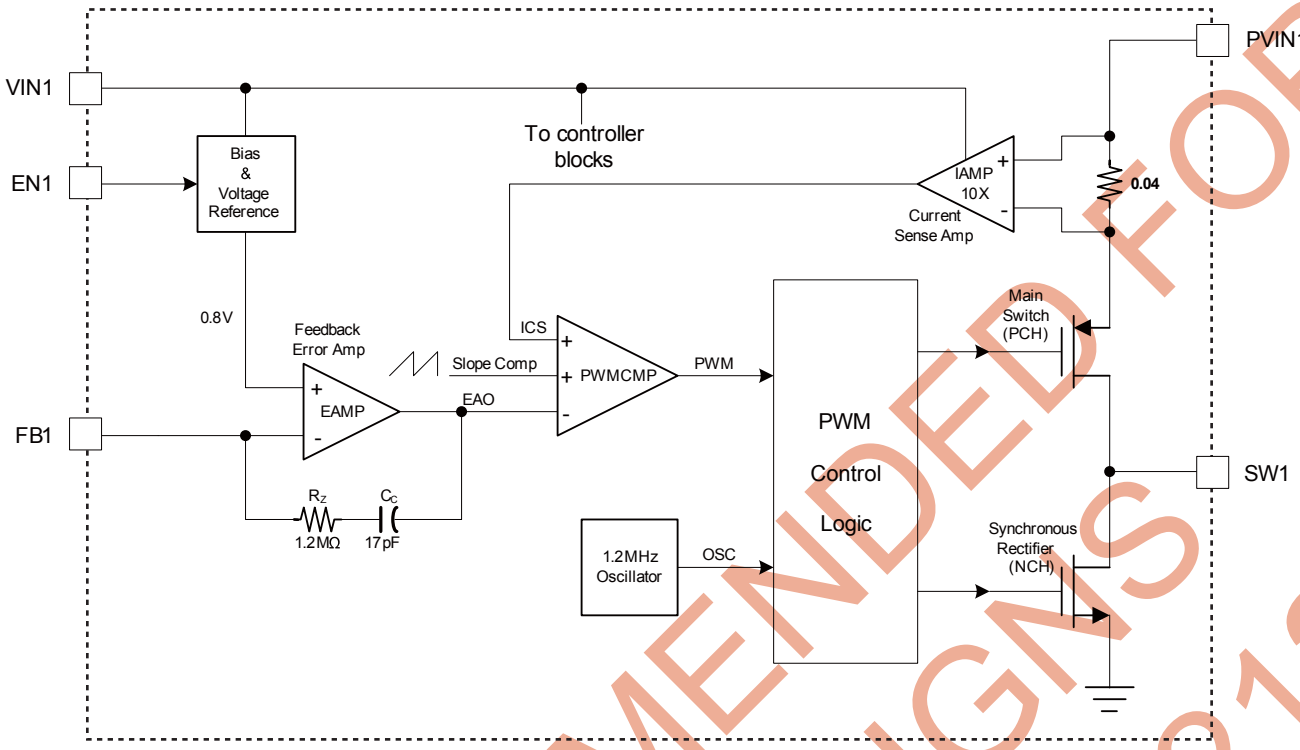


Figure 1 -Functional Block Diagram (1/2 of the MP2125)

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OPERATION

The MP2125 is a dual channel, fixed frequency, current mode step-down converter, optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. MP2125 integrates two high side PFET main switches and two low side synchronous rectifiers. It always operates in continuous conduction mode, simplifies the control scheme and eliminates the random spectrum noise due to discontinuous conduction mode.

The steady state duty cycle D for this mode can be calculated as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time and f_{OSC} is the oscillator frequency (1.2MHz typ.).

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limiting for superior load and line response as well as protection of the internal main switches and synchronous rectifiers. The MP2125 switches at a constant frequency (1.2MHz) and modulates the inductor peak current to regulate the output voltage. Specifically, for each cycle the PWM controller forces the inductor peak current to an internal reference level derived from the feedback error voltage. At normal operation for each channel, the main switch is turned on at each rise edge of the internal oscillator, and remains on for a certain period of time to ramp up the inductor current. As soon as the inductor current reaches the reference level, the main switch is turned off and immediately the synchronous rectifier will be turned on to provide the inductor current. The synchronous rectifier will stay on until the next oscillator cycle.

Dropout Operation

The MP2125 allows the main switch to remain on for more than one switching cycle to increase the duty cycle when the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on

continuously to deliver current to the output up to the PFET current limit. In this case, the output voltage becomes the input voltage minus the voltage drop across the main switch and the inductor.

Maximum Load Current

The MP2125 can operate down to 2.7V input voltage; however the maximum load current decreases at lower input due to a large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases.

Short Circuit Protection

When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage approaches 0.8V.

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APPLICATION INFORMATION

The MP2125 has two channels: channel 1 and channel 2. The following formulates are used for components selection of both channels.

Output Voltage Setting

The external resistor divider sets the output voltage.

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Rt is recommended when output voltage is high, as the Figure 2 shows.

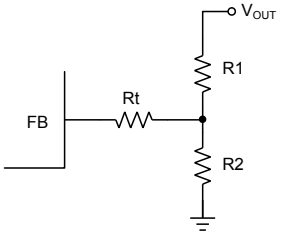


Figure 2—Feedback Network

Table 1 lists the recommended resistor value for common output voltages.

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT}/ V	Rt/ kΩ	R1/ kΩ	R2/ kΩ	L1/ μH	C2/ μF
1.2	300	4.99	10	2.2	22
1.8V	243	4.99	4.02	3.3	22
2.5V	100	121	57.6	3.3	22
3.3V	100	121	39	3.3	22

Inductor Selection

A 1μH to 10μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <200mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor ripple current. Choose inductor ripple current approximately 30% of the maximum load current, 1.5A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 2—Suggested Inductors

Manufacturer	Part Number	Inductance (μH)	Dimensions LxWxH (mm^3)
Toko	D63CB#A916 CY-3R3M	3.3	6.3X6.2X3.5
Cooper	SD25-3R3	3.3	5.2X5.2X2.5
TDK	SLF7045T-3R3M2R5-PF	3.3	7X7X4.5

Input Capacitor C_{IN} Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient.

Output Capacitor C_{OUT} Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. For forced PWM mode operation, the output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \left(R_{ESR} + \frac{1}{8} \cdot \frac{1}{f_{OSC} \cdot C_{OUT}}\right)$$

For most applications, a 22μF capacitor is sufficient.

Thermal Dissipation

Power dissipation shall be considered when operates MP2125 at maximum 1.5A output current. If the junction temperature rises above 150°C, MP2125 will be shut down by internal thermal protection circuitry.

The junction-to-ambient thermal resistance of the 14-pin QFN (3mm x 4mm) $R_{\Theta JA}$ is 50°C/W. The maximum allowable power dissipation is about 1.6W when MP2125 is operating in a 70°C ambient temperature environment:

$$PD_{MAX} = \frac{150^{o}C - 70^{o}C}{50^{o}C/W} = 1.6W$$

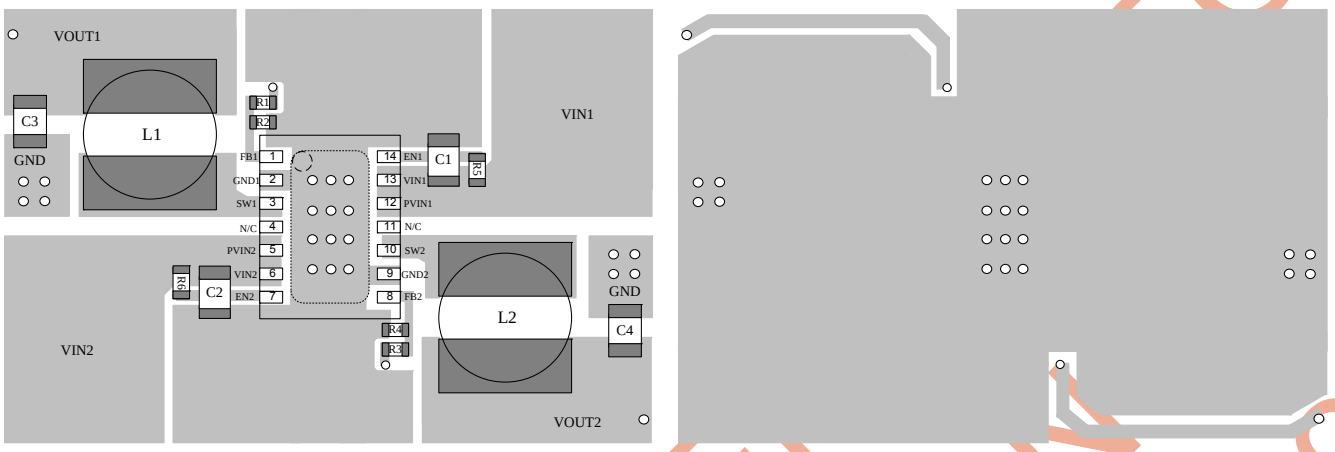
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PCB Layout

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure3 for references.

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. Input capacitors should be placed as close as possible to the respective IN and GND pins. The external feedback resistors shall be placed next to the FB pins. Keep the switching nodes SW short and away from the feedback network.



Top Layer **Bottom Layer**

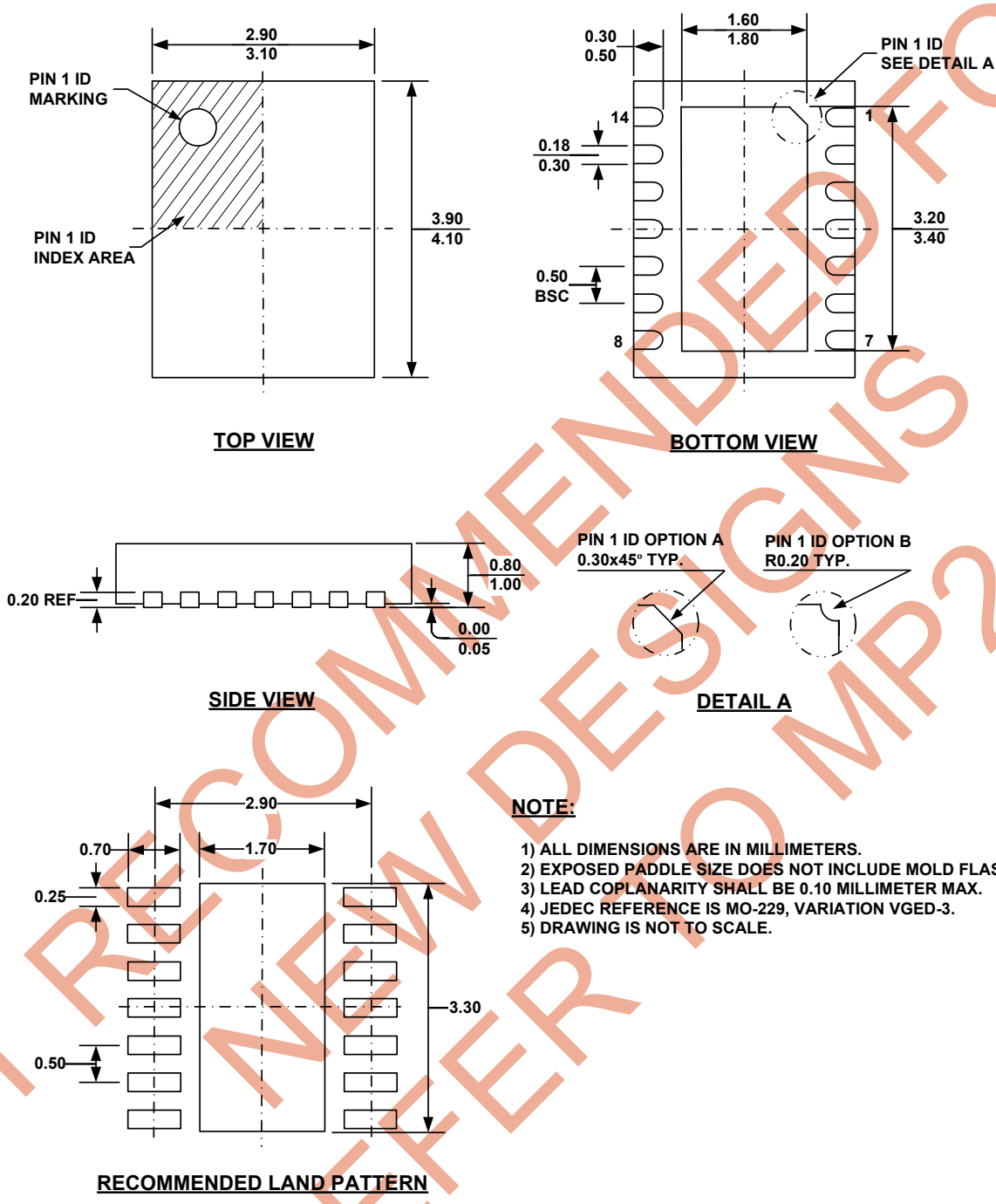
Figure 3 -PCB Layout

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PACKAGE INFORMATION

QFN14 (3mm x 4mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE.

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