MP2119

2A, 6V Synchronous Step-Down Switching Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP2119 is an internally compensated 1.5MHz fixed frequency PWM synchronous step-down regulator. MP2119 operates from a 2.7V to 6V input and generates an output voltage as low as 0.8V.

The MP2119 integrates a 100mΩ high-side switch and a 100mΩ synchronous rectifier for high efficiency without an external Schottky diode. With peak current mode control and internal compensation, the MP2119 based solution delivers a very compact footprint with a minimum component count.

The MP2119 is available in a small 3mm x 3mm QFN package.

FEATURES

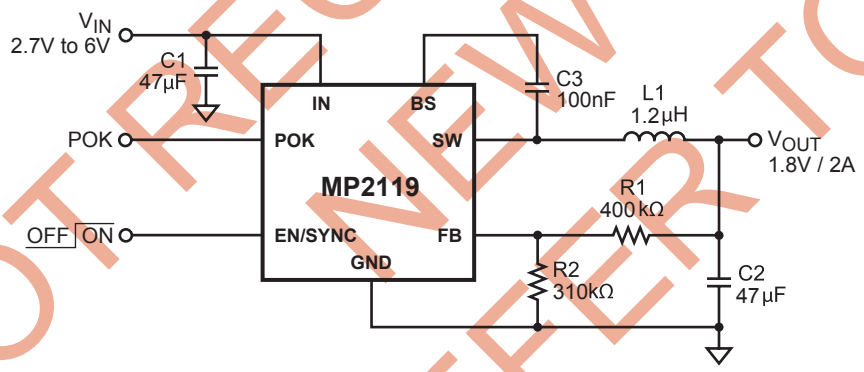
- 2A Output Current
- Input Operation Range: 2.7V to 6V
- All Ceramic Capacitor Design
- 1.5MHz Fixed Switching Frequency
- Adjustable Output from 0.8V to 0.9xV_{IN}
- Internal Soft-Start
- Frequency Synchronization Input
- Power Good Output
- Thermal Shutdown
- Cycle-by-Cycle Current Limiting
- Hiccup Short Circuit Protection
- 3mm x 3mm QFN Package

APPLICATIONS

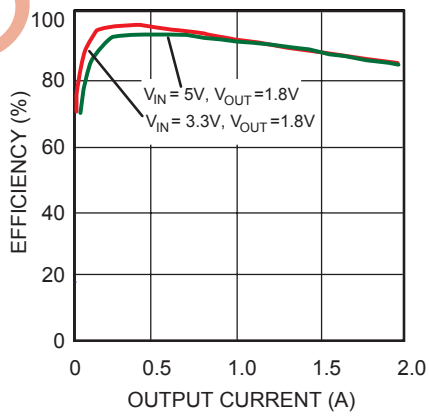
- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Printers and LCD TVs
- Network and Telecom Equipment
- Point of Load Regulators

"MPS" and "The Future of Analog IC Technology" are Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



Efficiency vs. Output Current



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

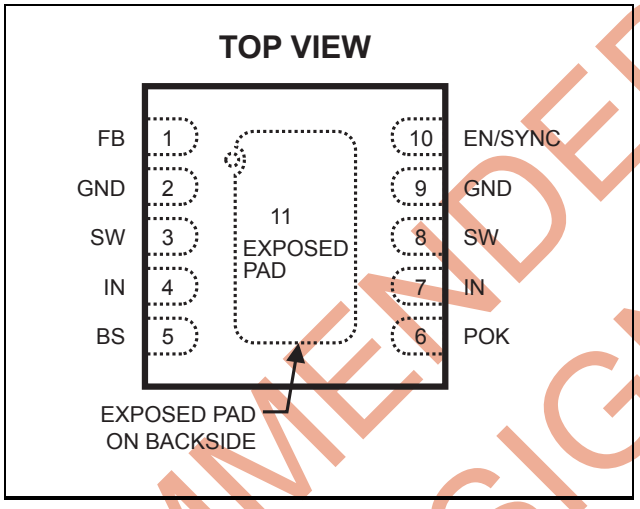
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2119DQ	QFN10 (3mm x 3mm)	U8	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2119DQ–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2119DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN to GND .....-0.3V to +6.5V
SW to GND .....-0.3V to V_{IN} + 0.3V
SW to GND ..... -2.5V to V_{IN}+2.5V for <50nS
FB, EN/SYNC, POK to GND.....-0.3V to +6.5V
BS to SW .....-0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....2.7V to 6V
Output Voltage V_{OUT}.....0.8V to 0.9 x V_{IN}
Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN10 (3mm x 3mm) .....50 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = V_{EN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Condition	Min	Typ	Max	Units
Supply Current	V_{EN} = V_{IN} V_{FB} = 0.85V		750		μA
Shutdown Current	V_{EN} = 0V, V_{IN} = 5V		1		μA
IN Undervoltage Lockout Threshold	Rising Edge		2.59	2.69	V
IN Undervoltage Lockout Hysteresis			210		mV
Regulated FB Voltage	T_A = +25°C	0.776	0.800	0.824	V
FB Input Current	V_{FB} = 0.85V		±50		nA
EN High Threshold	-40°C ≤ T_A ≤ +85°C	1.6			V
EN Low Threshold	-40°C ≤ T_A ≤ +85°C			0.4	V
Internal Soft-Start Time			120		μs
High-Side Switch On-Resistance	I_{SW} = 300mA		100		mΩ
Low-Side Switch On-Resistance	I_{SW} = –300mA		100		mΩ
SW Leakage Current	V_{EN} = 0V; V_{IN} = 5V V_{SW} = 0V or 5V	–10		10	μA
BS Under Voltage Lockout Threshold			1.8		V
High-Side Switch Current Limit	Sourcing	TBD	3.5		A
Low-Side Switch Current Limit	Sinking		3.5		A
Oscillator Frequency		1.2	1.5	1.8	MHz
Maximum Synch Frequency			2		MHz
Minimum Synch Frequency			1		MHz
Minimum On Time			50		ns
Maximum Duty Cycle			90		%
POK Upper Trip Threshold	FB respect to the nominal value		10		%
POK Lower Trip Threshold	FB respect to the nominal value		-10		%
POK Output Voltage Low	I_{SINK} = 5mA			0.4	V
POK Deglitch Timer			30		μs
Thermal Shutdown Threshold	Hysteresis = 20°C		150		°C

Note:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	FB	Feedback. This is the input to the error amplifier. An external resistive divider connects this pin between the output and GND. The voltage on the FB pin compares to the internal 0.8V reference to set the regulation voltage.
2, 9	GND	Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors.
3, 8	SW	Switch Node Connection to the Inductor. These pins connect to the internal high and low-side power MOSFET switches. All SW pins must be connected together externally.
4, 7	IN	Input Supply. A decoupling capacitor to ground is required close to these pins to reduce switching spikes.
5	BS	Bootstrap. A capacitor between this pin and SW provides a floating supply for the high-side gate driver.
6	POK	Open Drain Power Okay Output. “HIGH” output indicates V_{OUT} is within ±10% window. “LOW” output indicates V_{OUT} is out of ±10% window. POK is pulled down in shutdown.
10	EN/SYNC	Enable and Frequency Synchronization Input Pin. Forcing this pin below 0.4V shuts down the part. Forcing this pin above 1.6V turns on the part. Applying a 1MHz to 2MHz clock signal to this pin synchronizes the internal oscillator frequency to the external source.
11	Exposed Pad	Connect exposed pad to ground plane for optimal thermal performance.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MP2162A

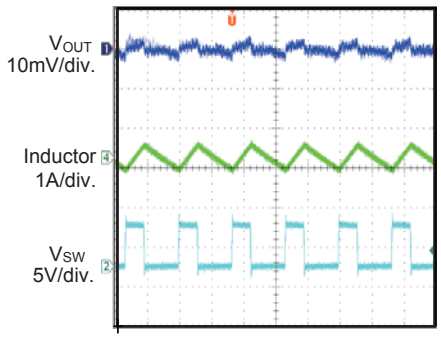
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, T_A = +25°C, unless otherwise noted.

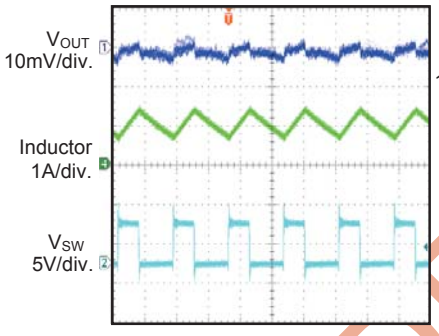
Steady State Operation

No Load



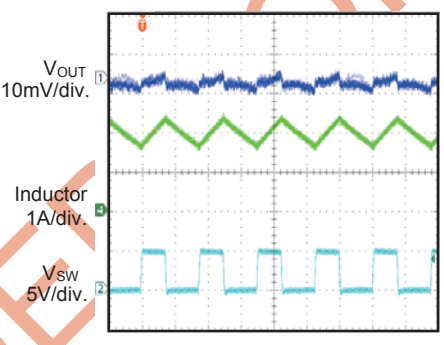
Steady State Operation

Half Load



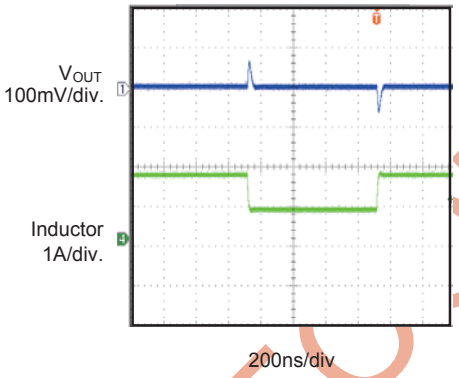
Steady State Operation

Full Load



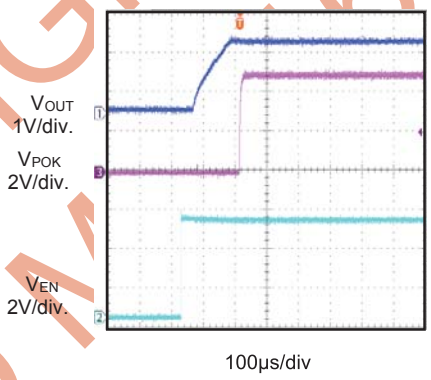
Load Transient

1A-2A Step Resistive Load



Start-up through enable

No Load



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

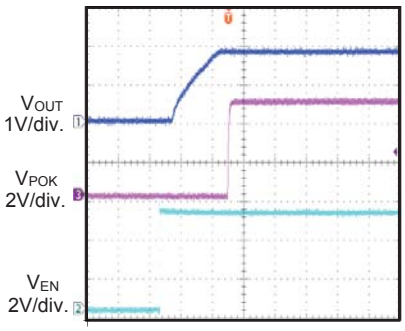
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, T_A = +25°C, unless otherwise noted.

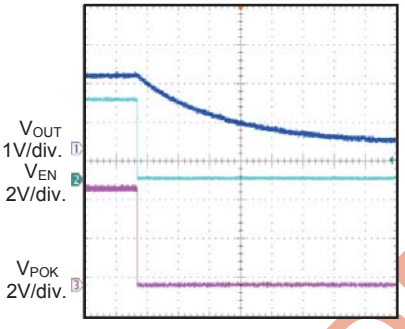
Steady State Operation

Full Load



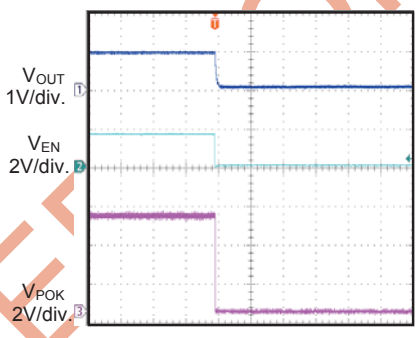
Shut Down through Enable

No Load



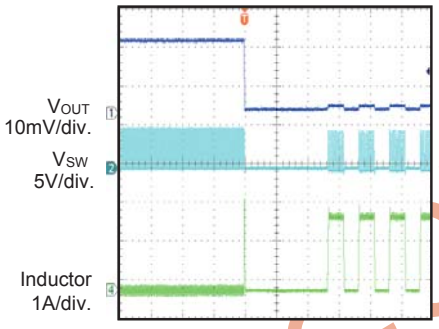
Shut Down through Enable

Full Load



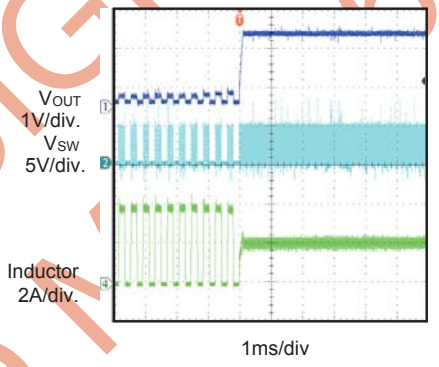
Short Circut Protection

V_{IN}=5V,V_{OUT}=1.8V



Short Circuit Recovery

V_{IN}=5V,V_{OUT}=1.8V



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

FUNCTION BLOCK DIAGRAM

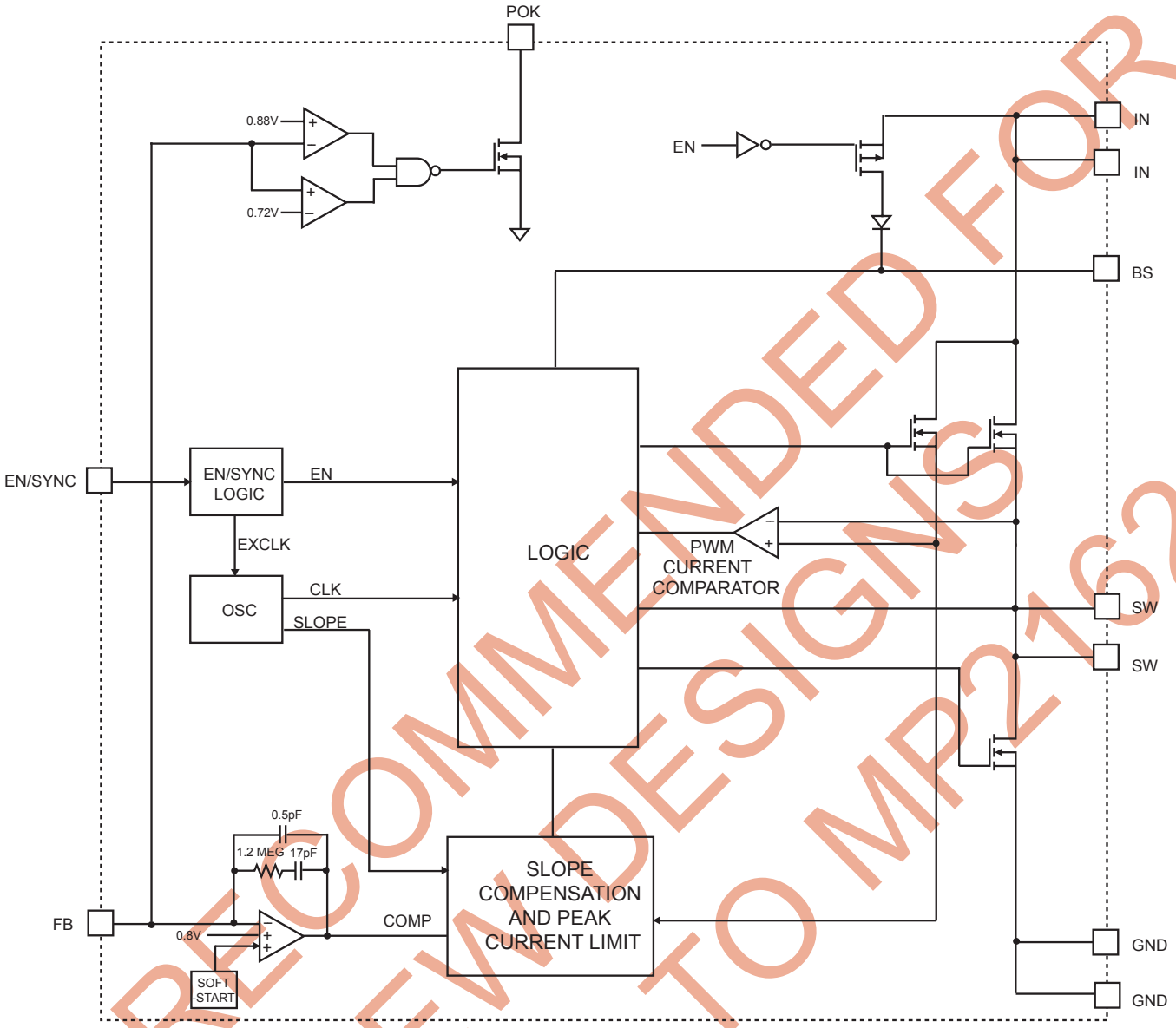


Figure 1—Function Block Diagram

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

FUNCTIONAL DESCRIPTION

PWM Control

The MP2119 is a constant frequency peak-current-mode control PWM switching regulator. Refer to the functional block diagram. The high side N-Channel DMOS power switch turns on at the beginning of each clock cycle. The current in the inductor increases until the PWM current comparator trips to turn off the high side DMOS switch. The peak inductor current at which the current comparator shuts off the high side power switch is controlled by the COMP voltage at the output of feedback error amplifier. The transconductance from the COMP voltage to the output current is set at 11.25A/V.

This current-mode control greatly simplifies the feedback compensation design by approximating the switching converter as a single-pole system. Only Type II compensation network is needed, which is integrated into the MP2119. The loop bandwidth is adjusted by changing the upper resistor value of the resistor divider at the FB pin. The internal compensation in the MP2119 simplifies the compensation design, minimizes external component counts, and keeps the flexibility of external compensation for optimal stability and transient response.

Enable and Frequency Synchronization (EN/SYNC PIN)

This is a dual function input pin. Forcing this pin below 0.4V for longer than 4μs shuts down the part; forcing this pin above 1.6V for longer than 4μs turns on the part. Applying a 1MHz to 2MHz clock signal to this pin also synchronizes the internal oscillator frequency to the external clock. When the external clock is used, the part turns on after detecting the first few clocks regardless of duty cycles. If any ON or OFF period of the clock is longer than 4μs, the signal will be intercepted as an enable input and disables the synchronization.

Soft-Start and Output Pre-Bias Startup

When the soft-start period starts, an internal current source begins charging an internal soft-start capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V.

At this point the reference voltage takes over at the non-inverting error amplifier input. The soft-start time is internally set at 120μs. If the output of the MP2119 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

Over current Protection

The MP2119 offers cycle-to-cycle current limiting for both high-side and low-side switches. The high-side current limit is relatively constant regardless of duty cycles. When the output is shorted to ground, causing the output voltage to drop below 50% of its nominal output, the IC is shut down momentarily and begins discharging the soft start capacitor. It will restart with a full soft-start when the soft- start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Power Good Output (POK PIN)

The MP2119 includes an open-drain Power Good output that indicates whether the regulator output is within ±10% of its nominal output. When the output voltage moves outside this range, the POK output is pulled to ground. There is a 30μs deglitch time when the POK output change its state.

Bootstrap (BST PIN)

The gate driver for the high-side N-channel DMOS power switch is supplied by a bootstrap capacitor connected between the BS and SW pins. When the low-side switch is on, the capacitor is charged through an internal boost diode. When the high-side switch is off and the low-side switch turns on, the voltage on the bootstrap capacitor is boosted above the input voltage and the internal bootstrap diode prevents the capacitor from discharging.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

APPLICATION INFORMATION

Output Voltage Setting

The external resistor divider sets the output voltage (see Page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation (refer to description function). The relation between R1 and feedback loop bandwidth (f_C), output capacitance (C_O) is as following:

$$R1(k\Omega) = \frac{1.24 \times 10^6}{f_C(kHz) \times C_O(uF)}$$

The feedback loop bandwidth (f_C) is no higher than 1/10 of switching frequency of MP2119. In the case of ceramic capacitor as C_O, it's usually set to be in the range of 50kHz and 150kHz for optimal transient performance and good phase margin. If electrolytic capacitor is used, the loop bandwidth is no higher than 1/4 of the ESR zero frequency (f_{ESR}). f_{ESR} is given by:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

For example, choose f_C=70kHz with ceramic capacitor, C_O=47uF, R1 is estimated to be 400kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (ceramic)
1.2	400	806	0.47μH-1μH	47μF
1.5	400	453	0.47μH-1μH	47μF
1.8	400	316	0.47μH-1μH	47μF
2.5	400	187	0.47μH-1μH	47μF
3.3	400	127	0.47μH-1μH	47μF

Inductor Selection

A 0.47μH to 1μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <10mΩ. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is Inductor Ripple Current. Choose inductor ripple current approximately 30% of the maximum load current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions, larger inductance is recommended for improved efficiency.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input source. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 47μF capacitor is sufficient.

Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures a stable regulation loop. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. If electrolytic capacitor is used, pay attention to output ripple voltage, extra heating, and the selection of feedback resistor R1 (refer to "Output Voltage Setting" section) due to large ESR of electrolytic capacitor.

The output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times (ESR + \frac{1}{8 \times f_{OSC} \times C_O})$$

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

External Schottky Diode

For this part, an external schottky diode is recommended to be placed close to "SW" and "GND" pins, especially when the output current is close to 2A.

With the external schottky diode, the voltage spike and negative kick on "SW" pin can be minimized; moreover, the conversion efficiency can also be improved a little.

For the external schottky diode selection, it's noteworthy that the maximum reverse voltage rating of the external diode should be larger than the maximum input voltage. As for the current rating of this diode, 0.5A rating should be sufficient.

PCB Layout

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines as follows. Here, the typical application circuit is taken as an example to illustrate the key layout rules should be followed.

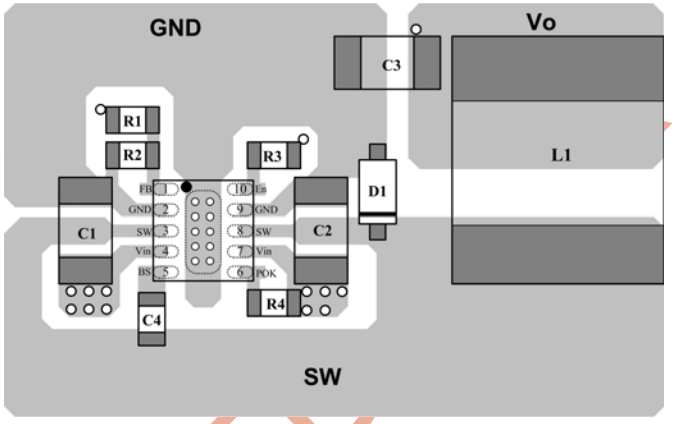
1) For MP2119, a PCB layout with more than (or) four layers is recommended.

2) The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces.

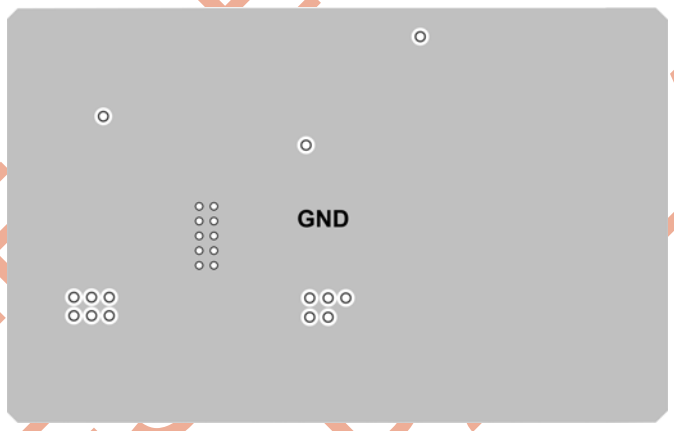
3) For MP2119, two input ceramic capacitors (2 x (10μF~22μF)) are strongly recommended to be placed on both sides of the MP2119 package and keep them as close as possible to the “IN” and “GND” pins. If this placement is not possible, a ceramic cap (10μF~47μF) must be placed across PIN7-“IN”and PIN9-“GND” since the internal Vcc supply is powered from PIN7, and good decoupling is needed to avoid any interference issues.

4) The external feedback resistors shall be placed next to the FB pin. Keep the FB trace as short as possible. Don’t place test points on FB trace if possible.

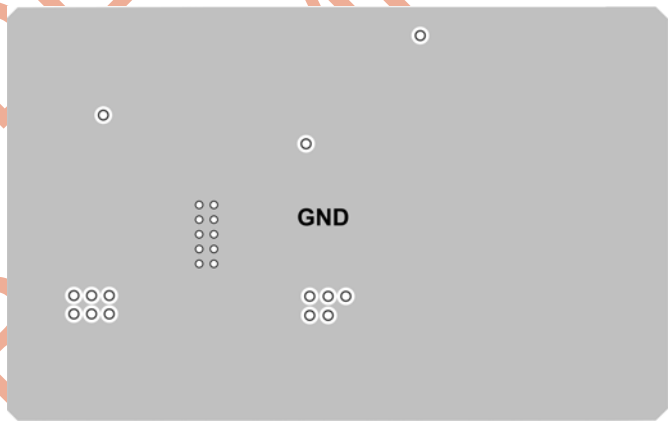
5) Keep the switching node SW short and away from the feedback network.



Top Layer



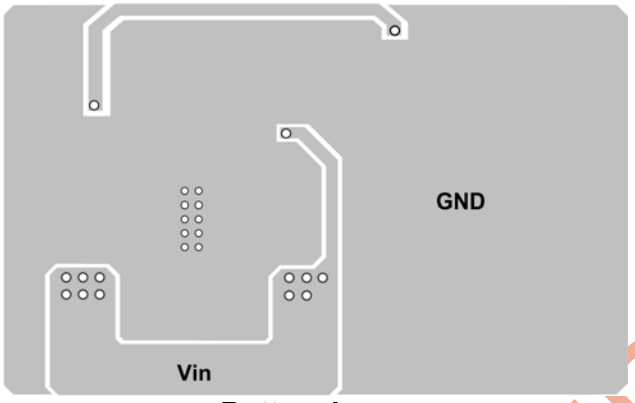
Inner Layer1



Inner Layer2

NOT RECOMMENDED FOR NEW DESIGN, REFER TO MP2119A

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.



Bottom Layer

Figure2—Recommended PCB Layout of MP2119

Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance (µH)	Max DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm3)
Wurth Electronics					
	744310055	0.55	4.5	14	7×6.9×3
	744310095	0.95	7.4	11	7×6.9×3
TOKO					
	B1015AS-1R0N	1	11	6.9	8.4×8.3×4

TYPICAL APPLICATION CIRCUIT

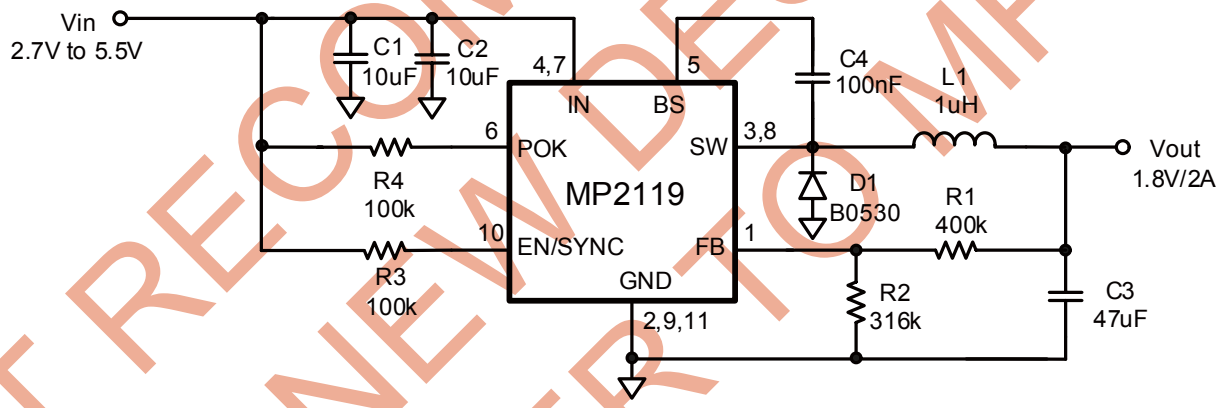


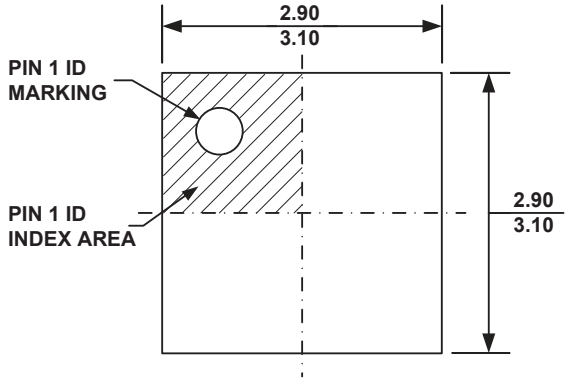
Figure3—Typical Application Circuit of MP2119

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

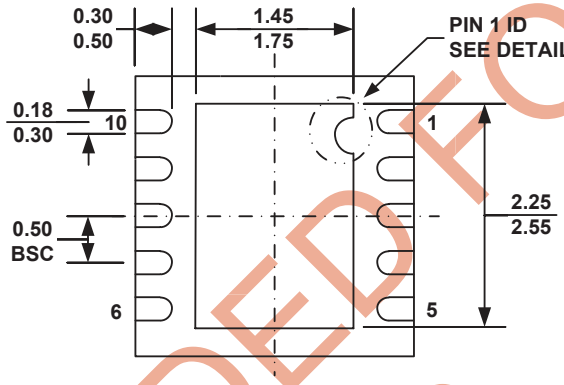
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

PACKAGE INFORMATION

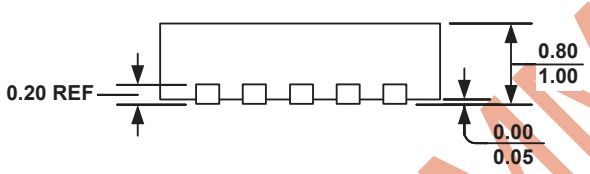
3mm x 3mm QFN10



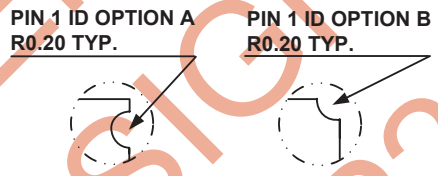
TOP VIEW



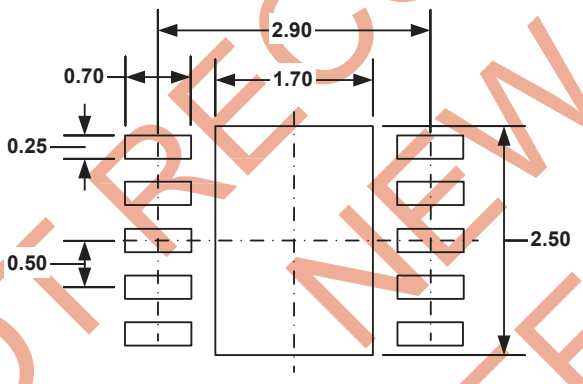
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2162A

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.