# MP2117

## 1.25MHz, 2.2A Synchronous Step-Down Switcher

The Future of Analog IC Technology

## DESCRIPTION

The MP2117 is an internally compensated 2.2A synchronous step-down switcher. The operating frequency is internally set at 1.25MHz. MP2117 is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery. The MP2117 can provide up to 2.2A continuous load current from a 2.5V to 6V input voltage. The output voltage can be regulated as low as 0.6V. 100% duty cycle provides low dropout operation that extends operating time in battery-operated systems.

The MP2117 features an integrated high-side switch and synchronous rectifier for high efficiency. With peak current mode control and internal compensation, the MP2117 can be stabilized with ceramic capacitors and small inductors. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

MP2117 is available in the small 10-pin 3mmx3mm QFN and SOIC-8 packages.

## FEATURES

- 2.2A Output Current
- 2.5V to 6V Input Range $V_{IN}$
- Internal Power MOSFET Switches
- Low Dropout Operation: 100% Duty Cycle
- Up to 90% Efficiency
- Stable with Ceramic Output Capacitors
- 1μA Shutdown Current
- 1.25MHz Switching Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Output Short Circuit Protection
- Internal Soft-start
- Power On Reset Output
- Available in 10-Pin QFN (3mmx3mm) and 8-pin SOIC Packages

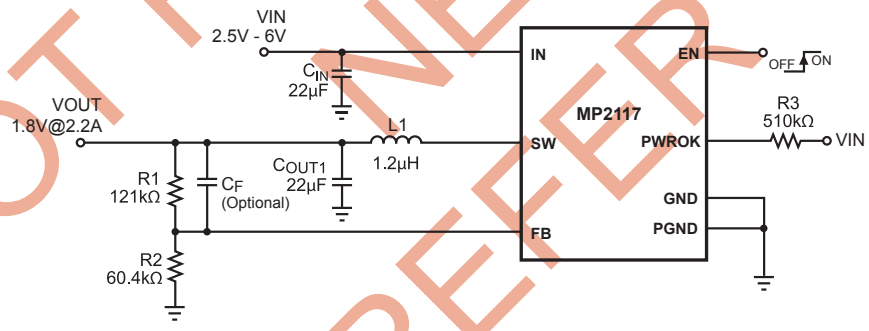
## APPLICATIONS

- DVD+/-RW Drives
- LCD TV
- PDAs
- Portable Instruments

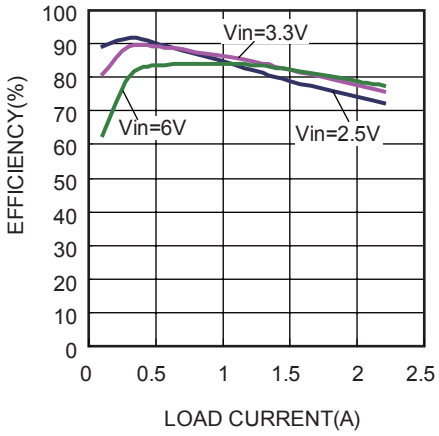
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## TYPICAL APPLICATION




**Efficiency vs. Load Current**





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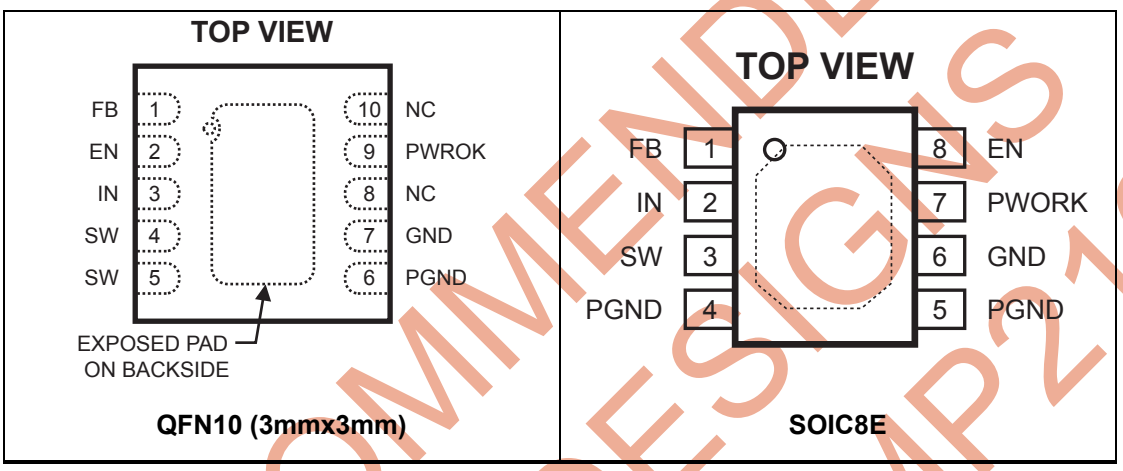
## ORDERING INFORMATION

| Part Number* | Package | Top Marking | Temperature |
|---|---|---|---|
| MP2117DQ | QFN10 (3mmx3mm) | S4 | –40°C to +85°C |
| **Part Number**** | **Package** | **Top Marking** | **Temperature** |
| MP2117DN | SOIC8E | MP2117DN | –40°C to +85°C |

*For Tape & Reel, add suffix –Z (eg. MP2117DQ–Z): For RoHS compliant packaging, add suffix –LF (eg. MP2117DQ–LF–Z). CONTACT FACTORY

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## PACKAGE REFERENCE




## ABSOLUTE MAXIMUM RATINGS (1)

IN to GND .....–0.3V to + 6.5V
SW to GND .....–0.3V to $V_{IN}$ + 0.3V
.....($V_{SW}$ >-2.5V, Transient <50ns ; $V_{SW}$<+8.5V, Transient <50ns)
PWROK to GND .....–0.3V to +6.5V
FB, EN to GND .....–0.3V to +6.5V
Operating Temperature..... –40°C to +85°C
Continuous Power Dissipation ($T_A$ = +25°C) (2)
SOIC8E..... 2.5W
QFN10 (3mm x 3mm) ..... 2.5W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature ..... –65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ .....2.5V to 6V
Output Voltage $V_{OUT}$.....0.6V to 6V
Operating Temperature..... –40°C to +85°C

## *Thermal Resistance* (4)

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| QFN10 (3mm x 3mm) | 50 | 12 | °C/W |
| SOIC8E | 50 | 10 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD5 1-7, 4-layer PCB.

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## ELECTRICAL CHARACTERISTICS (5)

**$V_{IN}$ = $V_{EN}$ = 3.6V, $T_A$ = +25°C, unless otherwise noted.**

| Parameters | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| No Load Supply Current | $V_{IN}$ = 3.6V, $V_{EN}$=3.6V<br>$V_{FB}$ = 0.65V | | 350 | 500 | μA |
| Shutdown Current | $V_{EN}$ = 0V, $V_{IN}$ = 6V | | 0.01 | 1 | μA |
| Thermal Shutdown Trip Threshold | Hysteresis = 20°C | | 150 | | °C |
| PWROK Upper Trip Threshold | FB with respect to the Nominal Value | | 10 | | % |
| PWROK Lower Trip Threshold | FB with respect to the Nominal Value | | –10 | | % |
| PWROK Output Lower Voltage | $I_{SINK}$ = 5mA | | | 0.3 | V |
| PWROK Deglitch Timer | | | 50 | | μs |
| EN Trip Threshold | –40°C ≤ $T_A$ ≤ +85°C | 0.3 | | 1.5 | V |
| EN Pull Down Resistor | | | 1 | | MΩ |
| IN Under Voltage Lockout Threshold | Rising Edge, Hysteresis=0.3V | 1.8 | 2.2 | | V |
| Regulated FB Voltage | $T_A$ = +25°C | 0.584 | 0.596 | 0.608 | V |
| | –40°C ≤ $T_A$ ≤ +85°C | 0.578 | 0.596 | 0.614 | |
| FB Input Bias Current | $V_{FB}$ = 0.62V | –50 | | +50 | nA |
| SW PFET On Resistance | $I_{SW}$ = 100mA | | 0.20 | | Ω |
| SW NFET On Resistance | $I_{SW}$ = –100mA | | 0.15 | | Ω |
| SW Leakage Current | $V_{EN}$ = 0V, $V_{IN}$ = 6V<br>$V_{SW}$ = 0V or 6V | –5 | | +5 | μA |
| SW PFET Peak Current Limit | Duty Cycle = 100%,<br>Current Pulse Width < 1ms | | 3.3 | | A |
| Oscillator Frequency | | 1.00 | 1.25 | 1.50 | MHz |

**Notes:**

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

## PIN FUNCTIONS

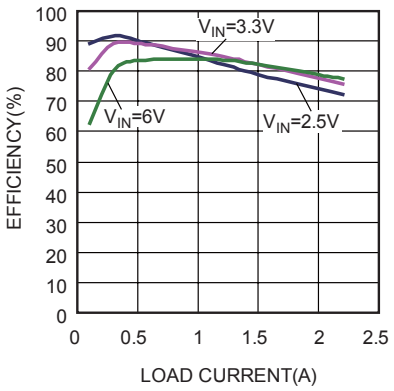
| QFN Pin # | SOIC Pin # | Name | Description |
|---|---|---|---|
| 1 | 1 | FB | Feedback Input for the switcher output VOUT. |
| 2 | 8 | EN | Enable Input for the switcher. |
| 3 | 2 | IN | Input Supply Pin. |
| 4, 5 | 3 | SW | Switcher switch node. |
| 6 | 4, 5 | PGND | Low Side Synchronous Rectifier Switch Power Ground. |
| 7 | 6 | GND | Chip Analog Ground. Connect the Exposed Pad to GND. |
| 9 | 7 | PWROK | Power On Reset Open Drain Output. HIGH output indicates that the output is within ±10% of the regulation value. LOW output indicates that the output is out of ±10% window. PWROK is pulled down in shutdown. The PWROK window comparators have 50us deglitch timer to avoid false trigger during load transient. |
| 8, 10 | - | N/C | No Connection. |

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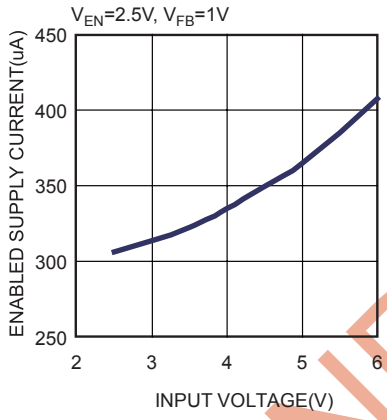
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, L=1.2uH, $T_A$ = +25ºC, unless otherwise noted.**

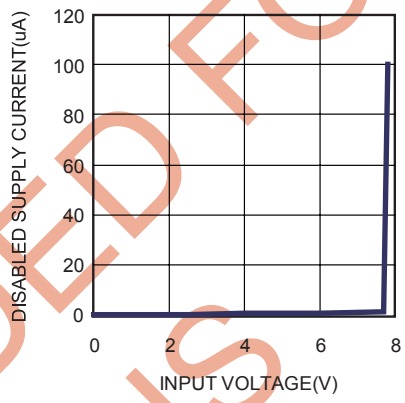
### Efficiency vs. Load Current



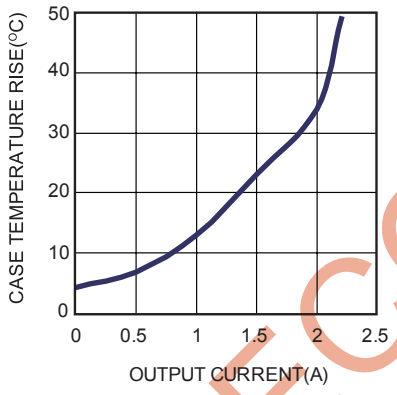

### Enabled Supply Current vs. Input Voltage



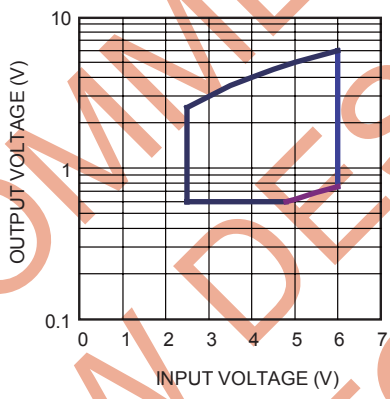

### Disabled Supply Current vs. Input Voltage



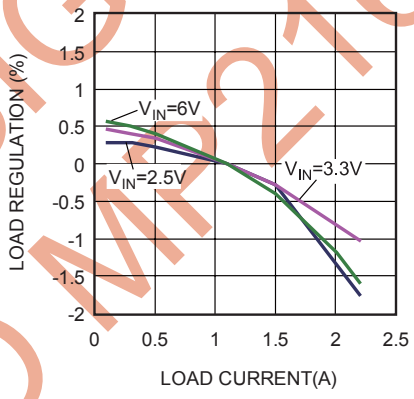

### Case Temperature Rise vs. Output Current



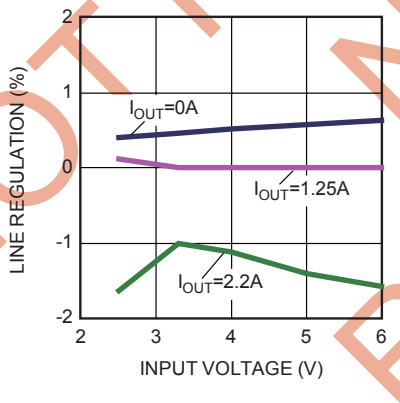

### Operating Range




### Load Regulation




### Line Regulation

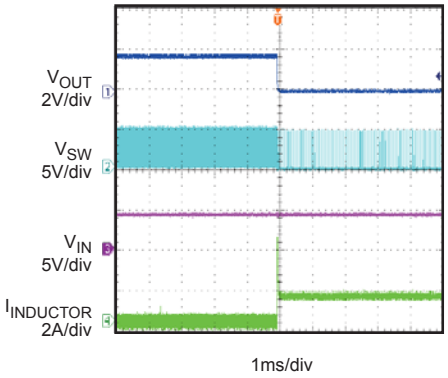



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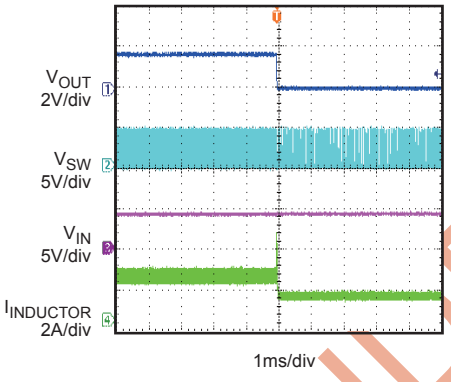
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, L=1.2uH, $T_A$ = +25ºC, unless otherwise noted.**

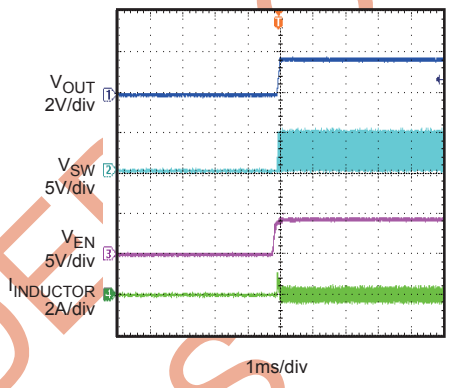
### Output Short Entry
$I_O$=0A



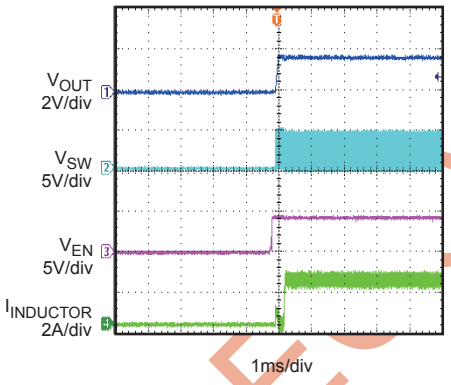

### Output Short Entry
$I_O$=2.2A



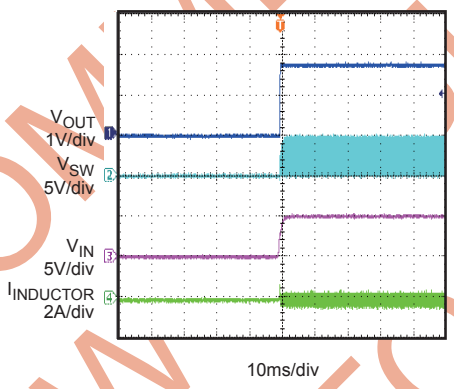

### Enable Startup
$I_O$=0A



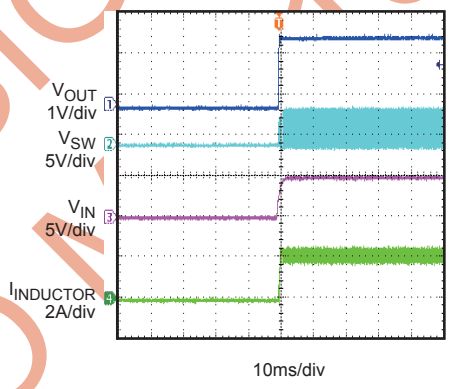

### Enable Startup
$I_O$=2.2A



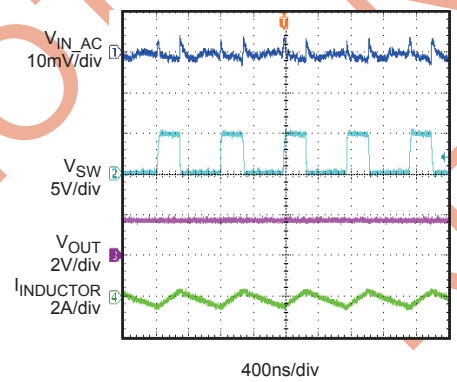

### Power Up
$I_O$=0A



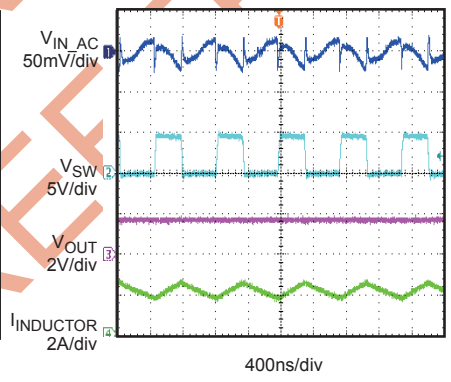

### Power Up
$I_O$=2.2A



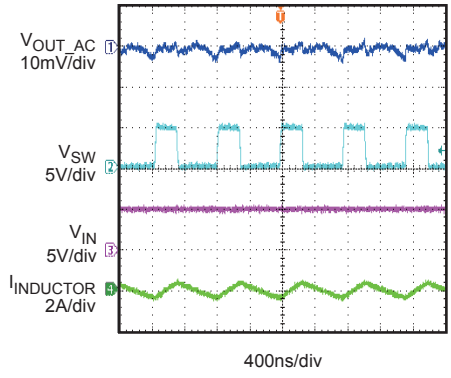

### Input Ripple Voltage
$I_O$=0A




### Input Ripple Voltage
$I_O$=2.2A




### Output Ripple Voltage
$I_O$=0A



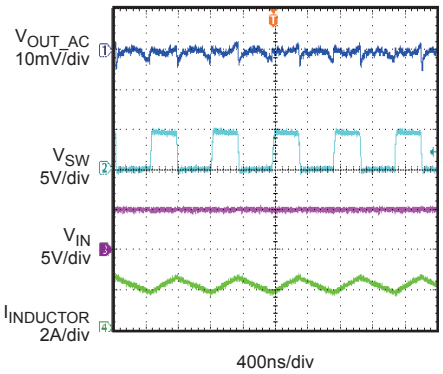

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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, L=1.2uH, $T_A$ = +25ºC, unless otherwise noted.**

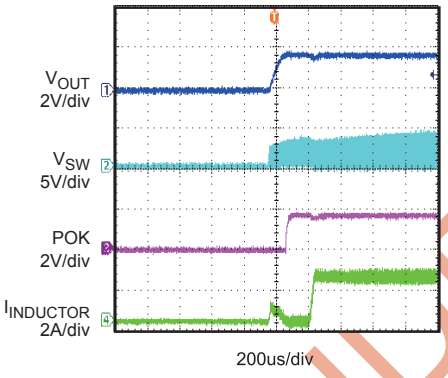
**Output Ripple Voltage**

$I_O$=2.2A



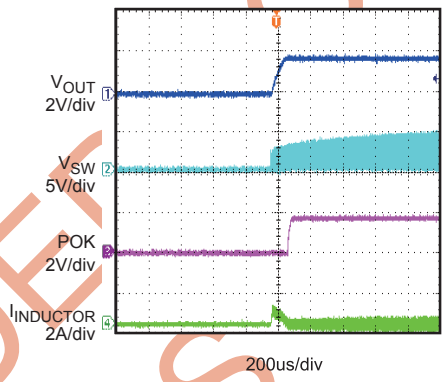

**Power OK Response**

$I_O$=2.2A




**Power OK Response**

$I_O$=0A




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## OPERATION

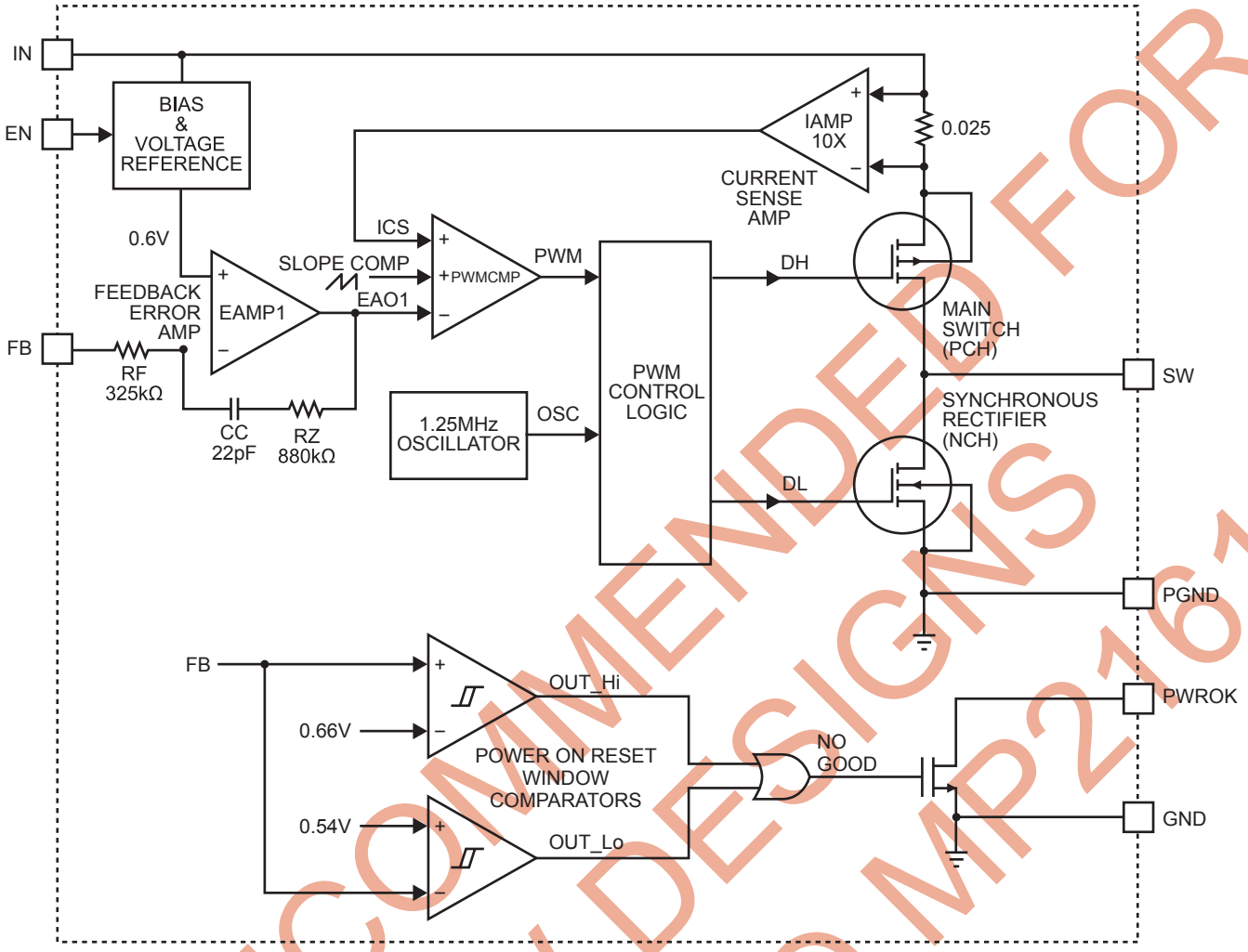



**Figure 1—Functional Block Diagram**

The MP2117 is a 1.25MHz fixed frequency current mode synchronous step-down switcher. The MP2117 is optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. The MP2117 can provide up to 2.2A continuous load current from a 2.5V to 6V input voltage.

The MP2117 uses an external resistor divider to set the switcher output voltage from 0.6V to 6V.

### 2.2A Step-Down Switcher

The switcher integrates both a main switch and a synchronous rectifier, which provides high efficiency and eliminates an external Schottky diode.

The duty cycle D of a step-down switcher is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where $T_{ON}$ is the main switch on time and $f_{OSC}$ is the oscillator frequency (1.25MHz).

### Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limiting for superior load and line response in addition to protection of the internal main switch and synchronous rectifier. The MP2117 switches at a constant frequency (1.25MHz) and regulates the output voltage. During each cycle the PWM comparator

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modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until the next cycle starts.

**Dropout Operation**

The MP2117 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the PFET current limit. The output voltage then becomes the input voltage minus the voltage drop across the main switch and the inductor.

**Short Circuit Protection**

When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

**Maximum Load Current**

The MP2117 can operate down to 2.5V input voltage; however the maximum load current decreases at lower input due to a large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases.

**Power OK**

The MP2117 provides an open-drain PWROK output that goes high after the output reaches regulation during startup. PWROK goes low after the output goes out of regulation by ±10% or when device enters shutdown. There is 50μsec deglitch timer built in to avoid PWROK false triggered during load transient.

**Enable Control**

MP2117 has a dedicated Enable control pin. By pulling it to high or low, the IC can be enabled and disabled by EN. Tie EN to VIN by proper voltage divider for automatic start up as Figure 2 shows. And make sure that:

$$\text{Max. EN Threshold} < V_{IN} \times \frac{R_{EN2}}{(R_{EN1} + R_{EN2})} < 6V$$

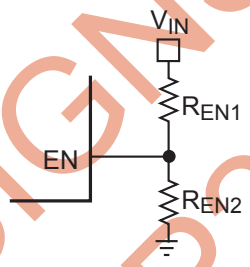



**Figure 2**

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## APPLICATION INFORMATION

### Output Voltage Setting

The external resistor divider sets the output voltage. It is optional to speed loop response by adding a small feedforward capacitor $C_F$ parallel with R1. Choose R1*$C_F$ time constant around 3usec.

Choose R2 value between 1kΩ and 100kΩ. R1 is then given by:

$$R1 = R2 \times (\frac{V_{OUT}}{0.6V} - 1)$$

**Table 1—Resistor Selection vs. Output Voltage Setting**

| $V_{OUT}$ | R1 | R2 |
|---|---|---|
| 1.2V | 60.4kΩ | 60.4kΩ |
| 1.5V | 90.9kΩ | 60.4kΩ |
| 1.8V | 121kΩ | 60.4kΩ |
| 2.5V | 191kΩ | 60.4kΩ) |
| 3.3V | 274KΩ | 60.4kΩ |

### Inductor Selection

A 1μH to 10μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance should be <100mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where $\Delta I_L$ is inductor ripple current. Choose inductor ripple current approximately 30% of the maximum load current, 2.2A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

**Table 2—Suggested Surface Mount Inductors**

| Manufacturer | Part Number | Inductance (μH) | Max DCR (mΩ) | Saturation Current (A) |
|---|---|---|---|---|
| Wurth | 7447745012 | 1.2 | 17 | 4.6 |
| Toko | D62LCB-#A918CY-1R0M | 1.0 | 17 | 3.7 |

### Switcher Input Capacitor $C_{IN1}$ Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF~22μF capacitor is sufficient.

### Switcher Output Capacitor $C_{OUT1}$ Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. For most applications, a 22μF~47μF capacitor is sufficient.

The output ripple $\Delta V_{OUT}$ is approximately:

$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left( ESR \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right)$$

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## Thermal Dissipation

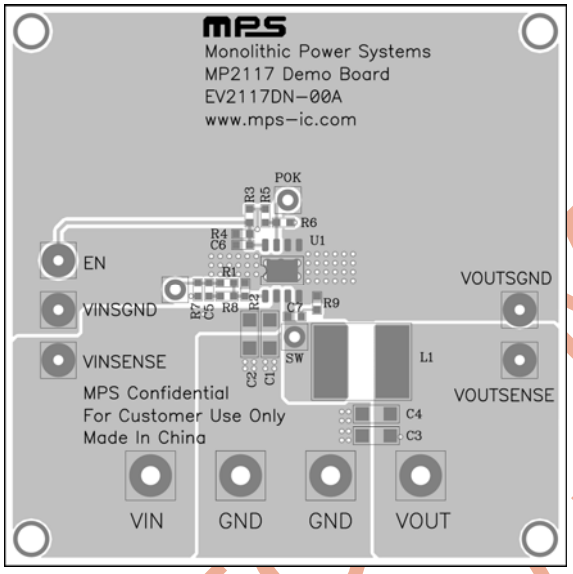
Power dissipation should be considered when MP2117 provide maximum 2.2A output current to the loads at high ambient temperature. If the junction temperature rises above 150°C, the MP2117 will be shut down.

The junction-to-ambient thermal resistance of the 10-pin QFN or 8-pin SOIC $R_{\Theta JA}$ is 50°C/W. The maximum power dissipation is about 1.6W when the MP2117 is operating in a 70°C ambient temperature environment.

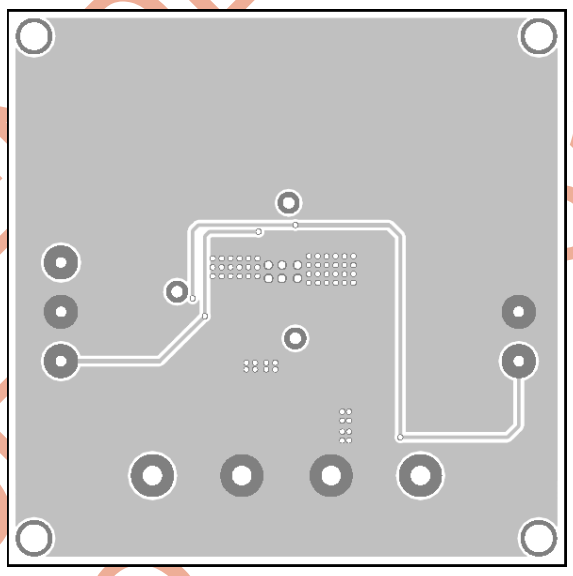
$$PD_{MAX} = \frac{150^{o}C - 70^{o}C}{50^{o}C/W} = 1.6W$$

## PCB Layout

The high current paths (GND, IN, OUT and SW) should be placed very close to the device with short, direct and wide traces. Input capacitors should be placed as close as possible to the respective IN and PGND pins. The external feedback resistors should be placed next to the FB pins. Keep the switching nodes SW short and away from the feedback network. An external diode (i.e. B130) can be added between SW and GND to reduce switching noise and to improve the load regulation. The reference layout and its schematic are shown below:




**Top Layer**



**Bottom Layer**

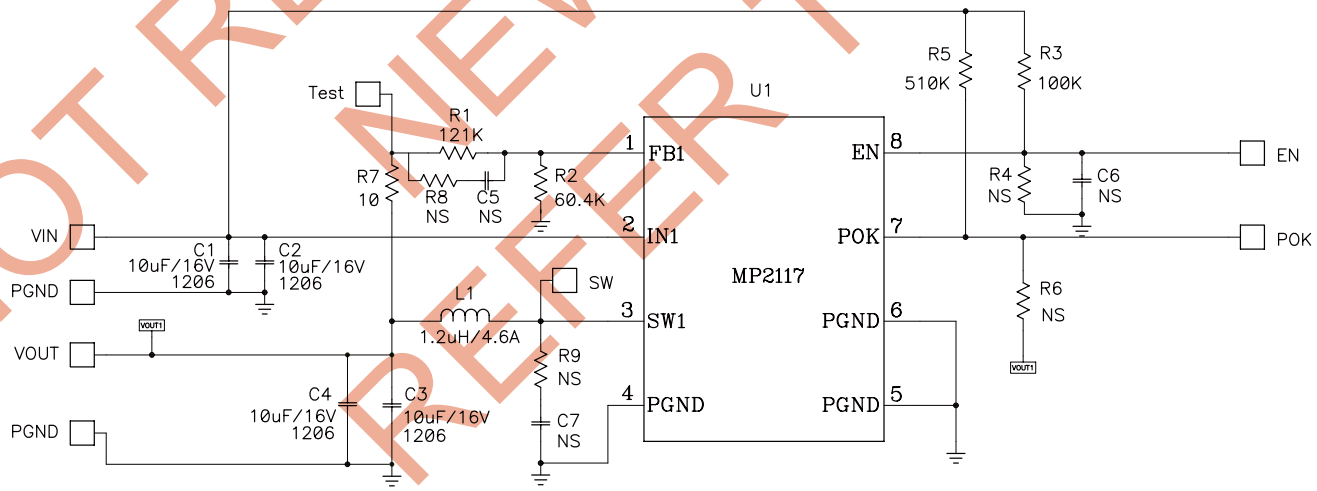


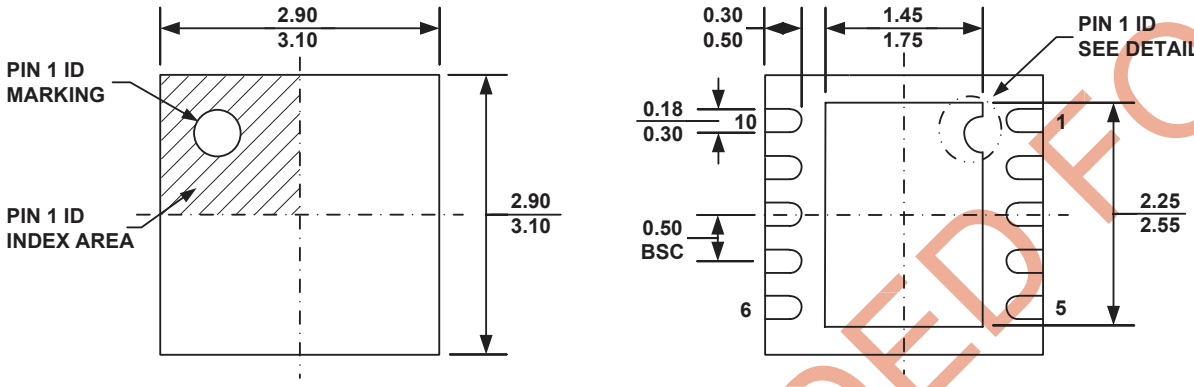

**Figure 3**

NOT RECOMMENDED FOR NEW DESIGN REFER TO MP2117A


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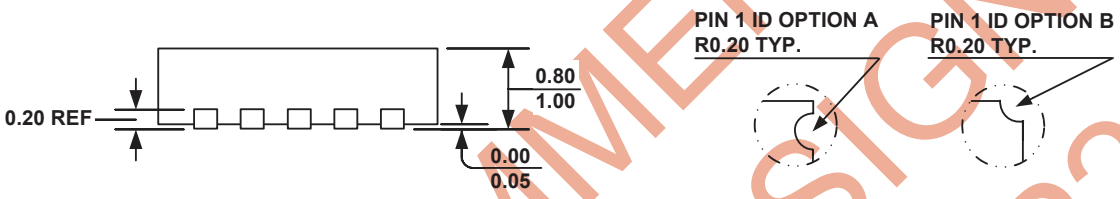
## PACKAGE INFORMATION

### QFN10 (3X3)



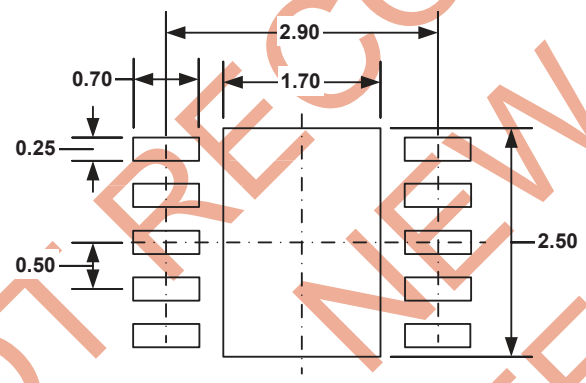

TOP VIEW

BOTTOM VIEW




SIDE VIEW

DETAIL A




RECOMMENDED LAND PATTERN

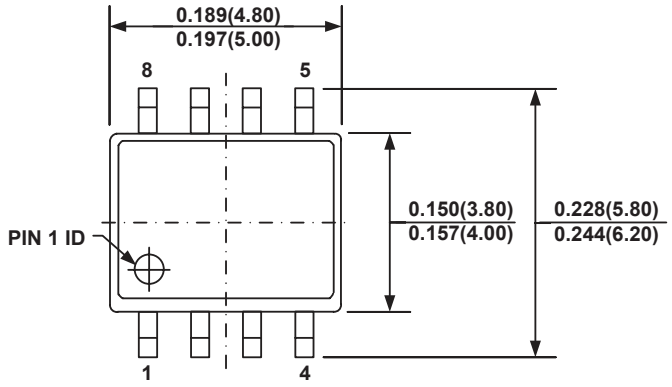
**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

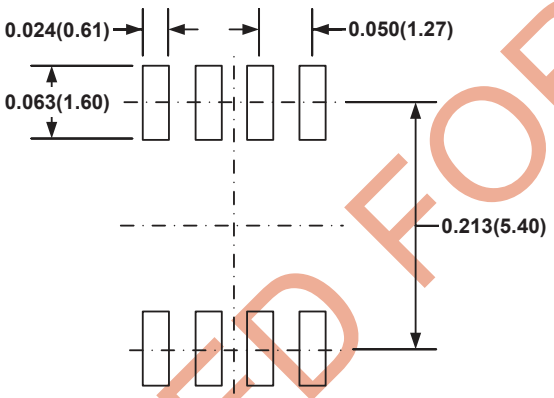
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2161A


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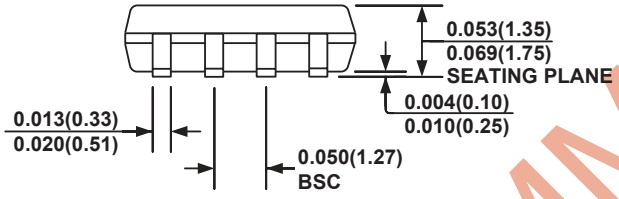
## SOIC8E



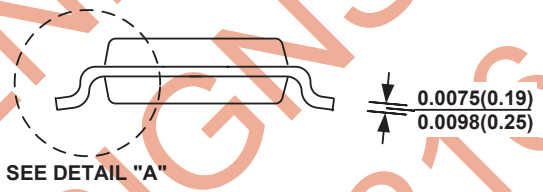

TOP VIEW



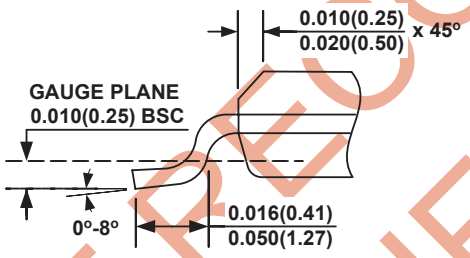

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW




DETAIL "A"

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2131A

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