# MP1924A

## 100V, 4A, High Frequency Half-Bridge Gate Driver

The Future of Analog IC Technology

## DESCRIPTION

The MP1924A is a high-frequency, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled independently and matched with less than 5ns of time delay. Under-voltage lockout (UVLO) on both the high-side and low-side supplies forces the outputs low in the event that the supply is insufficient. The integrated bootstrap diode reduces the external component count.

The MP1924A is available in QFN-10 (4mmx4mm) and SOIC-8 packages.

## FEATURES

- Drives an N-Channel MOSFET Half-Bridge
- 115V Bootstrap Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Driver Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns of Rise Time and 12ns of Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 150μA
- UVLO for Both High-Side and Low-Side Gate Drivers
- QFN-10 (4mmx4mm) and SOIC-8 Packages

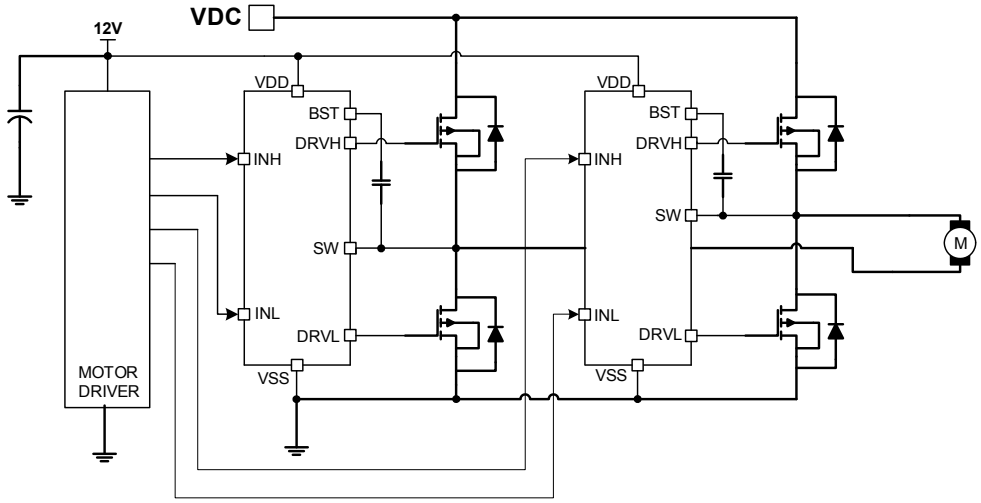
## APPLICATIONS

- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

## TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## ORDERING INFORMATION

| Part Number | Package | Top Marking |
|---|---|---|
| MP1924AHR* | QFN-10 (4mmx4mm) | *See Below* |
| MP1924AHS** | SOIC-8 | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MP1924AHR–Z)
For RoHS compliant packaging, add suffix –LF (e.g. MP1924AHR–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP1924AHS–Z)
For RoHS compliant packaging, add suffix –LF (e.g. MP1924AHS–LF–Z)

## TOP MARKING (MP1924AHR)

MPSYWW
M1924A
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M1924A: Product code of MP1924AHR
LLLLLL: Lot number

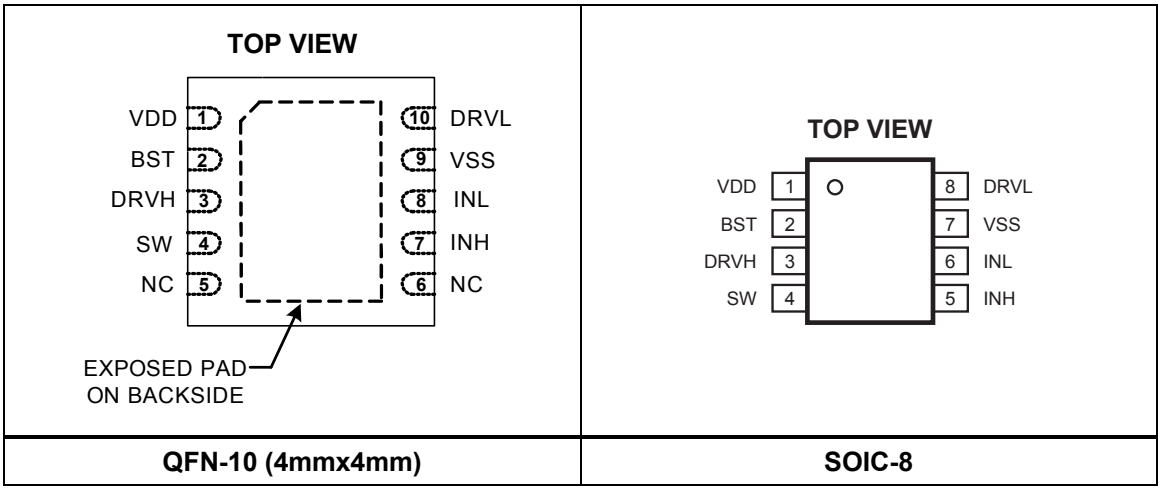
## TOP MARKING (MP1924AHS)

MP1924A
LLLLLLLL
MPSYWW

MP1924A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## PACKAGE REFERENCE




| QFN-10 (4mmx4mm) | SOIC-8 |
|---|---|

## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{DD}$) .....-0.3V to 18V
SW voltage ($V_{SW}$) .....-5.0V to 105V
BST voltage ($V_{BST}$) .....-0.3V to 115V
BST to SW .....-0.3V to 18V
DRVH to SW ..... -0.3V to (BST - SW) + 0.3V
DRVL to VSS ..... -0.3V to ($V_{DD}$ + 0.3V)
All other pins .....-0.3V to ($V_{DD}$ + 0.3V)
Continuous power dissipation ($T_A$ = 25°C) (2)
QFN-10 (4mmx4mm) ..... 2.66W
SOIC-8 ..... 1.3W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to 150°C

## *Recommended Operating Conditions* (3)

Supply voltage ($V_{DD}$) .....8.0V to 15.0V
SW voltage ($V_{SW}$) .....-1.0V to 100V
SW slew rate..... <50V/ns
Operating junction temp. ($T_J$ = $T_A$)
..... -40°C to 125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| QFN-10 (4mmx4mm) | 47 | 7 | °C/W |
| SOIC-8 | 96 | 45 | °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$(MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = $V_{BST}$ - $V_{SW}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, no load at DRVH and DRVL, $T_J$ = -40°C to +125°C, typical value is tested at $T_J$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Currents** | | | | | | |
| VDD quiescent current | $I_{DDQ}$ | INL = INH = 0 | | 100 | 150 | μA |
| VDD operating current | $I_{DDO}$ | fsw = 500kHz | | 9 | | mA |
| Floating driver quiescent current | $I_{BSTQ}$ | INL = INH = 0 | | 60 | 90 | μA |
| Floating driver operating current | $I_{BSTO}$ | fsw = 500kHz | | 7.5 | | mA |
| Leakage current | $I_{LK}$ | BST = SW = 100V | | 0.05 | 1 | μA |
| **Inputs** | | | | | | |
| INL/INH high | | | | 2 | 2.4 | V |
| INL/INH low | | | 1 | 1.4 | | V |
| INL/INH internal pull-down resistance | $R_{IN}$ | | | 185 | | kΩ |
| **Under-Voltage Protection** | | | | | | |
| VDD rising threshold | $V_{DDR}$ | | 6 | 6.8 | 7.2 | V |
| VDD hysteresis | $V_{DDH}$ | | | 0.5 | | V |
| BST-SW rising threshold | $V_{BSTR}$ | | 5.8 | 6.5 | 6.9 | V |
| BST-SW hysteresis | $V_{BSTH}$ | | | 0.5 | | V |
| **Bootstrap Diode** | | | | | | |
| Bootstrap diode VF at 100μA | $V_{F1}$ | | | 0.5 | | V |
| Bootstrap diode VF at 100mA | $V_{F2}$ | | | 0.95 | | V |
| Bootstrap diode dynamic R | $R_D$ | at 100mA | | 2.5 | | Ω |
| **Low-Side Gate Driver** | | | | | | |
| Low level output voltage | $V_{OLL}$ | $I_O$ = 100mA | | 0.1 | | V |
| High level output voltage to rail | $V_{OHL}$ | $I_O$ = -100mA | | 0.36 | | V |
| Source current(5) | $I_{OHL}$ | $V_{DRVL}$ = 0V, $V_{DD}$ = 12V | | 3 | | A |
| | | $V_{DRVL}$ = 0V, $V_{DD}$ = 16V | | 4.7 | | A |
| Sink current(5) | $I_{OLL}$ | $V_{DRVL}$ = $V_{DD}$ = 12V | | 4.5 | | A |
| | | $V_{DRVL}$ = $V_{DD}$ = 16V | | 6 | | A |
| **Floating Gate Driver** | | | | | | |
| Low level output voltage | $V_{OLH}$ | $I_O$ = 100mA | | 0.1 | | V |
| High level output voltage to rail | $V_{OHH}$ | $I_O$ = -100mA | | 0.32 | | V |
| Source current(5) | $I_{OHH}$ | $V_{DRVH}$ = 0V, $V_{DD}$ = 12V | | 2.6 | | A |
| | | $V_{DRVH}$ = 0V, $V_{DD}$ = 16V | | 4 | | A |
| Sink current(5) | $I_{OLH}$ | $V_{DRVH}$ = $V_{DD}$ = 12V | | 4.5 | | A |
| | | $V_{DRVH}$ = $V_{DD}$ = 16V | | 5.9 | | A |

**NOTE:**

5) Guaranteed by design.


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{DD}$ = $V_{BST}$ - $V_{SW}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, no load at DRVH and DRVL, $T_J$ = -40°C to +125°C, typical value is tested at $T_J$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Switching Specification—Low-Side Gate Driver** | | | | | | |
| Turn-off propagation delay INL falling to DRVL falling | $T_{DLFF}$ | | | 20 | | ns |
| Turn-on propagation delay INL rising to DRVL rising | $T_{DLRR}$ | | | 20 | | |
| DRVL rise time | | $C_L$ = 2.2nF | | 15 | | ns |
| DRVL fall time | | $C_L$ = 2.2nF | | 15 | | ns |
| **Switching Specification—Floating Gate Driver** | | | | | | |
| Turn-off propagation delay INH falling to DRVH falling | $T_{DHFF}$ | | | 20 | | ns |
| Turn-on propagation delay INH rising to DRVH rising | $T_{DHRR}$ | | | 20 | | ns |
| DRVH rise time | | $C_L$ = 2.2nF | | 15 | | ns |
| DRVH fall time | | $C_L$ = 2.2nF | | 15 | | ns |
| **Switching Specification—Matching** | | | | | | |
| Floating driver turn-off to low side driver turn-on(5) | $T_{MON}$ | | | 1 | 5 | ns |
| Low-side driver turn-off to floating driver turn-on(5) | $T_{MOFF}$ | | | 1 | 5 | ns |
| Minimum input pulse width that changes the output(5) | $T_{PW}$ | | | | 50 | ns |
| Bootstrap diode turn-on or turn-off time(5) | $T_{BS}$ | | | 10 | | ns |
| Thermal shutdown | | | | 150 | | °C |
| Thermal shutdown hysteresis | | | | 25 | | °C |

**NOTE:**

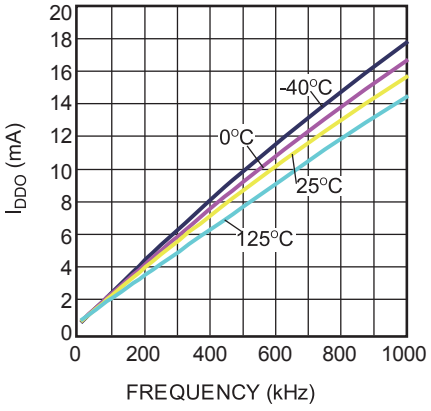
6) Guaranteed by design.


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

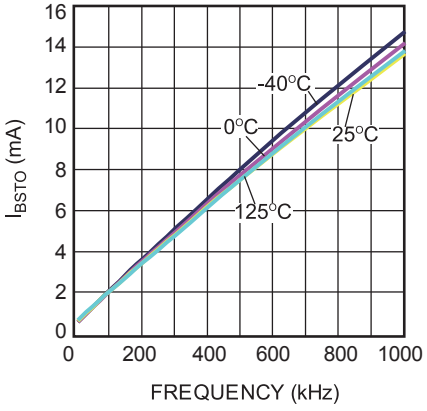
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{DD}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, $T_A$ = +25°C, unless otherwise noted.**

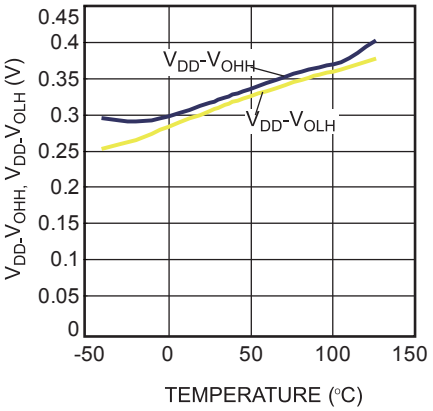
### $I_{DDO}$ Operation Current vs. Frequency



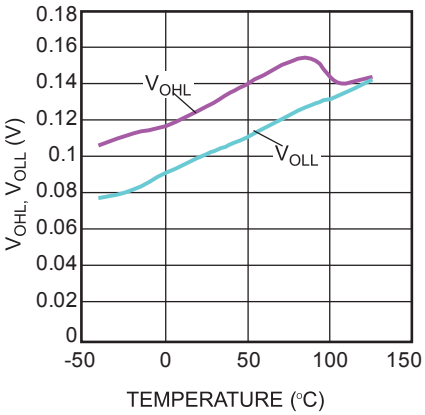

### $I_{BSTO}$ Operation Current vs. Frequency



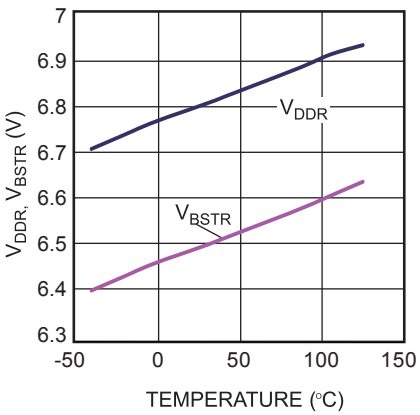

### High-Level Output Voltage vs. Temperature



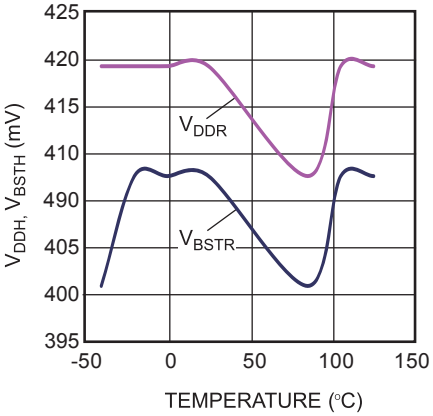

### Low-Level Output Voltage vs. Temperature



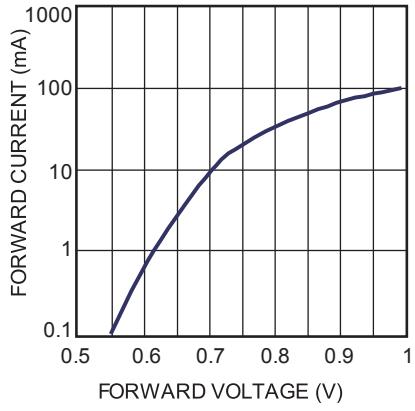

### Under-Voltage Lockout Threshold vs. Temperature




### Under-Voltage Lockout Hysteresis vs. Temperature

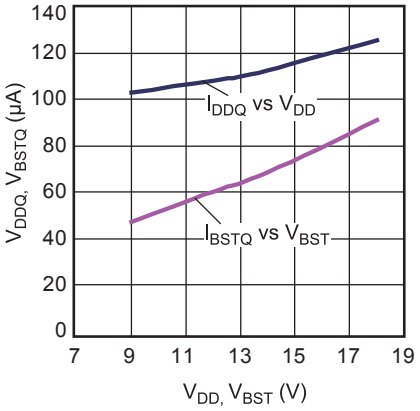



### Bootstrap Diode I-V Characteristic

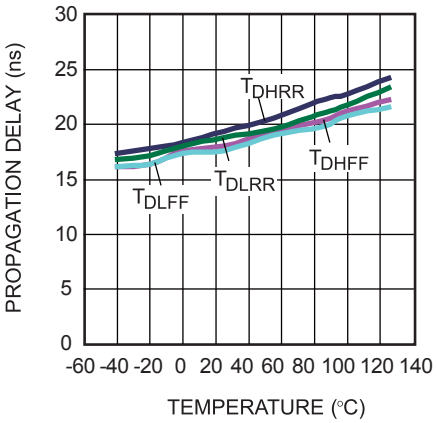



### Quiescent Current vs. Voltage

INH=INL=0V




### Propagation Delay vs. Temperature



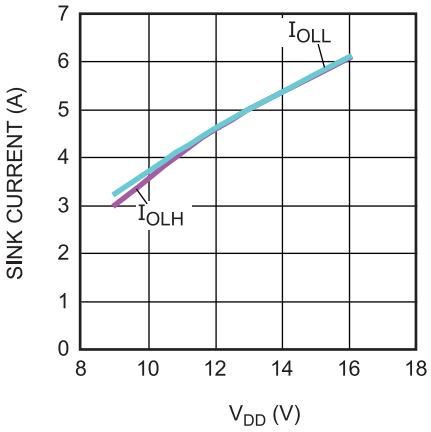


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

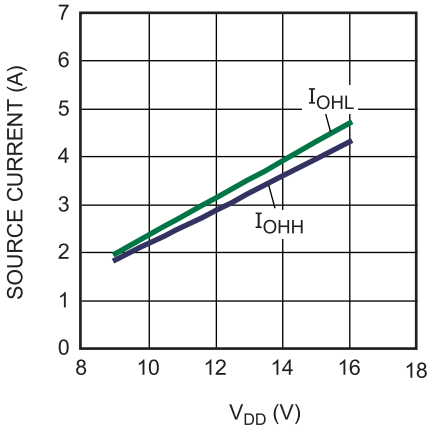
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{DD}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, $T_A$ = +25°C, unless otherwise noted.**

**Sink Current vs. $V_{DD}$ Voltage**

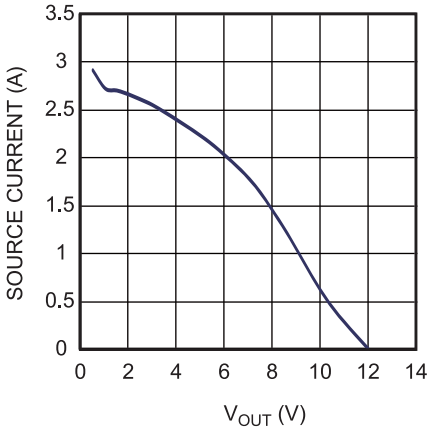



**Source Current vs. $V_{DD}$ Voltage**



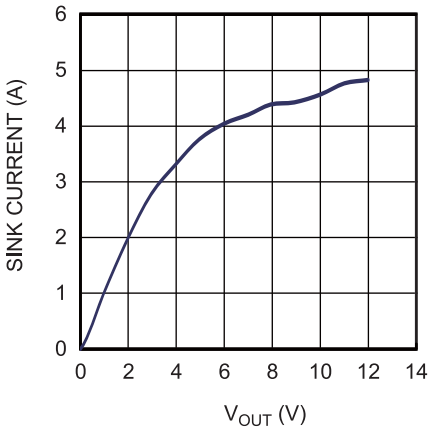

**Source Current vs. Output Voltage**

$V_{DD}$=12V




**Sink Current vs. Output Voltage**

$V_{DD}$=12V



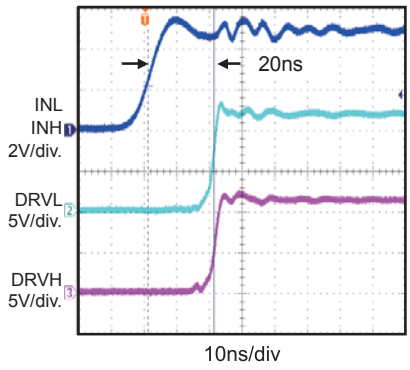


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

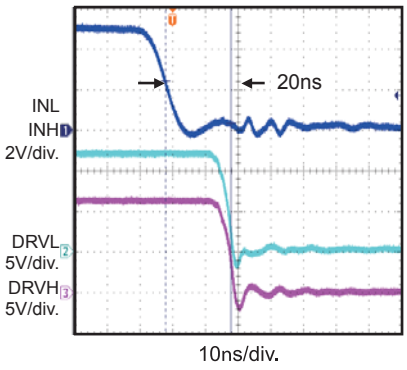
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{DD}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, $T_A$ = +25°C, unless otherwise noted.**

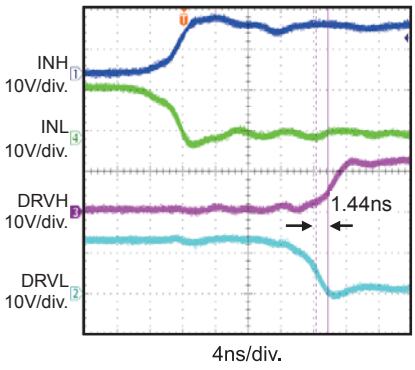
### Turn-On Propagation Delay



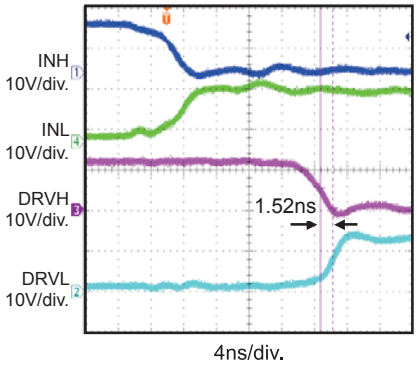

### Turn-Off Propagation Delay




### Gate Drive Matching $T_{MOFF}$

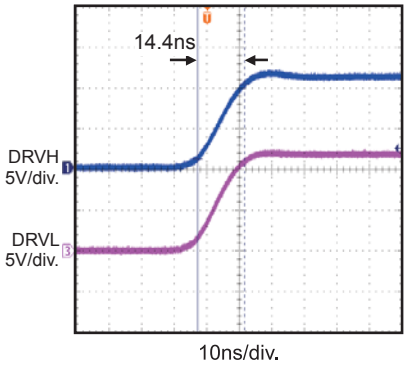



### Gate Drive Matching $T_{MON}$



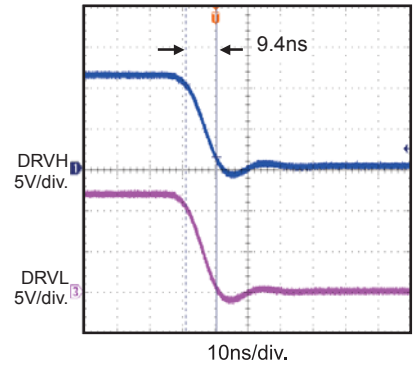

### Drive Rise Time

2.2nF Load




### Drive Fall Time

2.2nF Load





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## PIN FUNCTIONS

| QFN-10 Pin # | SOIC-8 Pin # | Name | Description |
|---|---|---|---|
| 1 | 1 | VDD | **Supply input.** VDD supplies power to the internal circuitry. Place a decoupling capacitor on ground close to VDD to ensure a stable and clean supply. |
| 2 | 2 | BST | **Bootstrap.** BST is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW. |
| 3 | 3 | DRVH | **Floating driver output.** |
| 4 | 4 | SW | **Switching node.** |
| 5, 6 | | NC | **No connection.** |
| 7 | 5 | INH | **Control signal input for the floating driver.** |
| 8 | 6 | INL | **Control signal input for the low-side driver.** |
| 9 | 7 | VSS, Exposed Pad | **Chip ground.** Connect the exposed pad to VSS for proper thermal operation. |
| 10 | 8 | DRVL | **Low-side driver output.** |


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## TIMING DIAGRAM

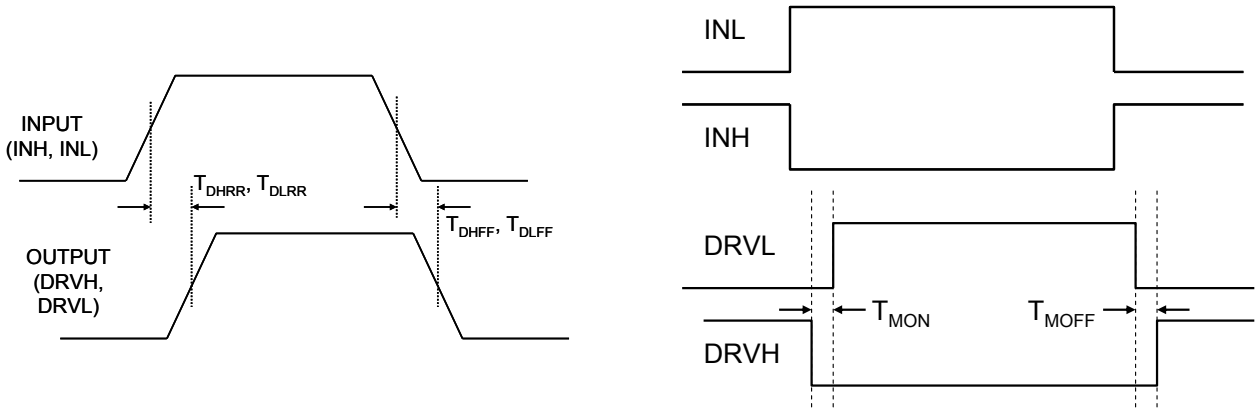



**Figure 1: Timing Diagram**


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## FUNCTIONAL BLOCK DIAGRAM

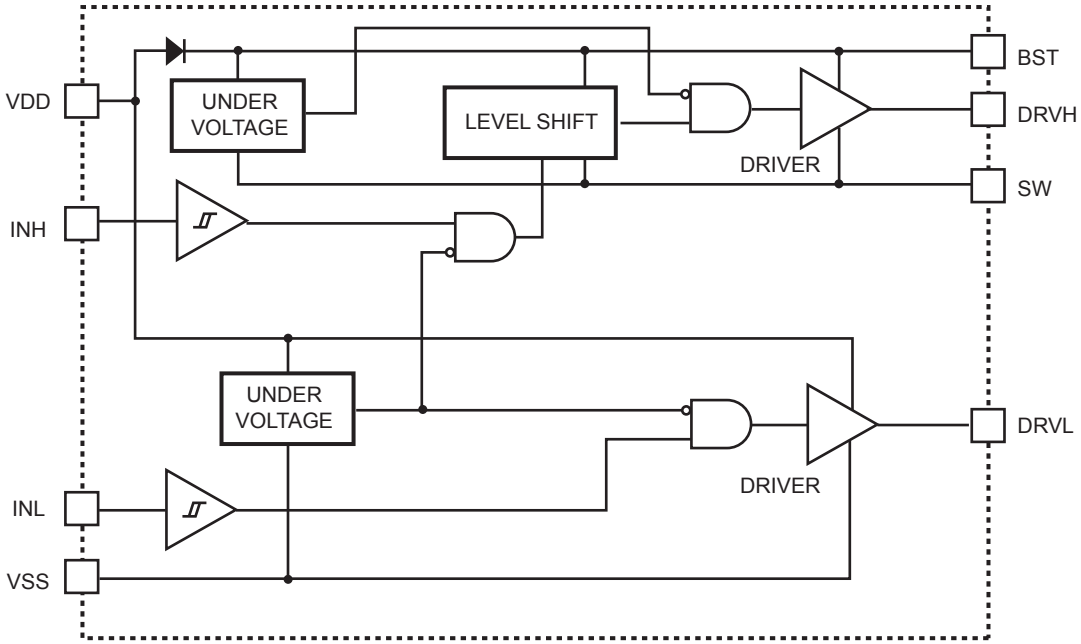



**Figure 2: Functional Block Diagram**


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## APPLICATION INFORMATION

The input signals of INH and INL can be controlled independently. If both INH and INL control the high-side and low-side MOSFETs of the same bridge, set a sufficient dead time between INH and INL low (and vice versa) to avoid a shoot-through (see Figure 3). Dead time is defined as the time interval between INH low and INL low.

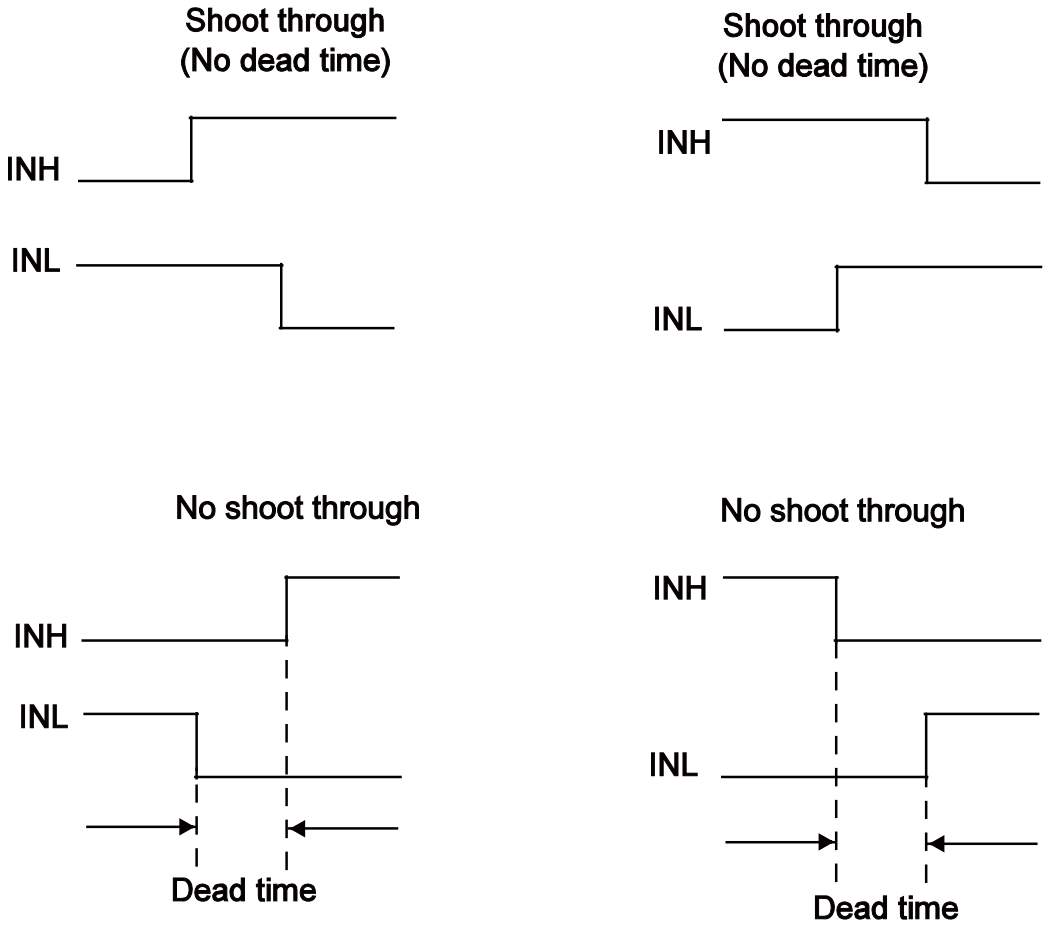



**Figure 3: Shoot-Through Timing Diagram**


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

## REFERENCE DESIGN CIRCUITS

### Half-Bridge Converter

The MP1924A drives the MOSFETS with alternating signals with dead time in half-bridge converter topology. The input voltage can rise up to 100V with the alternating signals INT and INL coming from the PWM controller (see Figure 4).

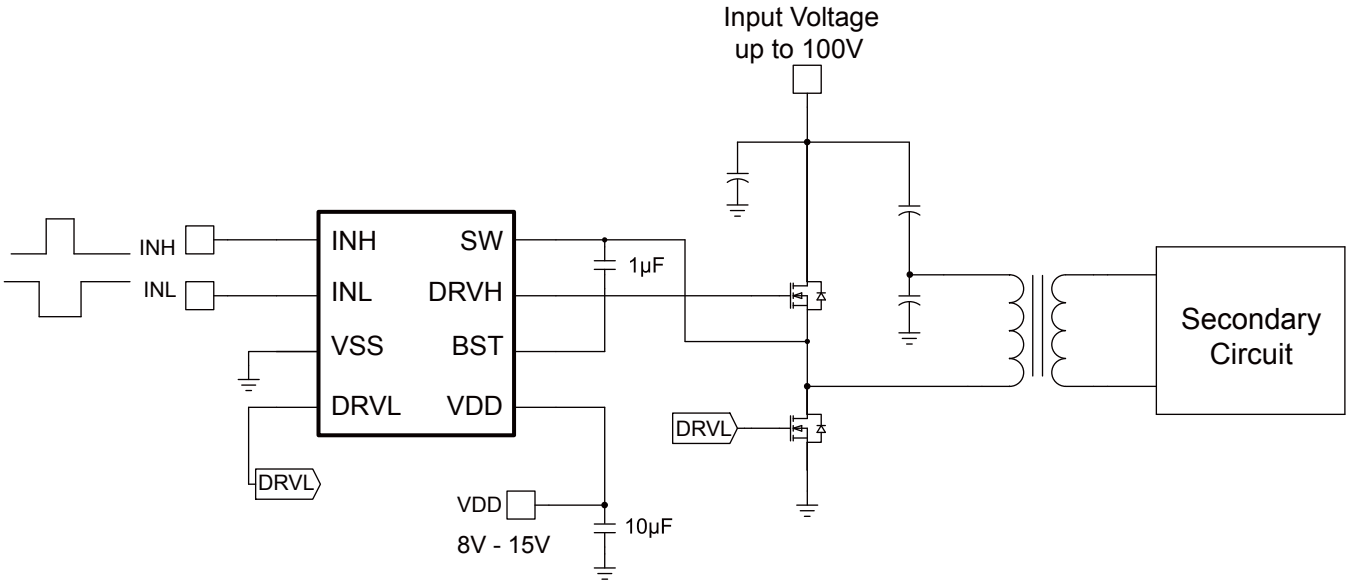



**Figure 4: Half-Bridge Converter**

### Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs are turned on and off simultaneously. The input signals INH and INL come from a PWM controller that senses the output voltage and output current during current-mode control.

The Schottky diodes clamp the reverse swing of the power transformer and must be rated for the input voltage. The input voltage can rise up to 100V (see Figure 5).

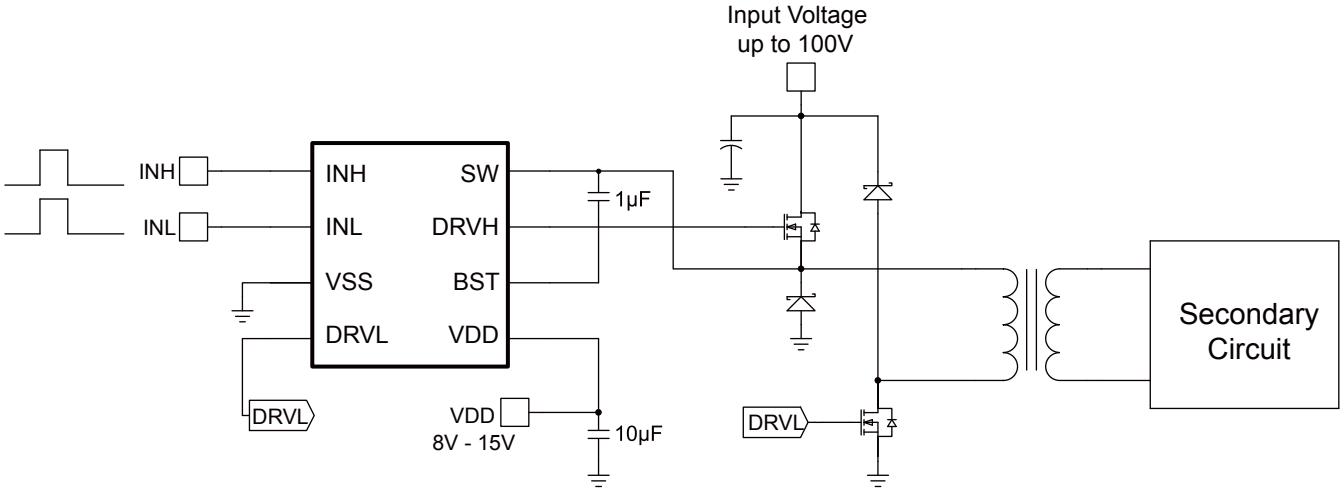



**Figure 5: Two-Switch Forward Converter**


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

### Active Clamp Forward Converter

In active clamp forward converter topology, the MP1924A drives the MOSFETs with alternating signals. The high-side MOSFET, in conjunction with $C_{reset}$, is used to reset the power transformer in a lossless manner.

This topology is optimal for running at duty cycles exceeding 50%. The device may not be able to run at 100V under this topology (see Figure 6).

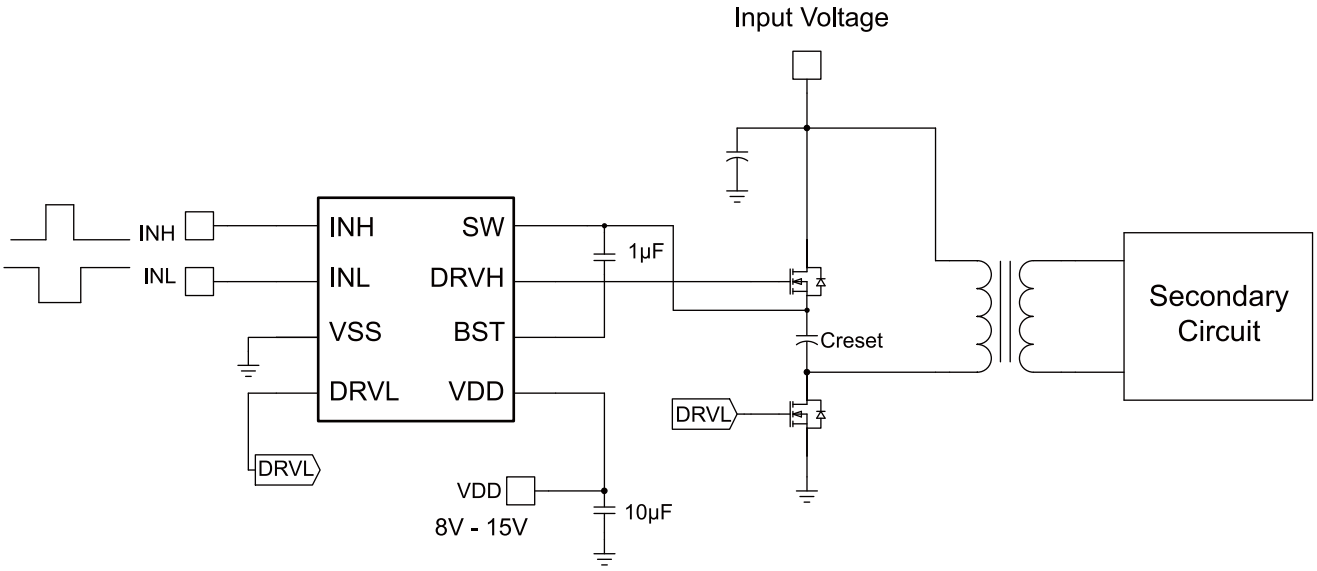
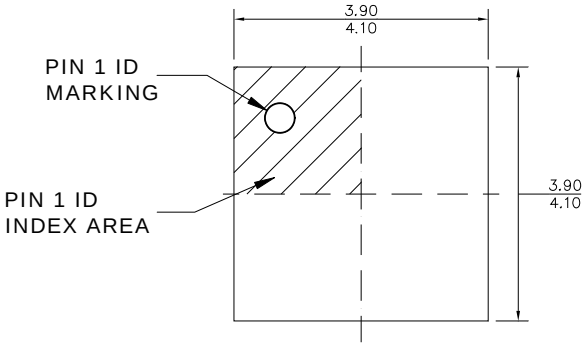



**Figure 6: Active Clamp Forward Converter**

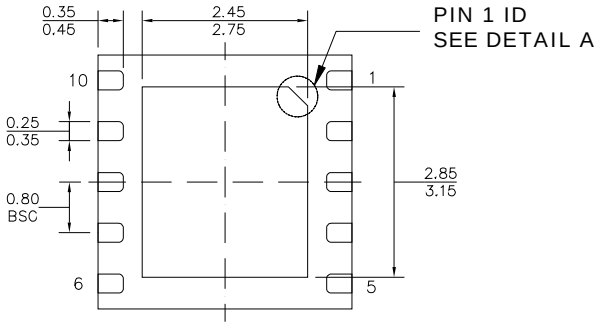

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

# PACKAGE INFORMATION

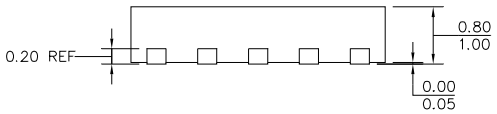
## QFN-10 (4mmx4mm)



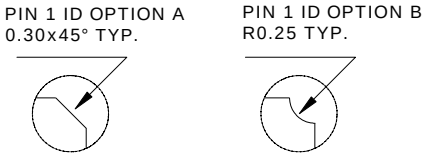

TOP VIEW



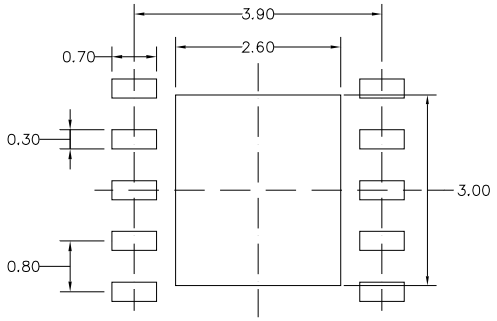

BOTTOM VIEW




SIDE VIEW




DETAIL A



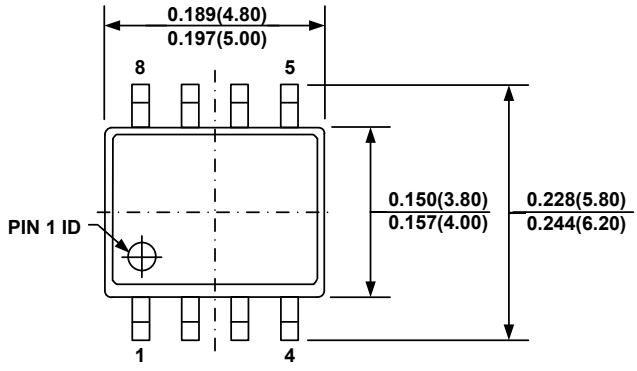

RECOMMENDED LAND PATTERN

NOTE:

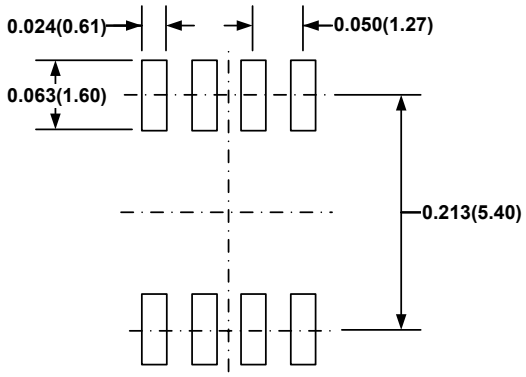
**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.**
**3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**4) JEDEC REFERENCE IS MO-220.**
**5) DRAWING IS NOT TO SCALE.**


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

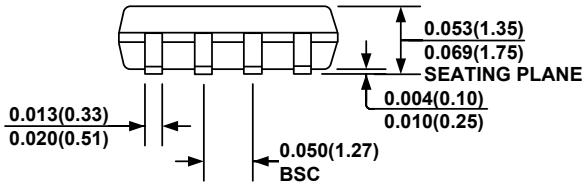
## SOIC-8



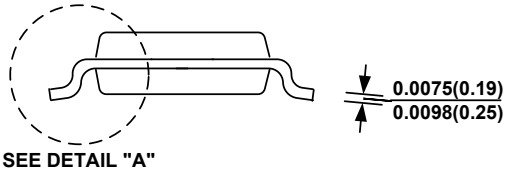

TOP VIEW



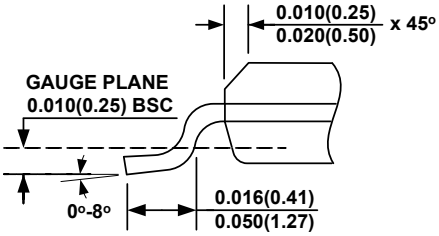

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW




DETAIL "A"

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

**NOTICE:** The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.