MP1740

3W HIGH EFFICIENCY

MONO CLASS-D AUDIO AMPLIFIER

The Future of Analog IC Technology

DESCRIPTION

The MP1740 is a high efficiency Class-D H-bridge audio amplifier. It utilizes a full bridge output structure capable of delivering 3W into 4Ω speaker. The device exhibits the high fidelity of a class AB amplifier with an efficiency of 91%. It also dramatically reduces solution size by integrating the following:

- 300mΩ (high side or low side) power MOSFETs (VCC=3.6V)
- Startup / Shutdown pop elimination
- Short circuit protection
- 9 Balls Wafer chip scale package (WLCSP) and requires a few external components.

This amplifier also improves GSM power supply rejection, and operates on a single cellular Li-ion battery.

The gain of this amplifier can be controlled easily by a few modification of external configuration while minimizing noise to 37 μVRMS.

FEATURES

- 3W Into 4Ω with 5 V Supply @ 10% THD+N
- Efficiency up to 90% at 1.7W Pout, 8 ohm load
- 2.5V to 5.5V Supply Voltage Operation
- THD+N = 0.1% @ 1.8W, 5V, 4Ω
- 2mA Quiescent current and 0.5μA shutdown current
- Full Bridge Output Drive
- Internal 250kHZ Switching frequency
- Fully Differential input
- Improved CMRR Eliminates Two Input Coupling Capacitors
- 1ms start-up time Eliminates pop
- Integrated Short Circuit Protection
- Integrated Thermal Shutdown
- 9 Balls Wafer chip scale package (WLCSP)

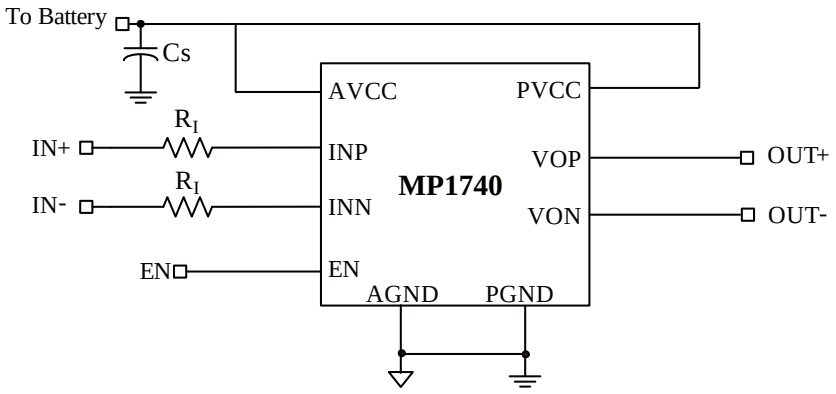
APPLICATIONS

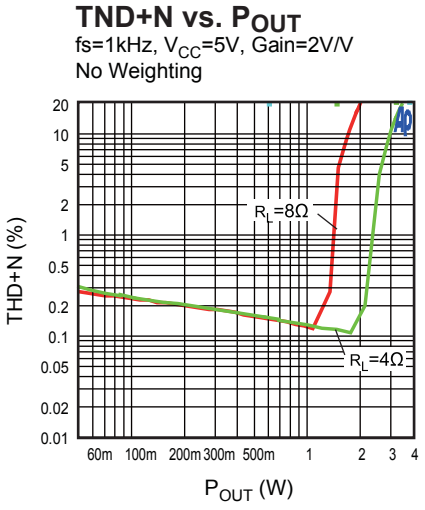
- Wireless or Cellular Handsets
- PDAs

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TYPICAL APPLICATION



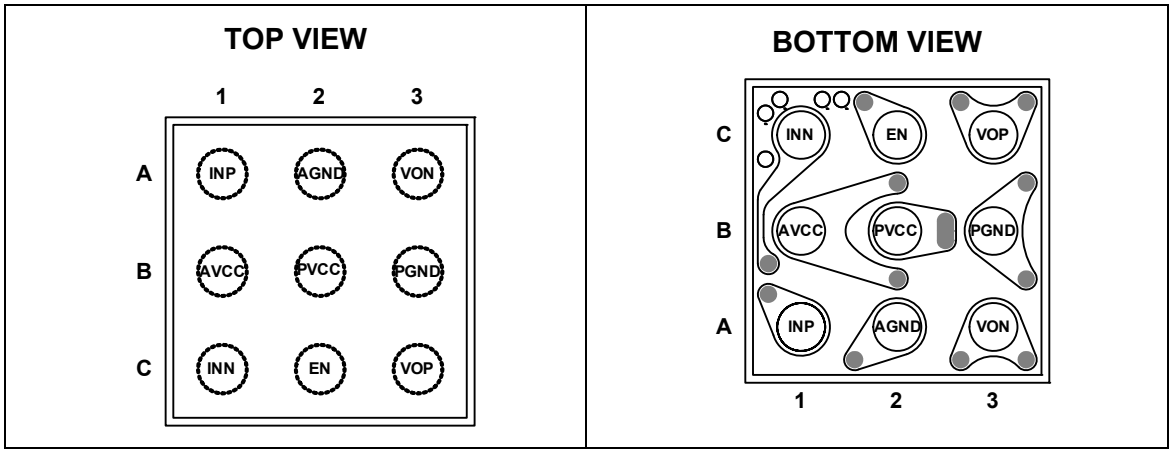


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ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP1740EC	WLCSP	6F	–20°C to +85°C

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{CC} .....-0.3V to 6.5V
Input Voltage V_{IN} ..... –0.3V to V_{CC} + 0.3V
Input Voltage V_{EN} ..... –0.3V to V_{CC} + 0.3V
Ambient Temperature T_A ..... –40°C to +85°C
Continuous Power Dissipation (T_A = +25°C)(2)
..... 1W
Junction Temperature T_J..... –40°C to +140°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} .....2.5V to 5.5V
Enable Voltage V_{EN} ..... 70%V_{CC} to V_{CC}
Disable Voltage V_{EN} ..... 0V to 15%V_{CC}
Common Mode Input Voltage V_{IC}
..... 0.5V to VCC-0.8V
Operating Junct. Temp (T_J)..... –20°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP .....114 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $PD_{(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) VCC Include AVCC and PVCC, VIN include INP and INN
4) Measured on JESD51-7, 4-layer PCB

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ELECTRICAL CHARACTERISTICS

T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Offset Voltage	$\|V_{os}\|$	VI=0V, Av=2V/V, VCC=2.5V to 5.5V		1	25	mV
Power Supply Rejection Ratio	PSRR	VCC=2.5V to 5.5V		-70	-45	dB
Common Mode Rejection Ratio	CMRR	VCC=2.5V to 5.5V, VIC＝1/2VCC to 0.5V, VIC＝1/2VCC to VCC -0.8V		-70		dB
High-level Input Current	I_{IH}	VCC=5.5V, VI=5.5V,RI=150kΩ		20	30	μA
Low-level Input Current	I_{IL}	VCC=5.5V, VI=0V,RI=150kΩ		20	30	μA
Quiescent Current	I_Q	VCC=5.5V, no load, switching		2.7	5.8	mA
		VCC=3.6V, no load, switching		2	4.6	
		VCC=2.5V, no load, switching		1.6	3.6	
Shut down Current	I_{ds}	VEN=0, VCC=2.5V to 5.5V		0.5	2	μA
VEN Enable L-H		VCC=2.5V to 5.5V	1.6			V
VEN Enable H-L		VCC=2.5V to 5.5V			0.4	V
UVLO_H		VCC from Low to High		2.4	2.48	V
UVLO_L		VCC from High to Low	1.95	2.1		V
Static On-state Resistance	Rds_on	VCC=5.5V		250		mΩ
		VCC=3.6V		300		
		VCC=2.5V		360		
Output impedance in disable	R_O	VEN<0.8V		2		kΩ
Switching frequency	F_{SW}	VCC=2.5V to 5.5V	200	250	300	kHz
GAIN (VO/VI)		R_l =15 kΩ, no load	19	20	21	V/V
RPD		Resistance from EN to GND		300		kΩ

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OPERATION CHARACTERISTICS

VCC=AVCC=PVCC=EN, AGND = PGND = 0V, signal frequency fs=1kHz, R_l=150 Ω, Gain=2 V/V, C_l=2.2uF, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Power	P_{OUT}	THD+N=1%, f_S=1kHz, R_L=4Ω	VCC=5.5V		2.82		W
			VCC=5V		2.32		
			VCC=3.6V		1.16		
			VCC=2.5V		0.54		
		THD+N=10%, f_S=1kHz, R_L=4Ω	VCC=5.5V		3.62		
			VCC=5V		3.0		
			VCC=3.6V		1.51		
			VCC=2.5V		0.70		
		THD+N=1%, f_S=1kHz, R_L=8Ω	VCC=5.5V		1.65		
			VCC=5V		1.36		
			VCC=3.6V		0.71		
			VCC=2.5V		0.33		
		THD+N=10%, f_S=1kHz, R_L=8Ω	VCC=5.5V		2.12		
			VCC=5V		1.74		
			VCC=3.6V		0.91		
			VCC=2.5V		0.42		
Total Distorsion Plus Noise	THD+N	P_{OUT}=2W, f_S=1kHz, R_L=4Ω	VCC=5V		0.19%		
		P_{OUT}=1W, f_S=1kHz, R_L=4Ω	VCC=3.6V		0.14%		
		P_{OUT}=0.4W, f_S=1kHz, R_L=4Ω	VCC=2.5V		0.11%		
		P_{OUT}=1W, f_S=1kHz, R_L=8Ω	VCC=5V		0.11%		
		P_{OUT}=0.5W, f_S=1kHz, R_L=8Ω	VCC=3.6V		0.12%		
		P_{OUT}=0.2W, f_S=1kHz, R_L=8Ω	VCC=2.5V		0.13%		
Supply Ripple Rejection Ratio	K_{SVR}	f_{RIPPLE}=217Hz, V_{RIPPLE}=400mVpp, input AC-ground with C_I=0.22μF	VCC=5V		-62		dB
Signal to Noise Ratio	SNR	P_{OUT}=1W, R_L=8Ω			97.7		dB
Output Noise	V_n	VCC=5V, f=20 to 20kHz, input AC-ground with C_I=0.22μF	No weighting		53		μV_{RMS}
			A-weighting		37		
Common Mode Rejection Ratio	CMRR	$V_{IC-RIPPLE}$=1 V_{PP}, f_{RIPPLE} =217Hz	VCC=5V		-65		dB
Start-up Time From Disable	T_S				1		ms

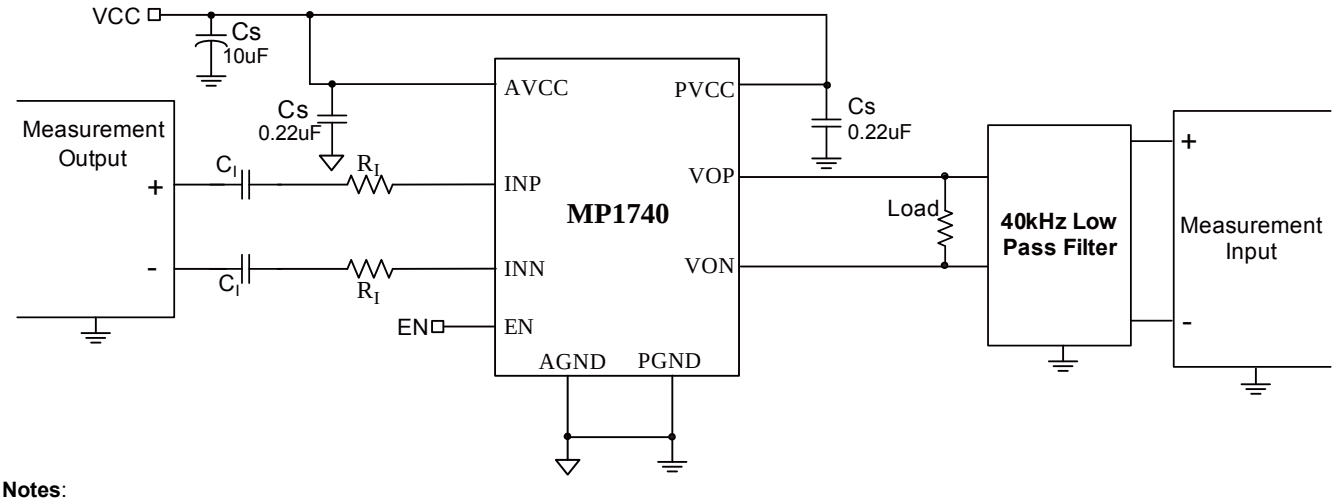
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PIN FUNCTIONS

Ball WLCSP	Name	Input/Ouput /Power (I/O/P)	Description
A1	INP	I	Positive differential input
A2	AGND	P	Analog Ground
A3	VON	O	Negative BTL output
B1	AVCC	P	Analog Power Supply
B2	PVCC	P	Power Supply
B3	PGND	P	Power Ground
C1	INN	I	Negative differential input
C2	EN	I	Enable Input. (drive high to enable the MP1740)
C3	VOP	O	Positive BTL output

TYPICAL PERFORMANCE CHARACTERISTICS

TEST SET-UP FOR GRAPHS



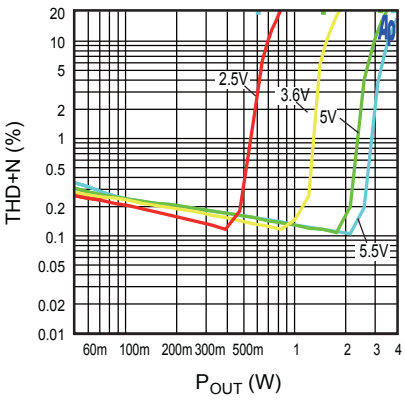
Notes:
5) C_I was Shorted for any Common-Mode input voltage measurement
6) A 33μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
7) The 40 kHz low-pass filter is required even if the analyzer has a low-pass filter.
8) For PSRR test, Please remove the great 10uF decoupling capacitor and just keep the small decoupling capacitors for recovery switching currents.

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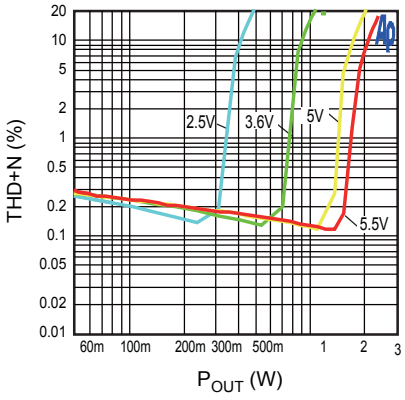
TYPICAL PERFORMANCE CHARACTERISTICS

VCC=AVCC=PVCC=EN, AGND = PGND = 0V, signal frequency fs=1kHz, R_l=150kohm, Gain=2 V/V, C_l=2.2uF, T_A = +25°C, unless otherwise noted.

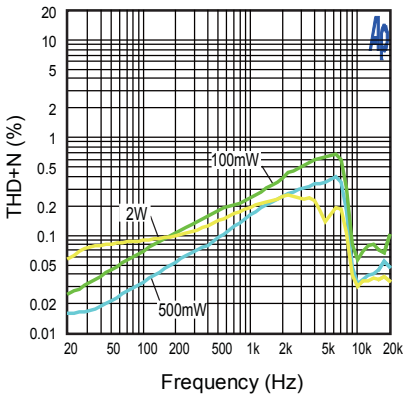
TND+N vs. P_{OUT}
R_L=4Ω, No weighting



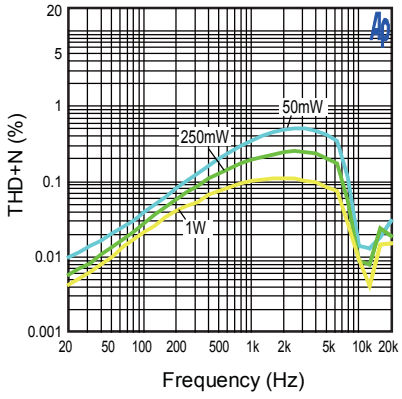
TND+N vs. P_{OUT}
R_L=8Ω, No weighting



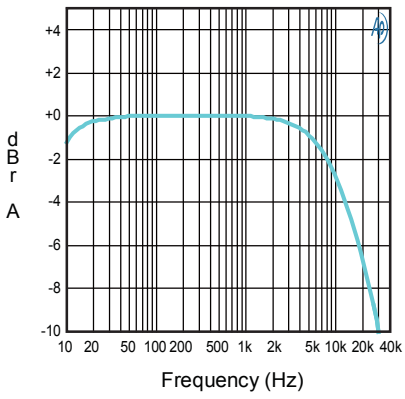
TND+N vs. Frequency
V_{CC}=5V, R_L=4Ω, No weighting



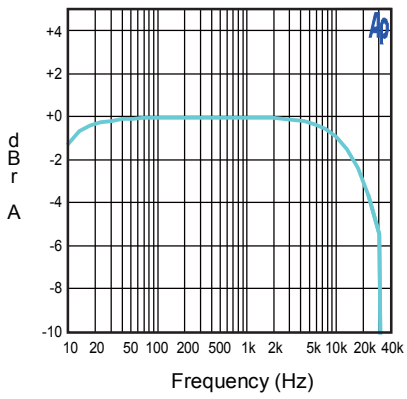
TND+N vs. Frequency
V_{CC}=5V, R_L=8Ω,



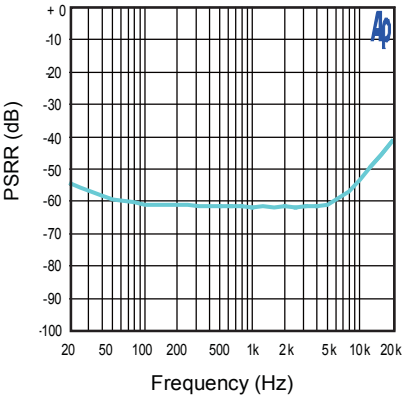
Frequency Response
V_{CC}=5V, R_L=4Ω, P_{OUT}=1W,
V_{OUT_ref} = V_{OUT_1kHz}



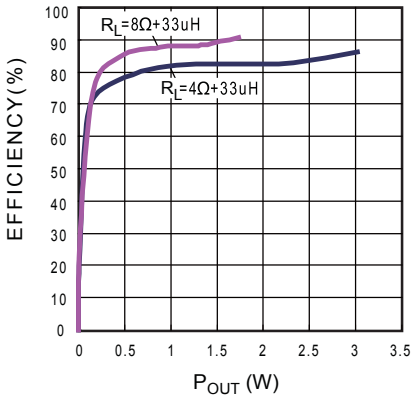
Frequency Response
V_{CC}=5V, R_L=8Ω, P_{OUT}=500mW,
V_{OUT_ref} = V_{OUT_1kHz}



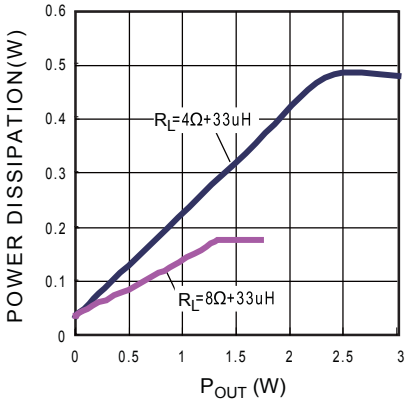
PSRR vs.Frequency
V_{CC}=5V, R_L=8Ω, Vripple=400mVpp
C_S=2x0.22uF, Inputs ac-grounded



Efficiency vs. P_{OUT}
V_{CC}=5V



Power Dissipation vs. P_{OUT}
V_{CC}=5V

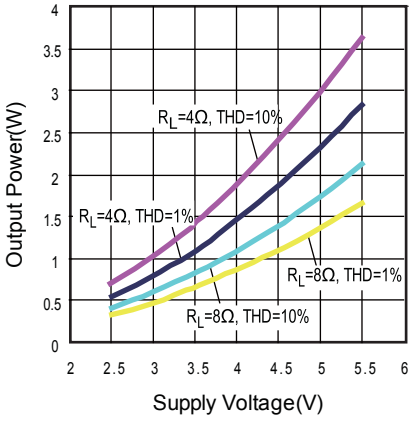


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

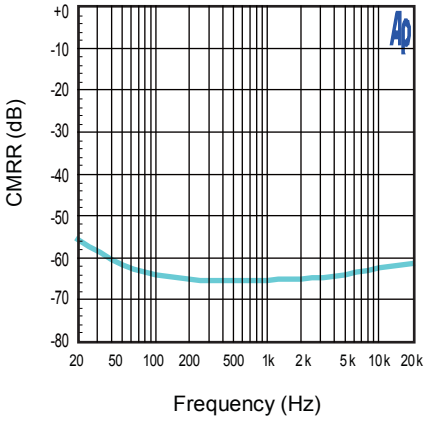
VCC=AVCC=PVCC=EN, AGND = PGND = 0V, signal frequency fs=1kHz, R_l=150kohm, Gain=2 V/V, C_l=2.2uF, T_A = +25°C, unless otherwise noted.

Output Power vs. Supply Voltage



CMRR vs. Frequency

V_{CC}=5V, R_L=4Ω, VIC-ripple=400mVpp



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FUNCTION BLOCK DIAGRAM

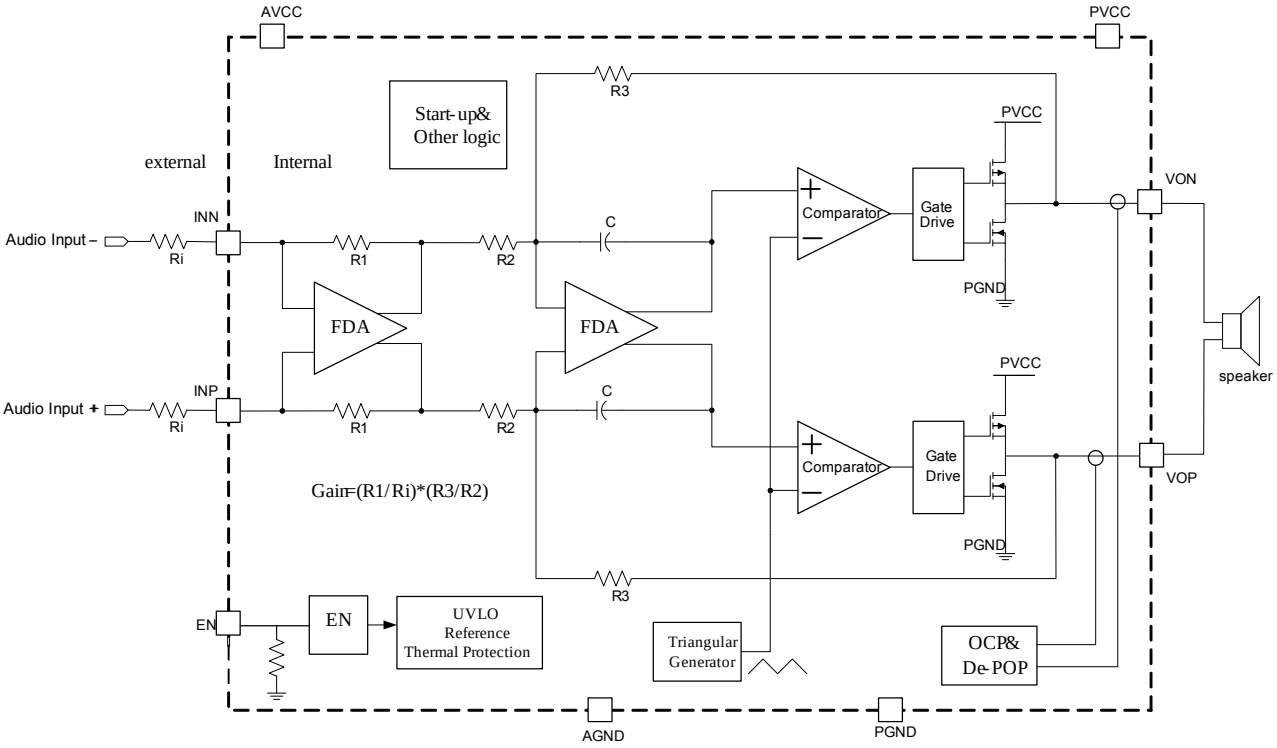


Figure 1—Functional Block Diagram

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APPLICATION INFORMATION

COMPONENT SELECTION

The MP1740 uses a minimum number of external components to complete a fully bridged Class D audio amplifier. Use the following sections to customize the amplifier for your particular application.

1. Setting the Voltage Gain

The voltage gain sets the output voltage swing for a given input voltage swing and is set by the input resistors (R_I) as the following equation:

$$GAIN=2\times\frac{150k\Omega}{R_I} \quad (1)$$

The maximum output voltage swing is limited by the power supply. To achieve the maximum output power of the MP1740 amplifier, set the amplifier gain such that the maximum peak-to-peak input signal results in at least the maximum peak-to-peak output voltage swing. Lower gain allows the MP1740 to operate at its best, because a higher voltage at the input for the same output power making the inputs less susceptible to noise. So setting voltage gain to 2V/V may achieve optimal performance.

2. Input Coupling Capacitors (C_I)

The MP1740 is a mono BTL Class-D amplifier with differential inputs and outputs. This device can still be used with a single-ended input; but for some noisy environment (such as a wireless handset) the MP1740 should be used with differential inputs to ensure maximum noise rejection.

The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. The input coupling capacitors are not required if the design uses a differential source that is biased from 0.5 V to VCC - 0.8 V (as shown in Recommended Operating Conditions). If the input signal is not biased within the recommended common-mode input range or if using a single-ended source, the input coupling capacitors are used to pass only the AC audio signal to the input of the amplifier as a high pass filter. The input capacitors create a high-pass filter with the input resistor. Choose an input coupling capacitor such that the corner frequency f_C is less than the desired pass-band frequency. The formula for the corner frequency is:

$$f_C=\frac{1}{2\pi R_I C_I} \quad (2)$$

Speakers in wireless handsets usually can't respond well to low frequencies, so for this application the corner frequency can be set to block the low frequencies.

The input coupling capacitance is calculated as:

$$C_I=\frac{1}{2\pi R_I f_C} \quad (3)$$

If the corner frequency is within the audible band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

3. Power Supply Decoupling Capacitor (C_S)

The class-D audio amplifier requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. To carry the higher frequency transient current, spikes, or digital hash on the line, a good low ESR ceramic capacitor is necessary. Place a 1μF decoupling capacitor as close as possible to the device VCC lead. It is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the capacitor and the device may cause a loss. A 10μF or greater capacitor placed near the audio power amplifier would also help for filtering lower-frequency noise.

4. Input Resistors (R_I)

In fully differential amplifiers, please use the matching input resistors. Matching is very important for the balance of the output on the reference voltage (more important than overall tolerance). The higher matching, the batter CMRR and PSRR performance. Therefore, it is recommended to use 1% precision resistors or better to keep the performance optimized. Place the input resistors as close to the MP1740 as possible to limit noise injection on the high-impedance nodes.

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TYPICAL APPLICATION CIRCUIT

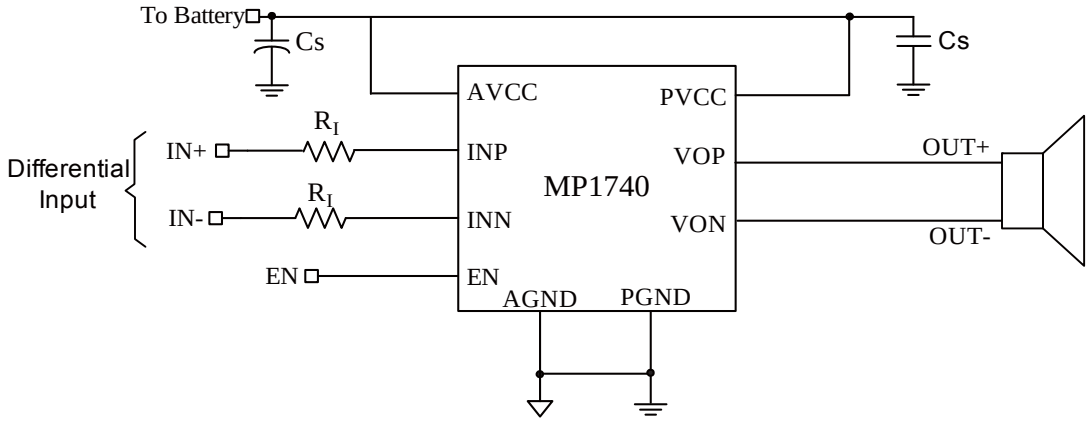


Figure 2—MP1740 Application Schematic with Differential Input

(input DC-biased voltage is within the recommended common-mode voltage range)

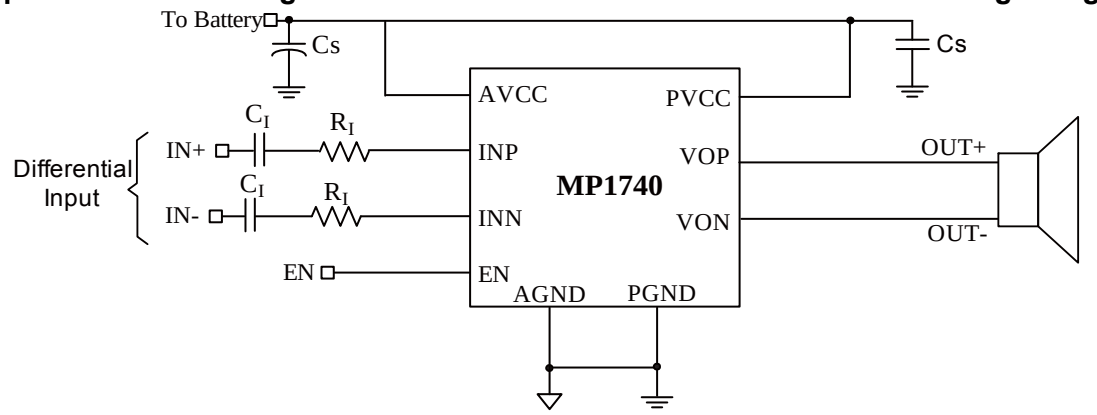


Figure 3—MP1740 Application Schematic with Differential Input

(input DC-biased voltage is out of the recommended common-mode voltage range)

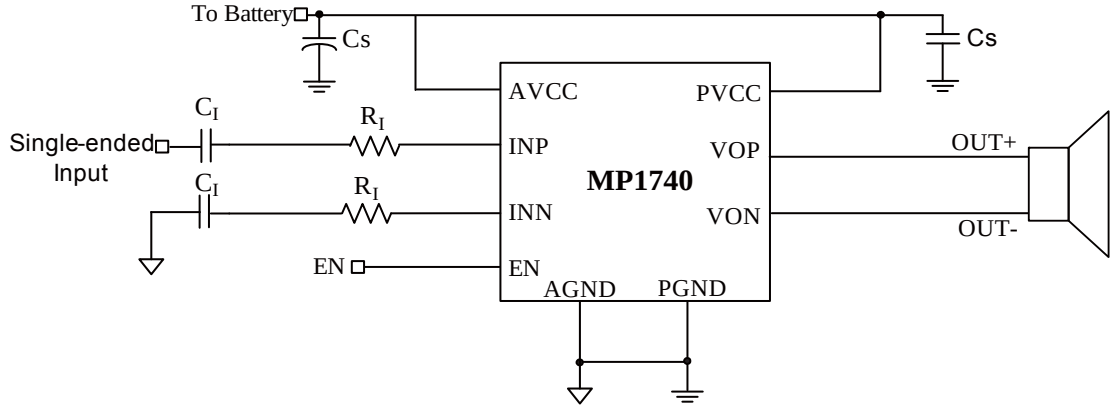
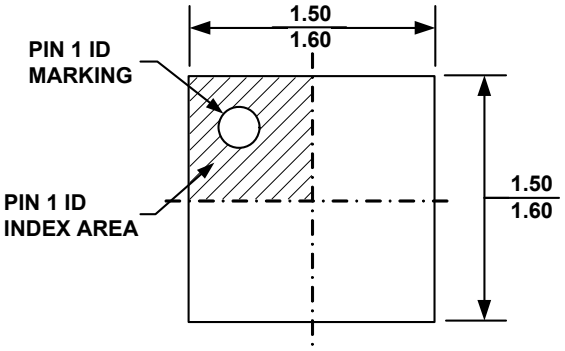


Figure 4—MP1740 Application Schematic with Single-Ended Input

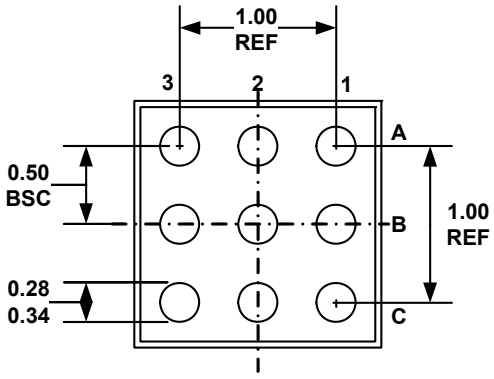
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PACKAGE INFORMATION

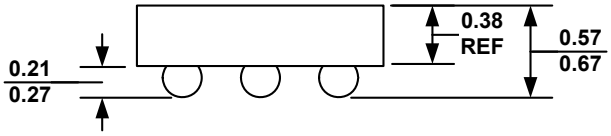
WLCSP



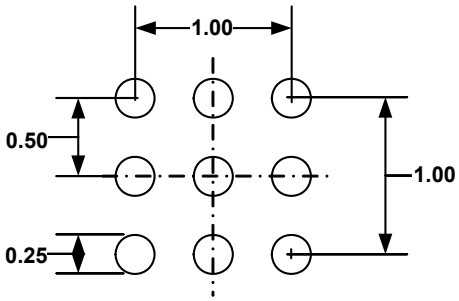
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION DD.
4) DRAWING IS NOT TO SCALE.

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