MP024-10

Primary-Side, CC/CV, Flyback Regulator with High-Voltage Current Source and Programmable Cable Compensation

The Future of Analog IC Technology

DESCRIPTION

The MP024-10 is a low-cost, offline, primary-side, flyback regulator with a simple, external circuit. It provides accurate constant voltage (CV) and constant current (CC) regulation without an optocoupler or secondary feedback circuit and has an integrated 700V MOSFET and high-voltage start-up current source.

The MP024-10 operates in discontinuous conduction mode (DCM) using variable off-time control. Its power-saving technologies limit the no-load power consumption to less than 30mW.

Full protection features include VCC under-voltage lockout (VCC UVLO), overload protection (OLP), over-temperature protection (OTP), open-loop protection (OCkP), sensing-short protection (SSP), and over-voltage protection (OVP).

The variable switching frequency method provides natural spectrum shaping to smooth the EMI signature, making the MP024-10 suitable for offline, low-power battery chargers and adapters.

The MP024-10 is available in a SOIC8-7B package.

Maximum Output Power (1) (4)

	230Vac ±15%		85Vac~265Vac	
	Open Frame (2)	Adapter (3)	Open Frame (2)	Adapter (3)
P_{OUT} (W)	13	10	10	7.5

NOTES:

1) The maximum output power is limited by thermal shutdown.
2) Maximum continuous power in an open frame design at 50°C ambient temperature.
3) Maximum continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4) Single output, V_{OUT} = 5V.

FEATURES

- Primary-Side Control without Optocoupler or Secondary Feedback Circuit
- Precise Constant Current and Constant Voltage Control (CC/CV)
- Variable Off-Time Peak-Current Control
- 700V/4.5Ω Integrated MOSFET
- 700V High-Voltage Current Source
- 30mW No-Load Power Consumption
- Programmable Cable Compensation
- Multiple Protections: OVP, OCkP, SSP, OLP, OTP, and VCC UVLO
- Low Cost and Simple External Circuit
- Available in a SOIC8-7B Package

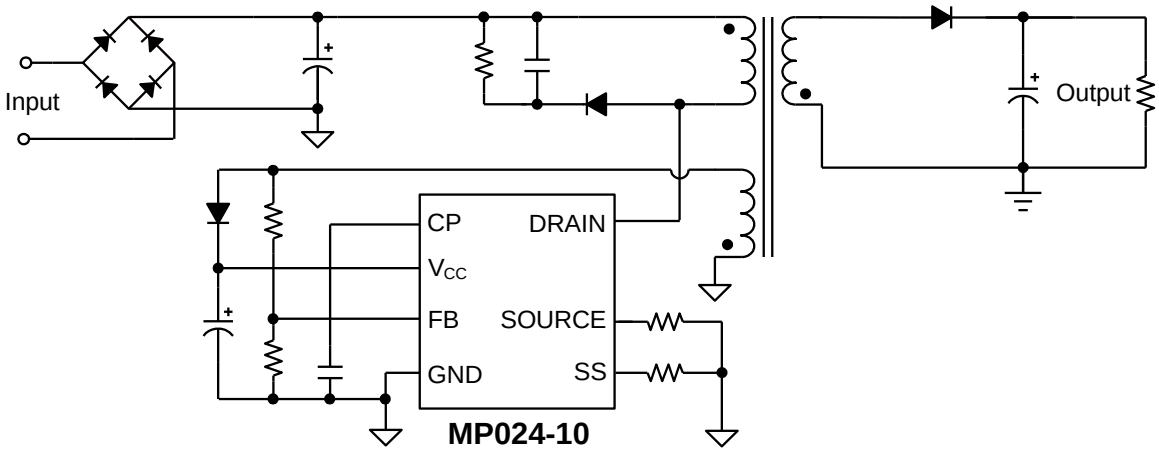
APPLICATIONS

- Cell Phone Chargers
- Adapters for Handheld Electronics
- Standby and Auxiliary Power Supplies

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP024GS-10	SOIC8-7B	*See Below*

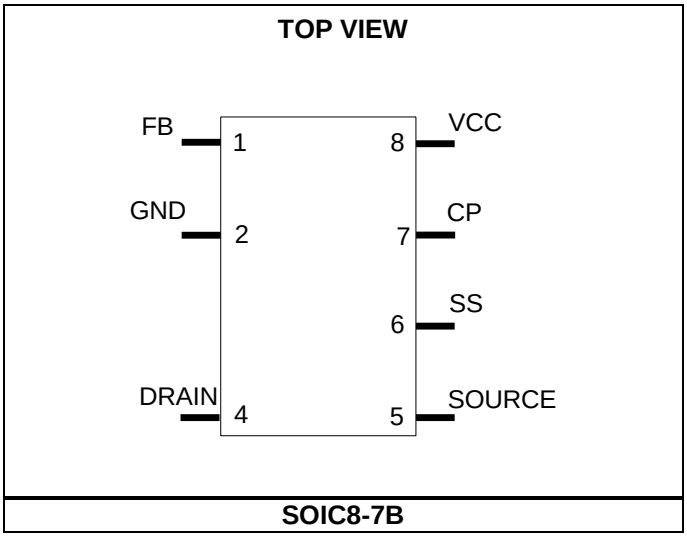
* For Tape & Reel, add suffix –Z (e.g. MP024GS-10–Z)

TOP MARKING

MP024-10
LLLLLLLL
MPSYWW

MP024-10: First five digits of the part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC8-7B

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ABSOLUTE MAXIMUM RATINGS (5)

DRAIN to SOURCE, GND ..... -0.3V to 700V
VCC to GND ..... -0.3V to 28V
CP, SS, SOURCE to GND ..... -0.3V to 7V
FB to GND ..... -0.7V to 7V
Continuous power dissipation (T_A = +25°C) (6) 1.66W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -60°C to +150°C
ESD capability human body model 2.0kV
ESD capability machine model 200V

Recommended Operating Conditions (7)

Junction temperature (T_J) ..... -40°C to +125°C
Ambient temperature (T_A) ..... -40°C to +110°C
Operating VCC range ..... 10V to 25V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8-7B	75	45	°C/W

NOTES:

5) Exceeding these ratings may damage the device.
6) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 15V, T_J = -40°C~125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage Management (VCC)						
VCC on threshold	V_{CCH}		18.8	19.4	20.0	V
VCC off threshold	V_{CCL}		8.2	8.7	9.2	V
Operating current	I_{OP}	$f_S = f_{S-min}$		235	300	µA
		f_S = 40kHz		0.55	0.85	mA
Internal MOSFET (DRAIN)						
Breakdown voltage	V_{BRDSS}		700			V
On state resistance	R_{DSon}	VCC = 10V, I_{DS} = 0.1A, T_J = 25°C		4.5	6.5	Ω
High-voltage current source supply current	I_{HV}	VCC = 18V, V_D = 80V, T_J = 25°C	1.8	2.2	2.6	mA
Leakage current	I_{leak}	V_D = 400V, T_J = 25°C			11	µA
Internal MOSFET (SOURCE)						
Maximum on time	t_{ONmax}	V_{SOURCE} = 0V	25	40	55	µs
Minimum switching frequency	f_{S-min}			75	110	Hz
Current limit	$V_{Limit-Max}$	$f_S \geq f_{S-H}$	464	480	496	mV
	$V_{Limit-Min}$	$f_S \leq f_{S-L}$	220	250	280	mV
f_S to start the current foldback	f_{S-H}		26	40	54	kHz
f_S to end the current foldback	f_{S-L}			20		kHz
Leading edge blanking	t_{LEB}		190	300	410	ns
Feedback Input (FB)						
FB input current	I_{FB}	V_{FB} = 4V, V_{CP} = 2V		12		µA
		V_{FB} = 4V, V_{CP} = 1.5V		9		µA
		V_{FB} = 4V, V_{CP} = 0.8V		4.6		µA
		V_{FB} = 4V, V_{CP} = 0.2V		1.2		µA
FB reference voltage	V_{FB}		3.90	3.96	4.02	V
OLP threshold at sampled FB	V_{FBolp}			1.4		V
OLP counter				768		
FB sampling duration	t_{FB-SD}		180	260	360	ns
FB maximum sampling time	$t_{FBS-Max}$	R_{SS} = 0Ω, V_{Limit} = 0.5V	2.60	3.62	4.9	µs
		R_{SS} = 1kΩ, V_{Limit} = 0.5V	1.85	2.72	3.65	
		R_{SS} = 2kΩ, V_{Limit} = 0.5V	3.8	5.5	7.2	
		R_{SS} = 4kΩ, V_{Limit} = 0.5V	5.3	7.2	9.3	
FB minimum sampling time	$t_{FBS-Min}$	R_{SS} = 0Ω, V_{Limit} = 0.25V	1.1	1.82	2.6	µs
		R_{SS} = 1kΩ, V_{Limit} = 0.25V	0.75	1.35	1.95	
		R_{SS} = 2kΩ, V_{Limit} = 0.25V	1.85	2.72	3.65	
		R_{SS} = 4kΩ, V_{Limit} = 0.25V	2.6	3.62	4.9	

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 15V, T_J = -40°C~125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ZCD threshold	V_{DCM}		55	100	145	mV
FB open-circuit threshold	V_{FBopen}		-190	-110	-45	mV
OVP threshold at FB	V_{FBovp}		5.7	5.96	6.3	V
FB OVP blanking time	t_{OVP-B}		1	1.35	1.7	µs
Output Cable Compensation (CP)						
Supply voltage on CP	V_{CP-Max}			4		V
Thermal Shutdown						
Thermal shutdown threshold (9)				140		°C
Thermal shutdown recovery hysteresis (9)				40		°C

NOTE:

9) The parameters are guaranteed by characterization.

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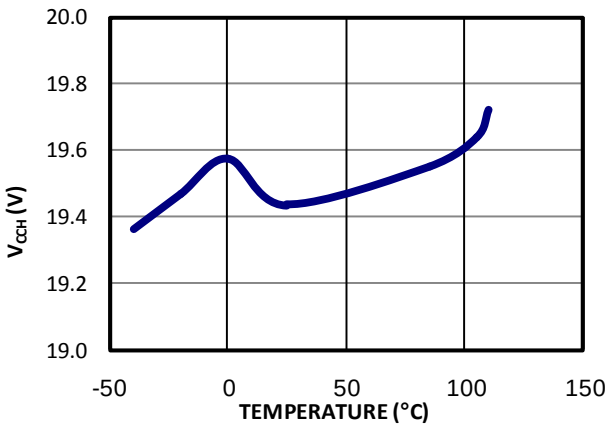
PIN FUNCTIONS

SOIC8-7B Pin #	Name	Description
1	FB	**Feedback.** The FB voltage determines the operation mode (CV mode or CC mode).
2	GND	**Ground.**
4	DRAIN	**Drain of the internal MOSFET.** DRAIN is integrated with an internal high-voltage current source, which charges up VCC for start-up.
5	SOURCE	**Source of the internal MOSFET.** Connect a current sense resistor to detect the MOSFET current for peak-current-mode control in CV and CC mode.
6	SS	**Select sampling time by different external resistor configurations.**
7	CP	**Output cable compensation.** Connect a 1µF ceramic capacitor to CP as a low-pass filter. The compensation voltage can be adjusted by the resistor divider. CP can also be used to select the secondary duty limitation by different external resistor configurations.
8	VCC	**Supply voltage.** When VCC is lower than a certain level, the internal high voltage current source is turned on to charge up VCC. When VCC is charged to a certain level by the internal high-voltage current source, the IC begins working. In addition to the bulk capacitor, a 0.1µF ceramic capacitor can be connected as close to VCC as possible to decouple the noise disturbance.

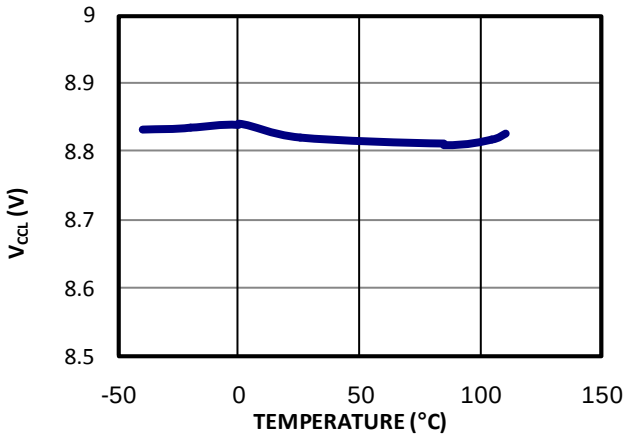
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TYPICAL CHARACTERISTICS

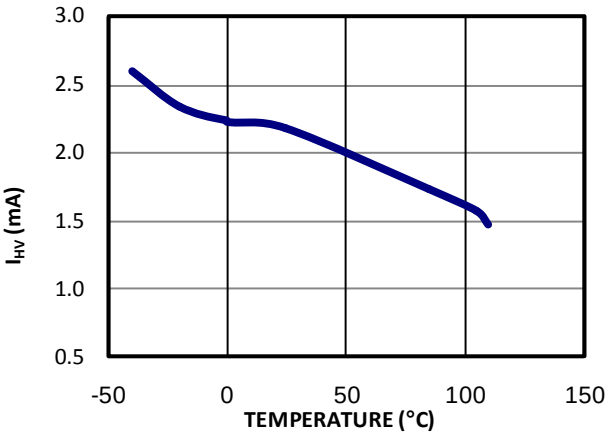
VCC On Threshold vs. Temperature



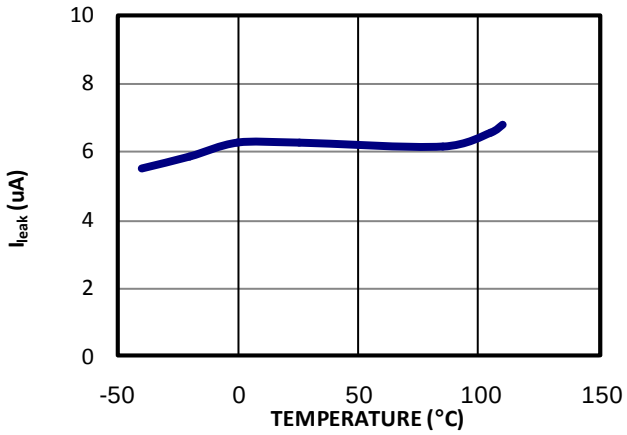
VCC Off Threshold vs. Temperature



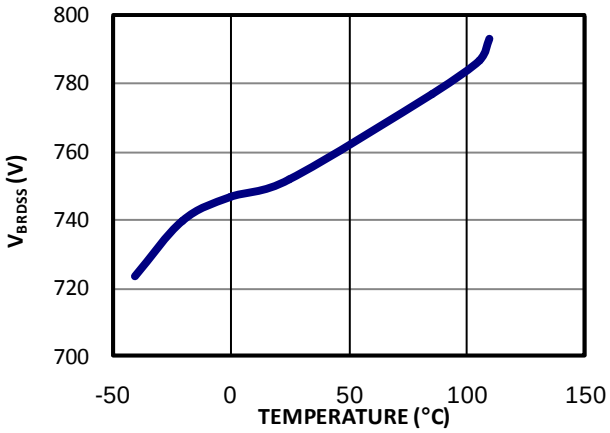
High-Voltage Current Source Supply Current @ V_D = 80V vs. Temperature



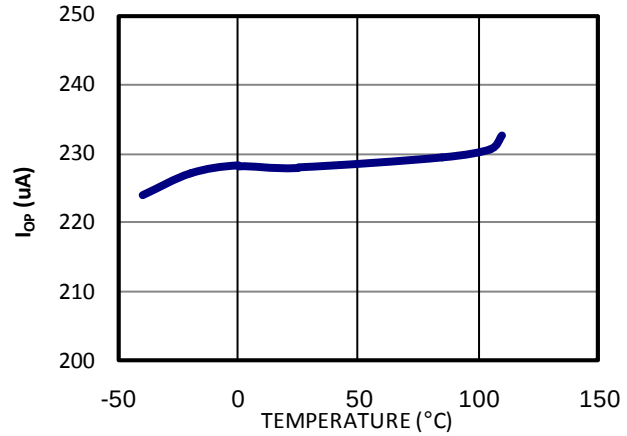
Leakage Current @ V_D = 400V vs. Temperature



Breakdown Voltage vs. Temperature



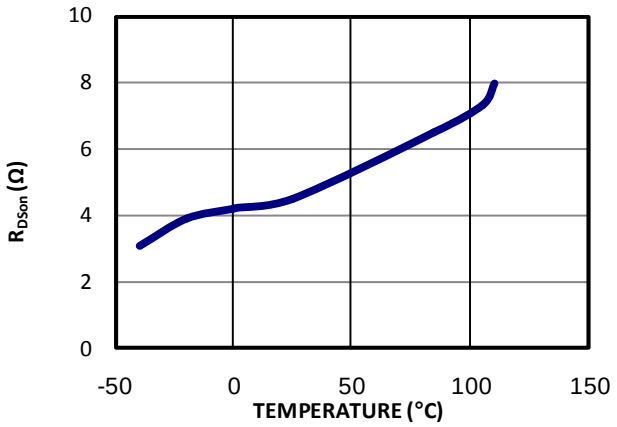
Operating Current @ F_{s_min} vs. Temperature



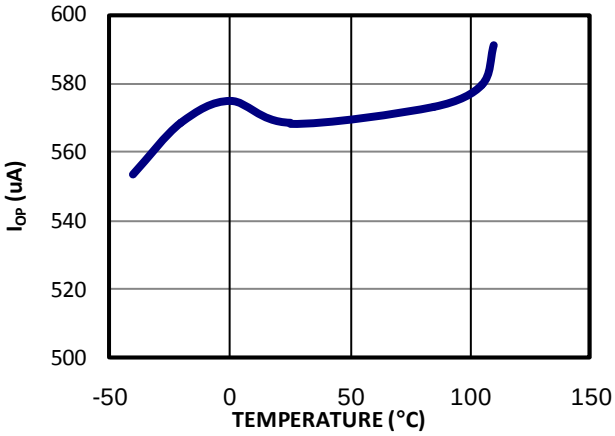
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TYPICAL CHARACTERISTICS *(continued)*

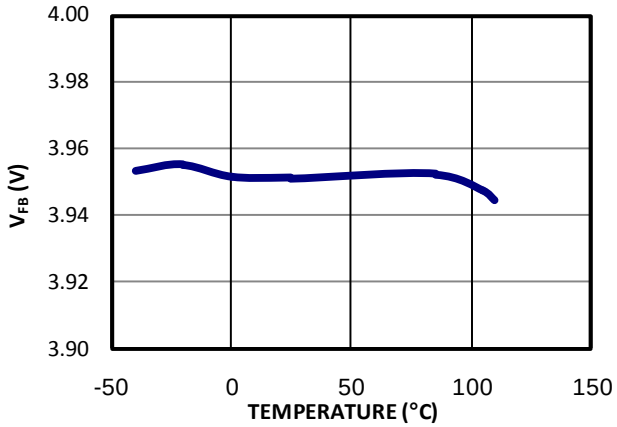
On-State Resistance vs. Temperature



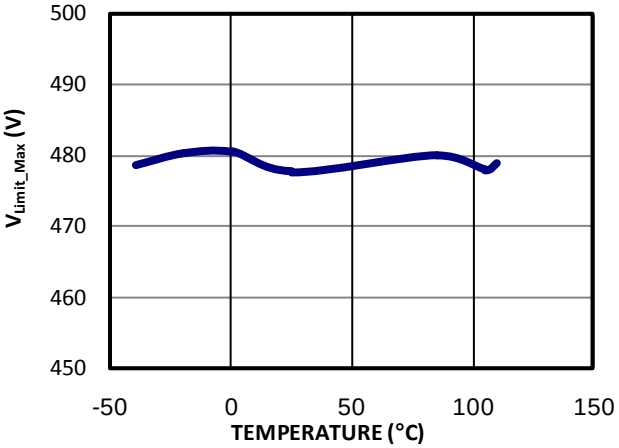
Operating Current @ f_S = 40kHz vs. Temperature



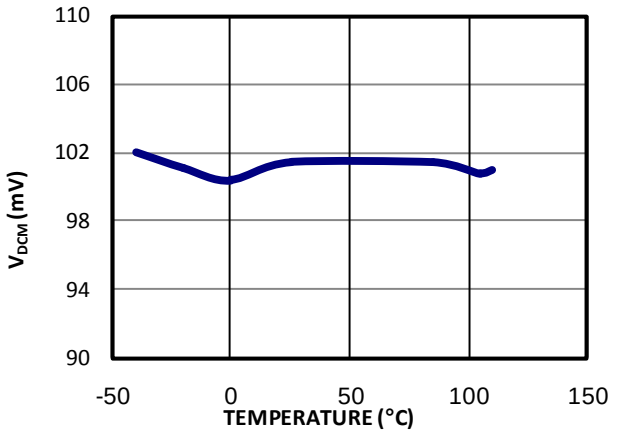
FB Reference Voltage vs. Temperature



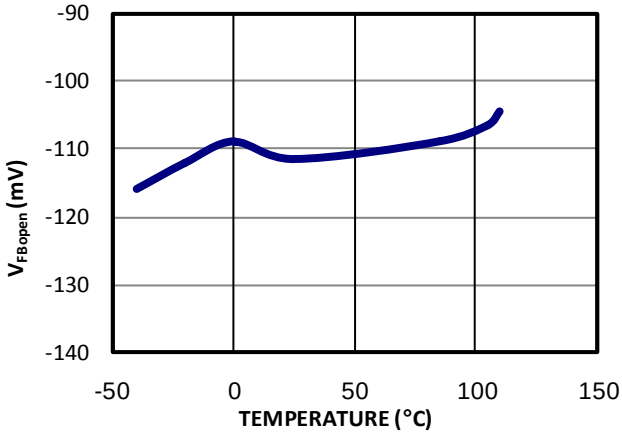
Current Limit vs. Temperature



ZCD Threshold vs. Temperature



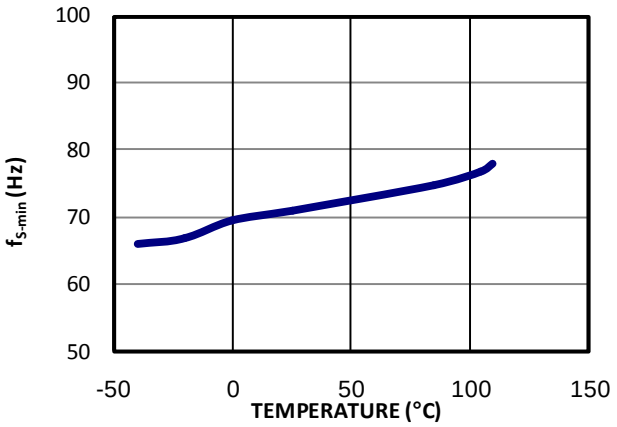
FB Open-Circuit Threshold vs. Temperature



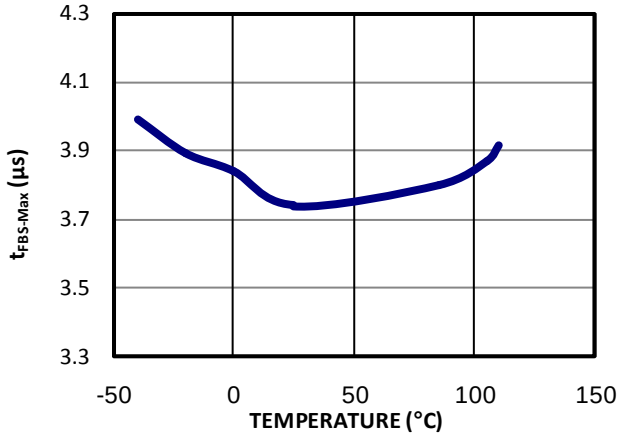
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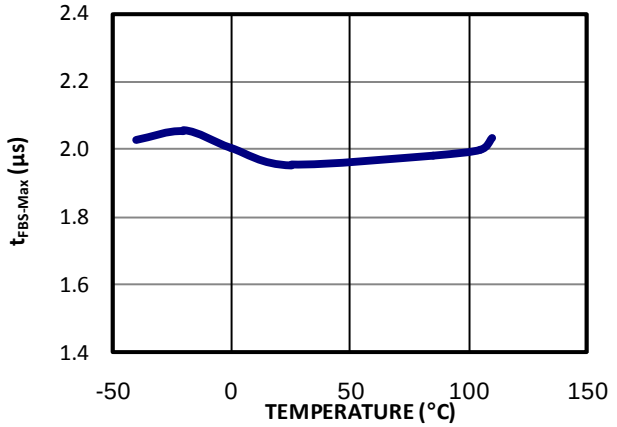
Minimum Switching Frequency vs. Temperature



FB Maximum Sampling Time @ R_{SS} = 0Ω vs. Temperature



FB Minimum Sampling Time @ R_{SS} = 0Ω vs. Temperature

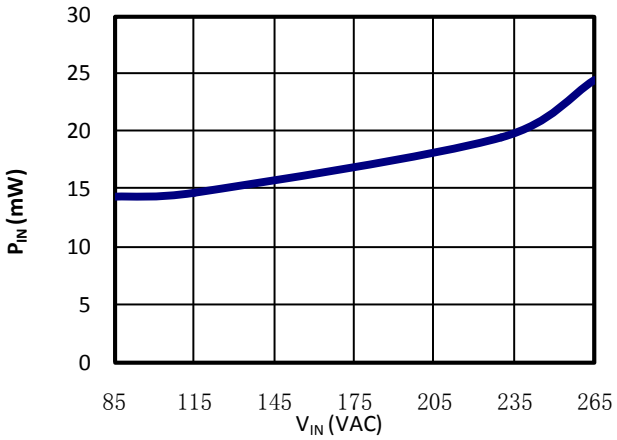


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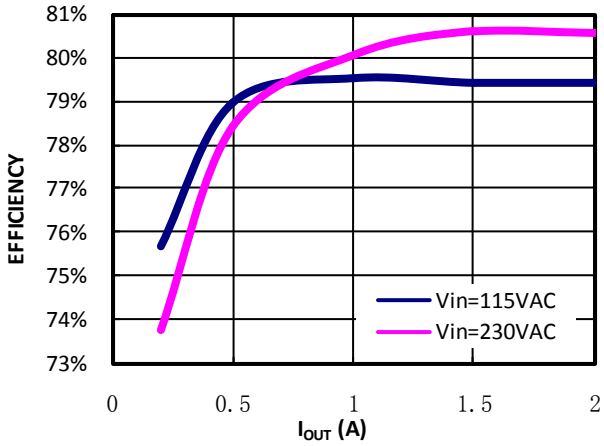
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 2A, unless otherwise noted.

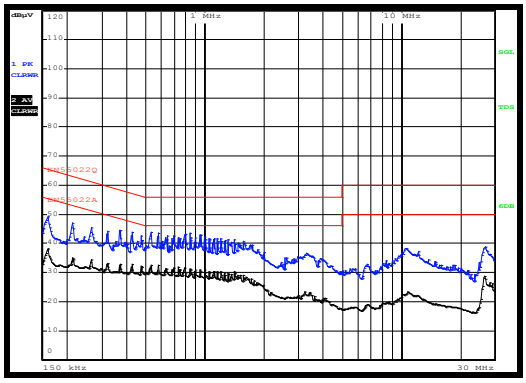
No-Load Consumption



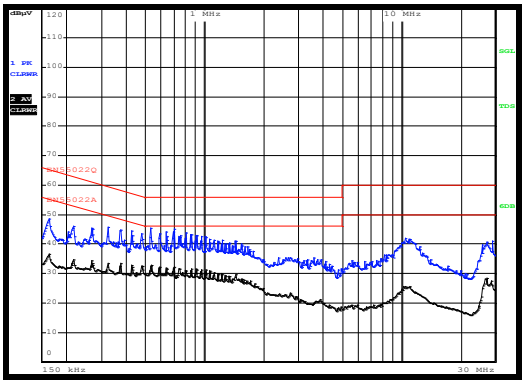
Efficiency



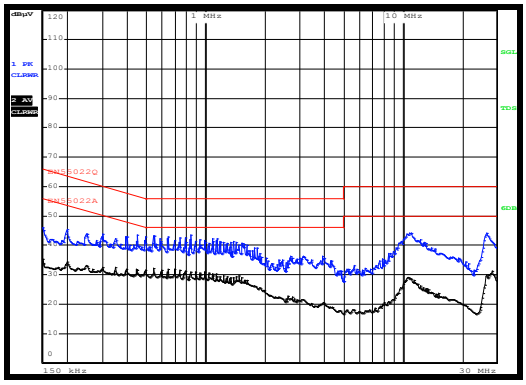
Conducted EMI
V_{IN} = 115V_{AC}, L Line



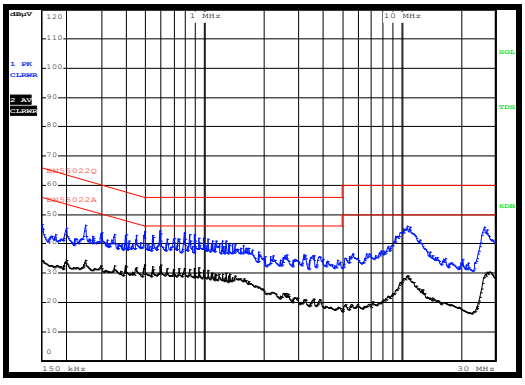
Conducted EMI
V_{IN} = 115V_{AC}, N Line



Conducted EMI
V_{IN} = 230V_{AC}, L Line



Conducted EMI
V_{IN} = 230V_{AC}, N Line



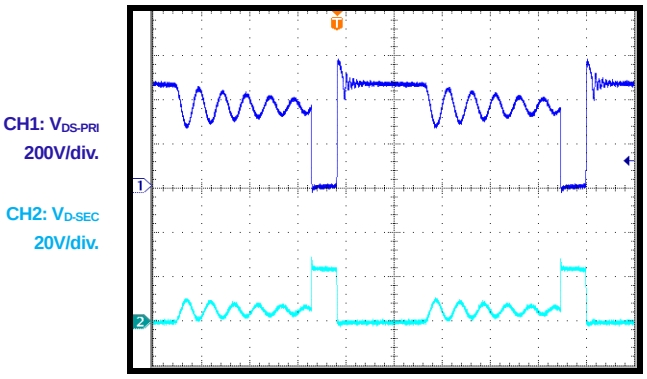
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT}=2A, unless otherwise noted.

Steady State

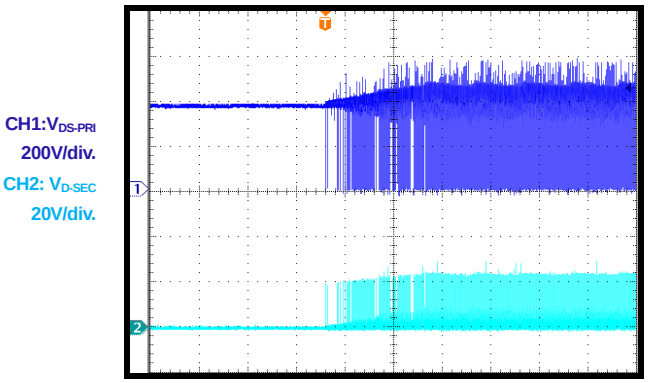
V_{IN} = 265V_{AC}



4µs/div.

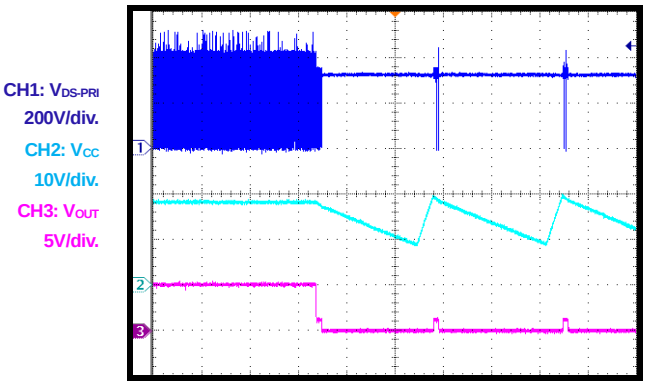
Power On

V_{IN} = 265V_{AC}



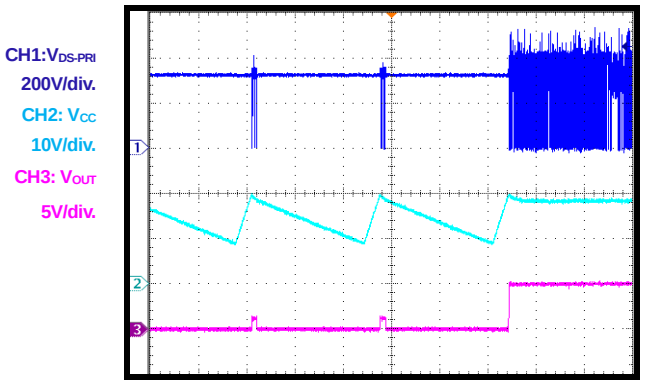
10ms/div.

OLP Entry



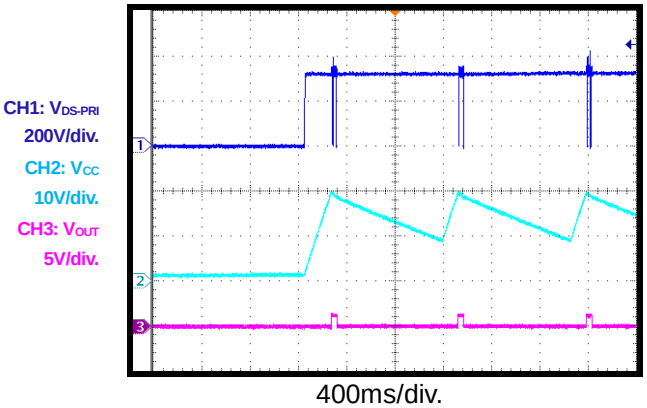
400ms/div.

OLP Recovery



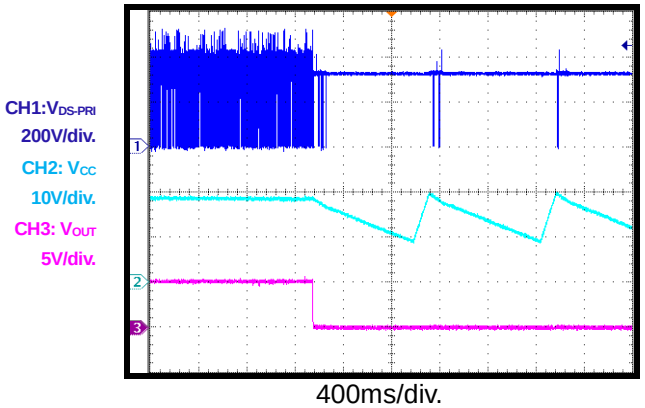
400ms/div.

OLP Power On



400ms/div.

Short-Circuit Entry



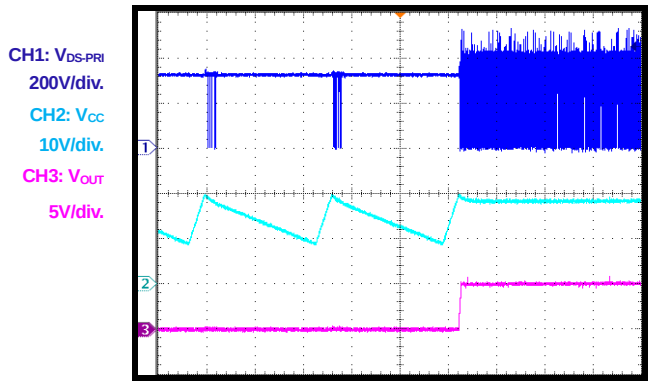
400ms/div.

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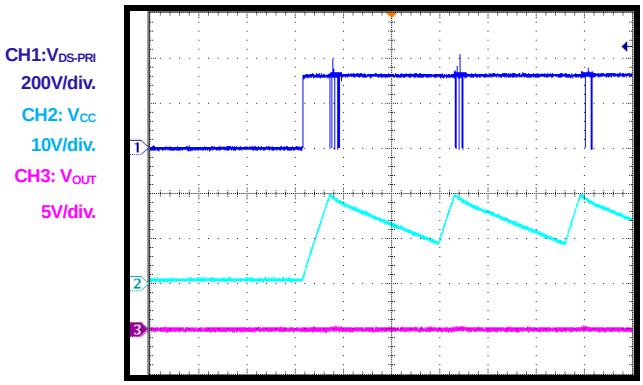
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 2A, unless otherwise noted.

Short-Circuit Recovery



Short-Circuit Power On



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BLOCK DIAGRAM

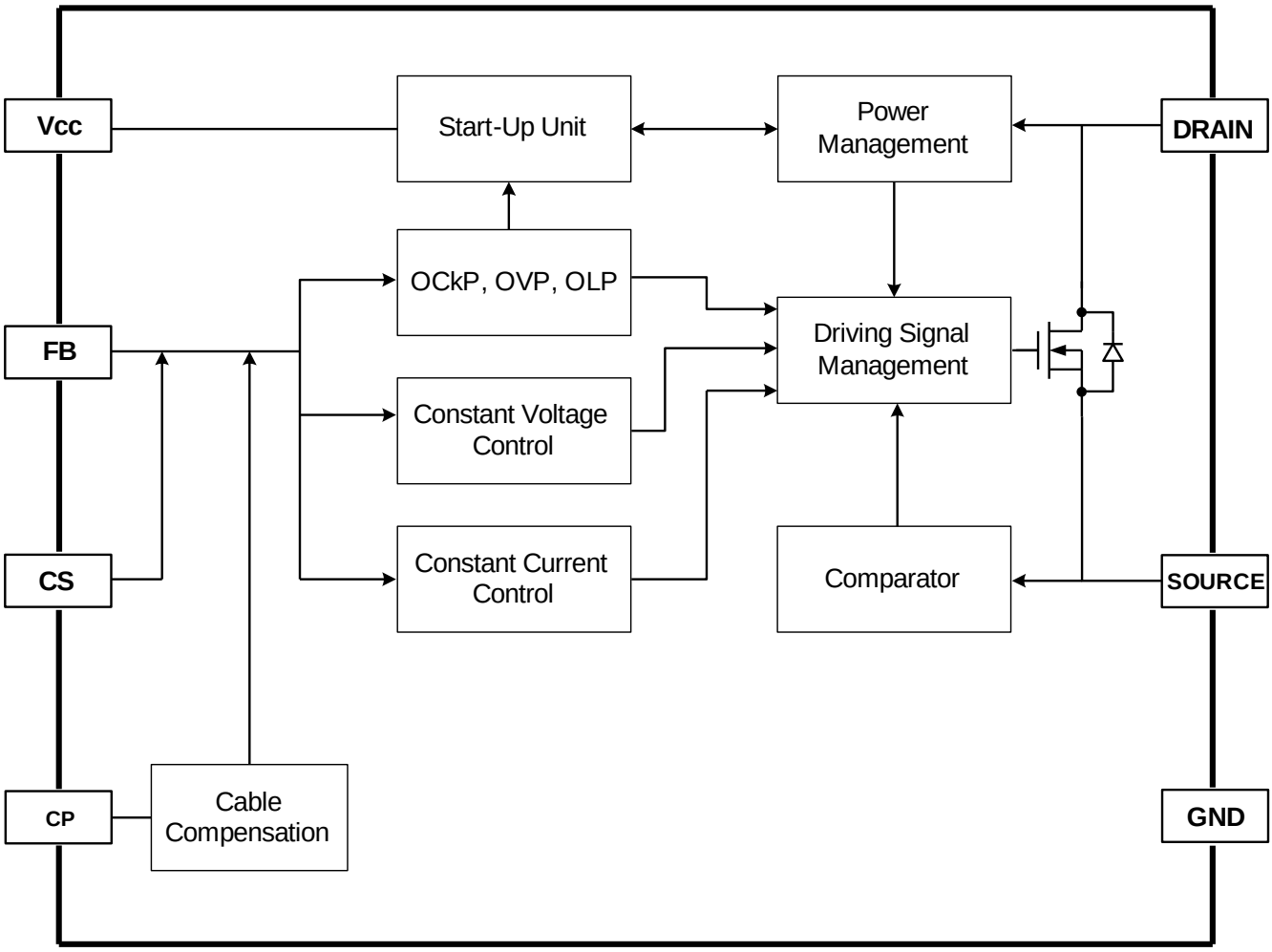


Figure 1: Functional Block Diagram

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OPERATION

The MP024-10 is a primary-side flyback regulator that provides accurate constant voltage and constant current regulation without an optocoupler or secondary feedback circuit. The regulator is designed to operate with a minimal number of external components.

Start-Up

Initially, the IC is self-supplied by the internal high-voltage current source, which is drawn from DRAIN. The internal high-voltage current source turns off for better efficiency once VCC reaches the VCC on threshold (V_{CCH}). Afterward, the power supply is taken over by the auxiliary winding of the transformer. When VCC falls below the VCC off threshold (V_{CCL}), the IC stops switching, and the internal high-voltage current source turns on again (see Figure 2).

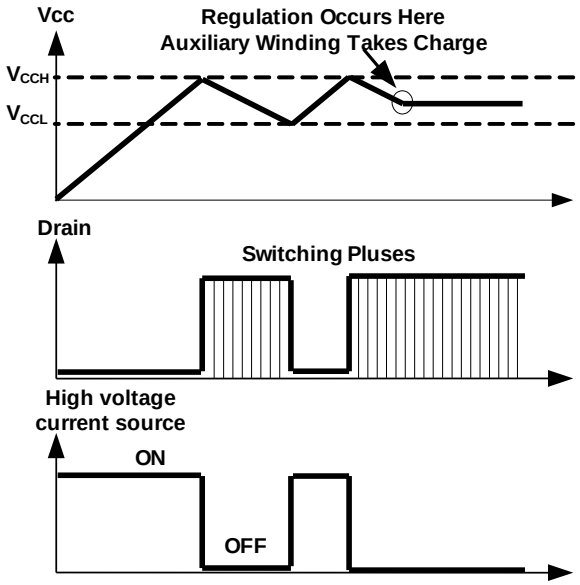


Figure 2: VCC Under-Voltage Lockout

Peak-Current Control on the Primary Side

A current sense resistor (R_S) is used to sense the primary current $I_p(t)$ (see Figure 3). The current rises linearly at a rate shown in Equation (1):

$$\frac{dI_p(t)}{dt} = \frac{V_{in}}{L_m} \quad (1)$$

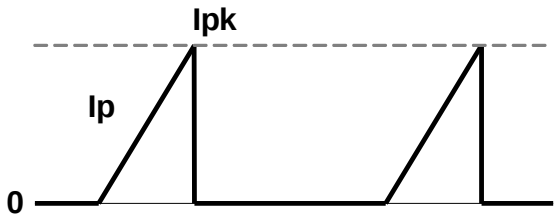


Figure 3: Primary Current Waveform

When the current $I_p(t)$ rises up to I_{pk}, the MOSFET turns off. Calculate I_{pk} with Equation (2):

$$I_{pk} = \frac{V_{IPK}}{R_S} \quad (2)$$

The energy stored in the inductor (L_m) within each cycle can be calculated with Equation (3):

$$E = \frac{1}{2} L_m \times I_{pk}^2 \quad (3)$$

The power transferred from the input to the output can be calculated with Equation (4):

$$P = \frac{1}{2} L_m \times I_{pk}^2 \times f_s \quad (4)$$

Where f_s is the switching frequency.

In constant current operation, the reference for I_{pk} is fixed at $V_{Limit-Max}$. In constant voltage operation, I_{pk} is modulated by the switching frequency (see Figure 4).

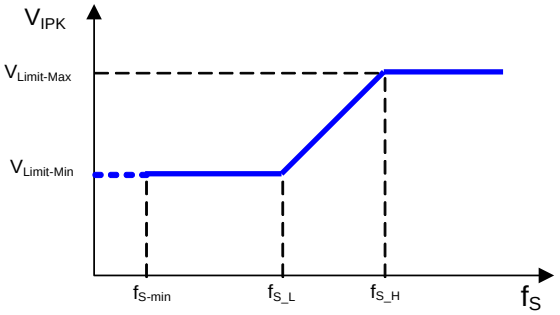


Figure 4: Peak Current Modulation

The turn-on time is limited at t_{ONmax} in case the current sensing resistor is shorted and the primary current runs away. If this maximum limitation is reached, IC protection is triggered.

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Constant Voltage (CV) Operation

In constant voltage (CV) mode, the MP024-10 detects the output voltage from FB and generates the switching frequency to regulate the output voltage.

To regulate the output voltage on the primary side, FB uses a resistor divider to sample the auxiliary winding voltage (V_{aux}). The relationship between V_{aux} and the output voltage (V_o) can be calculated with Equation (5):

$$V_{aux} = \frac{N_{aux}}{N_s} \times (V_O + V_D) \quad (5)$$

Where V_D is the forward drop voltage of the secondary diode.

During the conduction time of the secondary diode, the difference between the output voltage and the voltage on the secondary winding is not constant, since V_D varies with the current flowing through the diode. To compensate for the voltage drop difference, the sampling time decreases gradually from $t_{FBS-Max}$ to $t_{FBS-Min}$ as the current limitation folds back from $V_{Limit-Max}$ to $V_{Limit-Min}$ (see Figure 5).

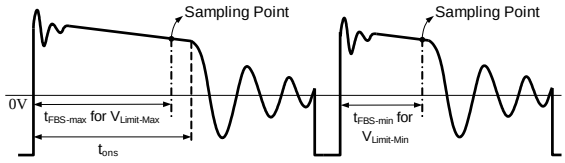


Figure 5: Auxiliary Winding Voltage

The FB sampling time is able to be customized with different resistor values connected to SS (see Figure 6). See the Electrical Characteristics table on page 5 for all available choices for the sampling time. The entire customization process is completed before start-up and stored in a register, so it does not have any influence on the normal operation.

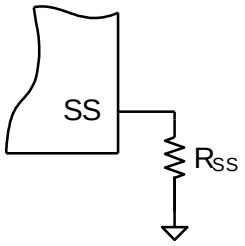


Figure 6: External Resistor for Sampling Time Customization

The sampling should be chosen almost at the end of the secondary diode conduction period for accurate CV regulation.

Constant Current (CC) Operation

Figure 7 shows the secondary current waveforms.

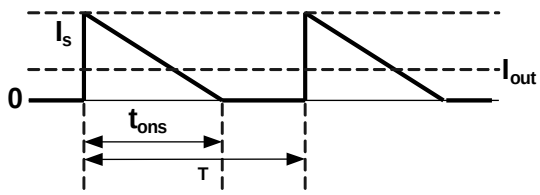


Figure 7: Secondary Current Waveform

In constant current (CC) operation, I_{pk} is fixed, and the CC loop control function maintains a fixed ratio between the secondary diode on time (t_{ons}) and the switching cycle. The fixed ratio limits the maximum duty of the secondary side diode on time as shown in Equation (6):

$$\frac{t_{ons}}{T} = D_{S-Max} \quad (6)$$

The relationship between the output constant-current and the secondary peak current (I_{pks}) is shown in Equation (7):

$$I_{out} = \frac{1}{2} I_{pks} \frac{t_{ons}}{t_{ons} + t_{offs}} = \frac{1}{2} I_{pks} D_{S-Max} \quad (7)$$

When the secondary diode is turned on, the peak current on the secondary side can be calculated with Equation (8):

$$I_{pks} = \frac{N_p}{N_S} I_{PK} \quad (8)$$

The output current regulation is shown in Equation (9):

$$I_{out} = \frac{1}{2} \frac{N_p}{N_S} I_{PK} D_{S-Max} \quad (9)$$

For different applications with different kinds of output voltages, D_{S-Max} can be customized from CP. If CP is connected with a capacitor directly or shorted to GND, D_{S-Max} remains at a default value of 0.4.

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If CP is connected with a resistor, then there are several options for the CP and D_{S-Max} combination (see Figure 8).

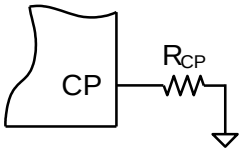


Figure 8: External Configuration of CP

Table 1 shows all available choices for D_{S-Max}. The entire customization process is completed before start-up and latched in a register, so it does not have any influence on the normal operation.

Table 1: D_{S-Max} vs. CP Configuration

R_{CP}/C_{CP}	D_{S-Max}
0Ω/NC	0.4
10kΩ/NC	0.3
20kΩ/NC	0.35
40kΩ/NC	0.5
NC/1μF	0.4

To enable the overload protection (OLP) function in CC mode, the sampling on the FB voltage should be running, and the sampling time should be fixed at $t_{FBS-Max}$.

Leading-Edge Blanking

The MP024-10 uses a leading-edge blanking period when the MOSFET turns on. Leading-edge blanking is used to prevent a false termination of the switching pulse caused by the turn-on current spike. During this blanking period, the current sense comparator is disabled, and the MOSFET cannot be turned off.

Discontinuous Conduction Mode (DCM) Detection

The MP024-10 is designed to operate in discontinuous conduction mode (DCM) in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the MP024-10 implements a zero-current detection function internally with a threshold of V_{DCM}. The IC does not begin the next cycle until ZCD is detected.

During normal operation, the blanking time for ZCD is synchronized with the FB sampling time (i.e.: ZCD always starts after the sampling phase is done). There is also a soft-start (SS) function on the ZCD blanking time that prevents ZCD from being falsely triggered when the output capacitor is not charged up. During the start-up period, the blanking time for ZCD gradually shrinks from t_{B_STP} (10μs) to the FB sampling time in three cycles.

Protection Features (OVP, OCkP, SSP, and OLP)

The MP024-10 includes over-voltage protection (OVP), open-circuit protection (OCkP), sensing-short protection (SSP), and overload protection (OLP). If the voltage at FB exceeds V_{FBovp}, OVP is triggered. If V_{FBopen} cannot be monitored for each cycle, OCkP is triggered. If the maximum turn on time is reached, SSP is triggered. If the sampled FB voltage is lower than V_{FBolp} for 128 consecutive cycles, OLP is triggered. The MP024-10 immediately shuts down the driving signals and enters hiccup mode when any of these protection features are triggered and resumes normal operation when the fault has been removed.

OLP is not enabled until the soft-start period of the ZCD blanking time is finished.

Over-Temperature Protection (OTP)

When the junction temperature of the IC exceeds the thermal shutdown threshold, over-temperature protection (OTP) is triggered, and the IC stops switching. The MP024-10 resumes normal operation when the junction temperature drop exceeds the thermal shutdown hysteresis.

Output Cable Compensation

The MP024-10 has an internal output cable compensation circuit (see Figure 9). A switching signal (V_{Limit}*t_{ONS}) is generated internally and is synchronized with the switching frequency. The duty on time of this signal is t_{ONS}, and the amplitude of this signal is proportional to the current limit threshold. The switching signal is output to CP through a 1MΩ resistor. A low-pass filter can be implemented by placing an external capacitor on CP, and a DC voltage (V_{CP}) that is proportional to the output current can be derived on CP.

An internal current sinking into FB is proportional to V_{CP}, so the voltage drop on the upper resistor of the divider implements the output cable compensation function.

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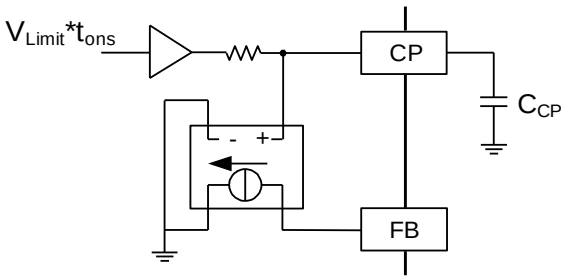


Figure 9: Output Cable Compensation

Determine the compensation voltage with Equation (10):

$$V_{FCP} = \frac{8 \times V_{Limit} \times D_S}{300 \times 10^3} \times 2 \times R_{UP} \times \frac{N_S}{N_{P_AU}} \quad (10)$$

Where V_{FCP} is the secondary-side compensation voltage drop, D_S is the secondary-diode duty cycle, R_{UP} is the upper resistor of the resistor divider, N_S is the number of turns for the secondary-side transformer windings, N_{P_AU} is the number of transformer auxiliary winding turns, and V_{Limit} is the current limit.

For example, to calculate the maximum output cable compensation in CC condition, use D_S = $D_{S\text{-}Max}$ (when CP function is used, $D_{S\text{-}Max}$ is 0.4) and V_{Limit} = $V_{Limit\text{-}Max}$ (typically 480mV) in the formula. The compensation voltage drops as V_{Limit} or D_S decrease along with the load current. The CP voltage is 8*V_{Limit}*D_S.

Connect a 1µF capacitor to CP for cable compensation. Since CP is also used for $D_{S\text{-}Max}$ customization, the cable compensation function is only available when CP is connected to the capacitors directly. If there is any non-zero resistor connected to CP, all of the internal blocks related to the cable compensation function are disabled and there is no current sinking into FB.

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APPLICATION INFORMATION

Input Filter

The input filter helps to maintain the bus voltage when the AC input voltage is low.

Figure 10 shows the typical input filter of an application with a low power range. The bulk capacitors (C1 and C2) filter the rectified AC input. Usually, C1 and C2 are set at 2μF/W to 3μF/W for a universal input condition. For $230V_{AC}$ single-range applications, cut the capacitor values in half. The inductor (L) forms a pi (π) filter with C1 and C2 to restrain the differential mode EMI noise. The resistor (R) in parallel with L dampens the mid-frequency band EMI noise, if necessary. Normally, R is 1kΩ to 10kΩ.

Figure 11 shows the typical DC bus voltage waveform after the rectifier.

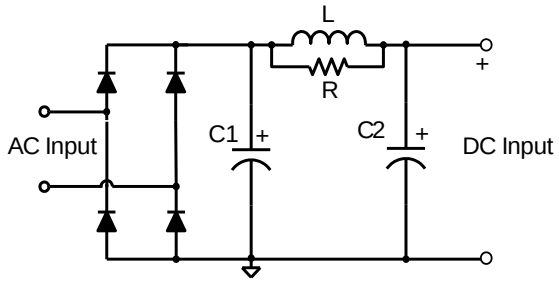


Figure 10: Input Filter

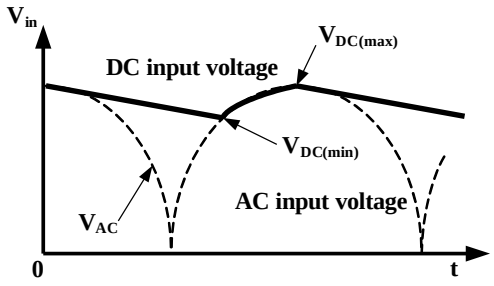


Figure 11: DC Input Voltage Waveform

A low DC input voltage causes insufficient output current due to the maximum on-duty limitation of the secondary side. To prevent this, calculate the minimum input DC voltage with Equation (11):

$$V_{DC(min)} \geq \frac{N_p}{N_s}(V_O + V_D)\frac{D_{S-Max}}{1-D_{S-Max}} \quad (11)$$

If $V_{DC(min)}$ cannot satisfy this expression, use larger input capacitors to increase $V_{DC(min)}$.

Output Capacitor

Low or very low ESR output capacitors are recommended to meet the output voltage ripple requirements. Low ESR capacitors improve the output voltage regulation accuracy at high or low temperatures and can provide better efficiency than high ESR output capacitors.

Output Diode Or Synchronous Rectifier

Schottky diodes are recommended for their fast switching speed and low forward voltage drop for better high or low temperature CV regulation and efficiency.

If lower average efficiency (3% to 4%) is acceptable, replace the output diode with a fast or ultra-fast diode to reduce cost. Re-adjust the resistor divider values for an accurate output voltage since the forward voltage drop is higher than the Schottky diode.

If the circuit has a high efficiency requirement, it is recommended to use a synchronous rectifier (SR) instead. The MP6906 is a suitable SR controller where the output voltage is low and there is no need for a secondary auxiliary winding (see Figure 12). The MP6906 is available in a SOT23-6 package, which only requires few extra PCB dimensions and external components.

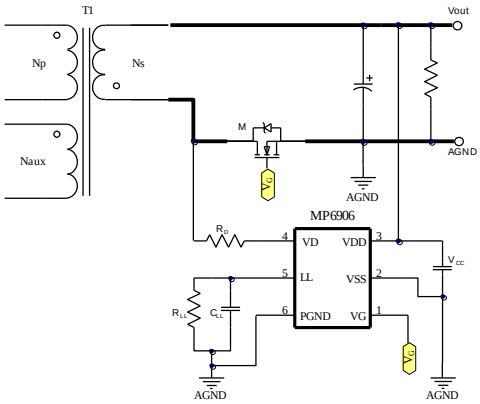


Figure 12: Synchronous Rectifier

Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects either the output current or voltage constant precision. The transformer structure can be optimized to minimize the leakage inductance. The leakage inductance should be less than 5% of the primary inductance.

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RCD Snubber

The transformer's leakage inductance causes MOSFET drain voltage spikes and excessive ringing on the drain voltage waveform, which affects the output voltage sampling after the primary MOSFET turns off.

The RCD snubber circuit limits the drain voltage spike (see Figure 13).

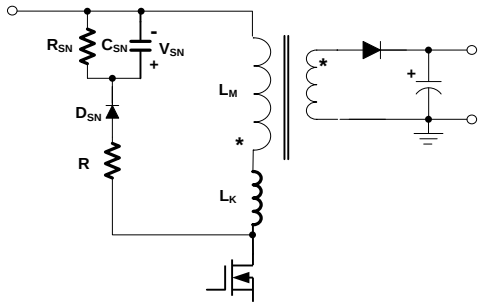


Figure 13: RCD Snubber

Select an appropriate R_{SN} and C_{SN} value to meet voltage spike requirements and improve system operation.

The power dissipated in the snubber circuit can be approximated with Equation (12):

$$P_{SN} = \frac{1}{2} L_K I_{PK}^2 \frac{V_{SN}}{V_{SN} - N_{PS} V_O} f_S \quad (12)$$

Where L_K is the leakage inductance, V_{SN} is the clamp voltage, and N_{PS} is the turn ratio of the primary-to-secondary side.

Since R_{SN} consumes the majority of the power, calculate R_{SN} with Equation (13):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (13)$$

The maximum ripple of the snubber capacitor voltage is then calculated with Equation (14):

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} R_{SN} f_S} \quad (14)$$

Generally, a 15% ripple is reasonable.

Select a time constant ($t = R_{SN} \cdot C_{SN}$) below 0.1ms for better CV sampling. Calculate C_{SN} using Equation (14).

The RCD resistor is a trade-off between the power loss and the acceptable clamp voltage in practical applications.

The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a damping resistor value in the range of 100Ω to 500Ω to restrain the drain voltage ringing.

Resistor Divider

For better application performance, select the resistor divider's total value with in the range of 10kΩ to 100kΩ. Smaller resistors will draw larger current from the auxiliary winding, which increases the no-load consumption, and larger resistors may pick up noise from adjacent components.

If there is oscillation or noise disturbing the FB sampling, an R-C filter can be inserted between the resistor divider and FB to achieve a stable voltage. The C_{FB} value is recommended to be several pF, and R_{FB} is recommended to be between 1kΩ and 2kΩ. R_{FB} can also limit substrate injection current effects (see Figure 14).

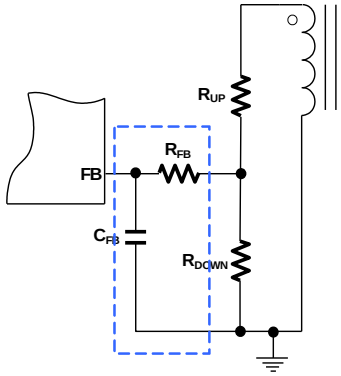


Figure 14: Feedback Resistor Divider Circuit

For accurate CV regulation, the accuracy of these feedback resistors should be at least 1%.

Dummy Load

When the system operates without any load, the output voltage rises above the normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. The dummy load is a trade-off between efficiency and load regulation. For example, a large dummy load can deteriorate efficiency and no-load consumption. For most applications, a dummy load of several mW is reasonable.

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Maximum Switching Frequency

The maximum switching frequency should be limited by the sampling point. The relationship between R_{SS} and the sampling time point is shown in the Electrical Characteristics table on page 5. The secondary on time must be longer than the maximum $T_{FBS-Max}$. Calculate T_{S_ON} with Equation (15):

$$T_{S_ON} = I_{PK} \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > t_{FBS_Max} + t_{FB_SD} \quad (15)$$

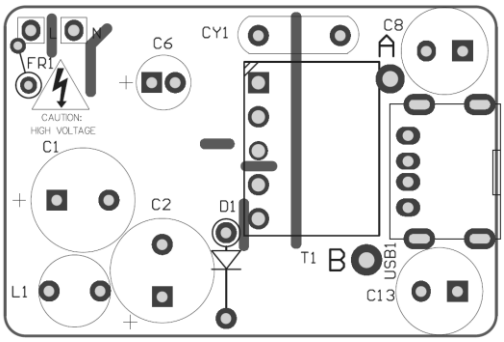
Where $T_{FBS-Max}$ is the FB maximum sampling time, and t_{FB_SD} is the FB sampling duration.

Combine Equation (14) and the relationship of R_{CP} and D_{S-Max} shown in Table 1 to fix the maximum switching frequency.

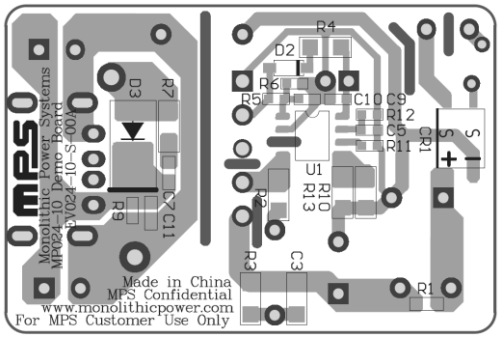
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI, and good thermal performance. For best results, refer to Figure 15 and follow the guidelines below.

1. Minimize the loop area formed by the input capacitor, the transformer's primary winding, the MOSFET drain and source of the MP024-10, and the sensing resistor to reduce EMI noise.
2. Minimize the voltage jumping area, such as the MOSFET drain, the anode of the secondary diode, etc. for better EMI.
3. Minimize the clamp circuit loop to reduce EMI.
4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise.
5. Provide sufficient copper areas at the cathode terminal of the output diode to act as a heat sink.
6. Place the AC input away from the switching nodes to minimize any noise coupling that may bypass the input filter.
7. Place the bypass capacitor as close to the IC as possible.
8. Place the feedback resistors next to FB and minimize the feedback sampling loop to minimize noise coupling.
9. Use a single-point connection at the negative terminal of the input filter capacitor for the IC GND and bias winding return.



Top Layer



Bottom Layer

Figure 15: Recommended Layout

Design Example

Table 2 shows a design example following the application guidelines.

Table 2: Design Example

V_{IN}	85Vac~265Vac, 47Hz/63Hz
V_{OUT}	5V
I_{OUT}	2A

Figure 16 shows the detailed application schematic. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUIT

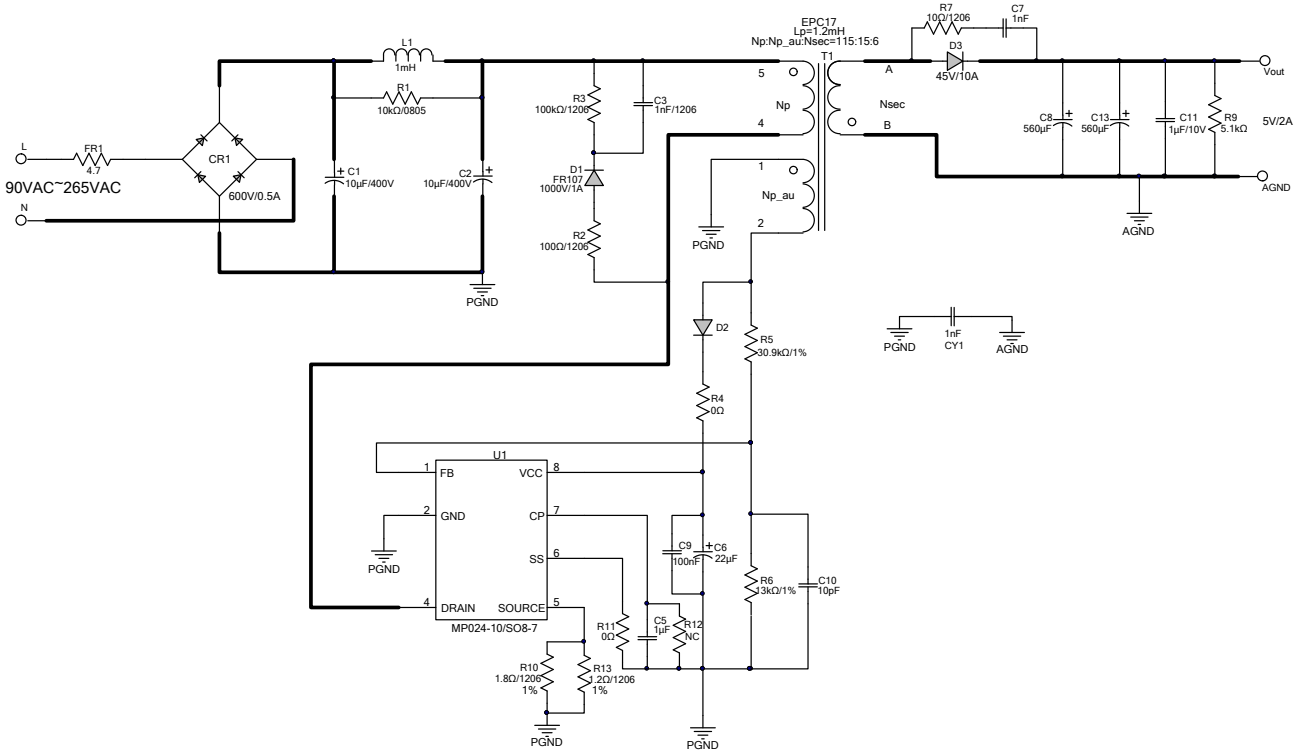


Figure 16: Universal Input, 5V/2A Output

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FLOW CHART

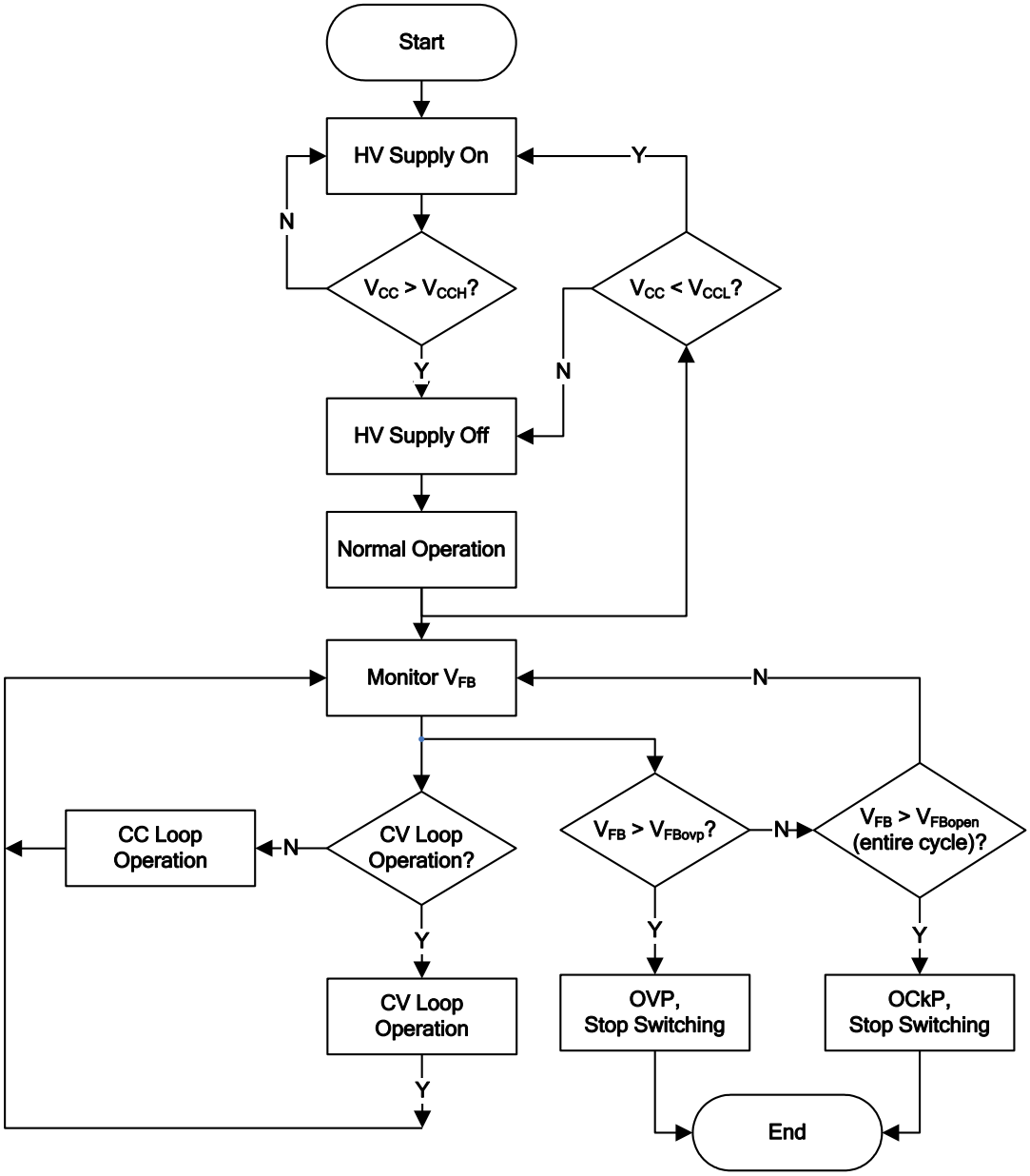


Figure 17: Flow Chart

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SIGNAL TIMING SEQUENCE WAVEFORM

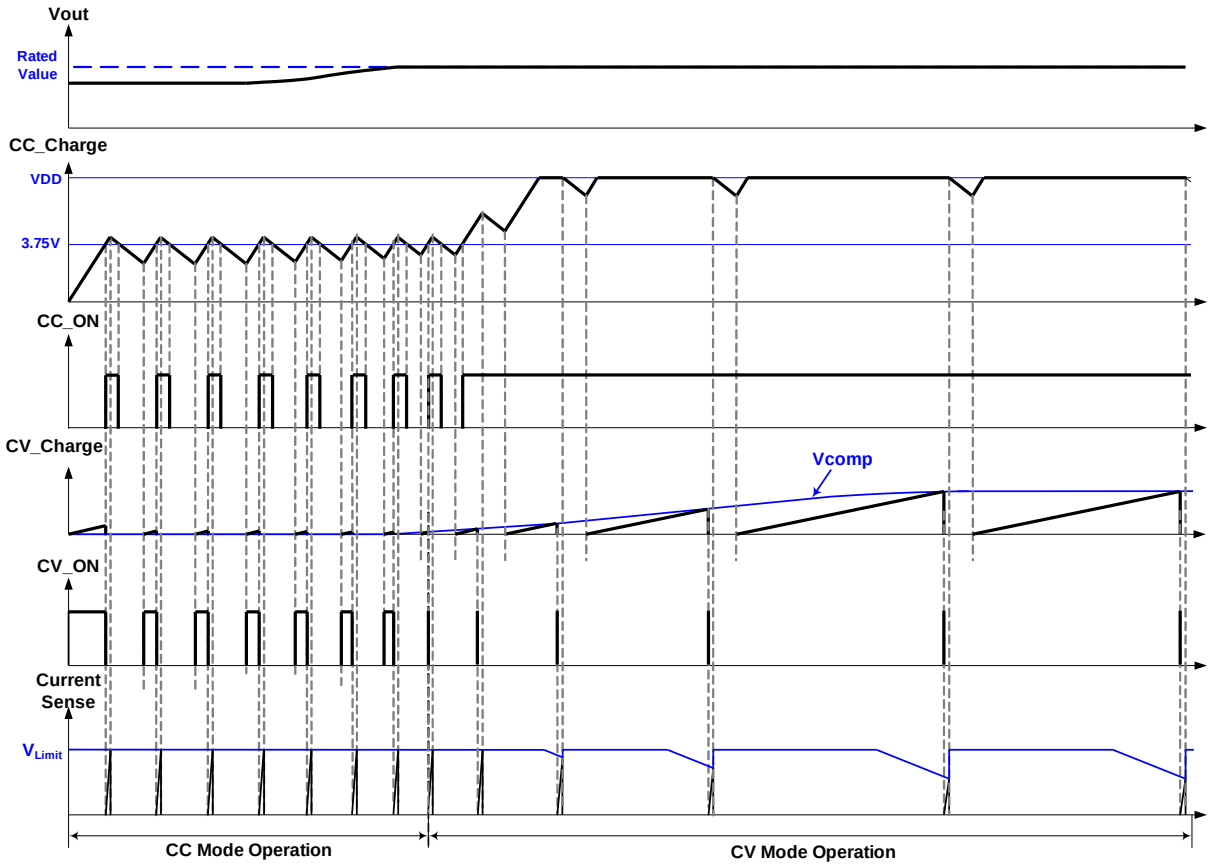


Figure 18: Start-Up Sequence

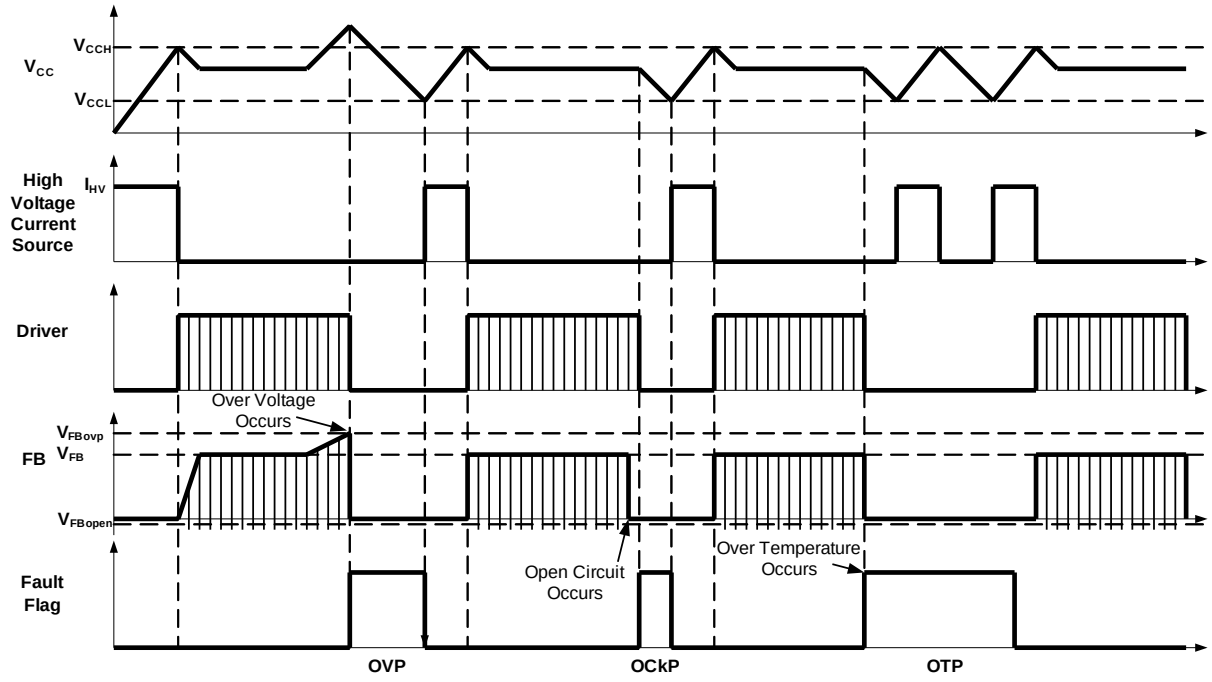
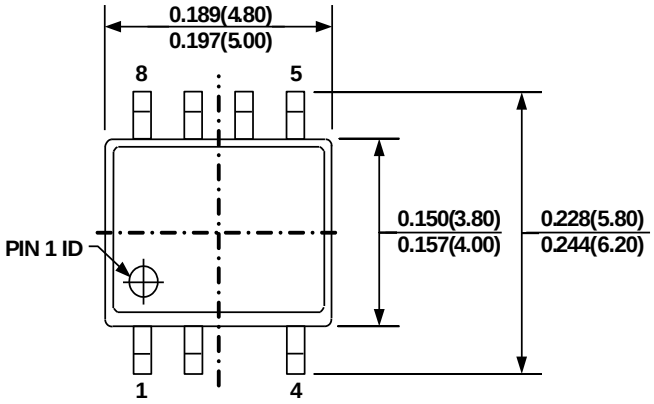


Figure 19: Protection Sequence

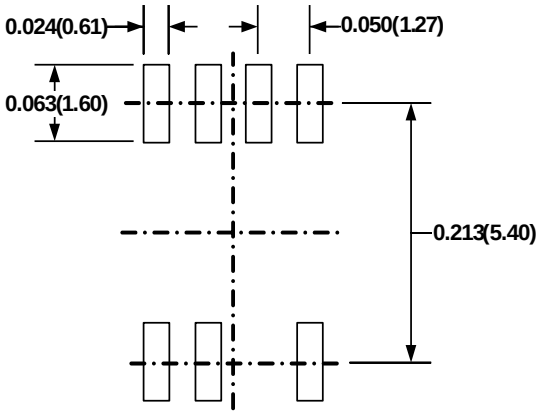
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PACKAGE INFORMATION

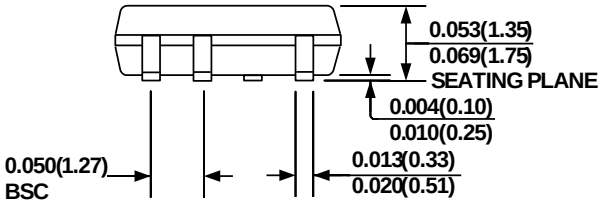
SOIC8-7B



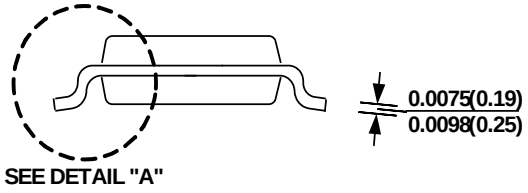
TOP VIEW



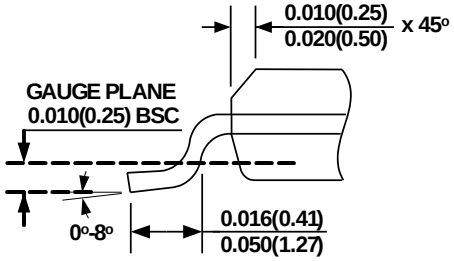
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE

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